

8bit Register with leds.

TITLE: Register

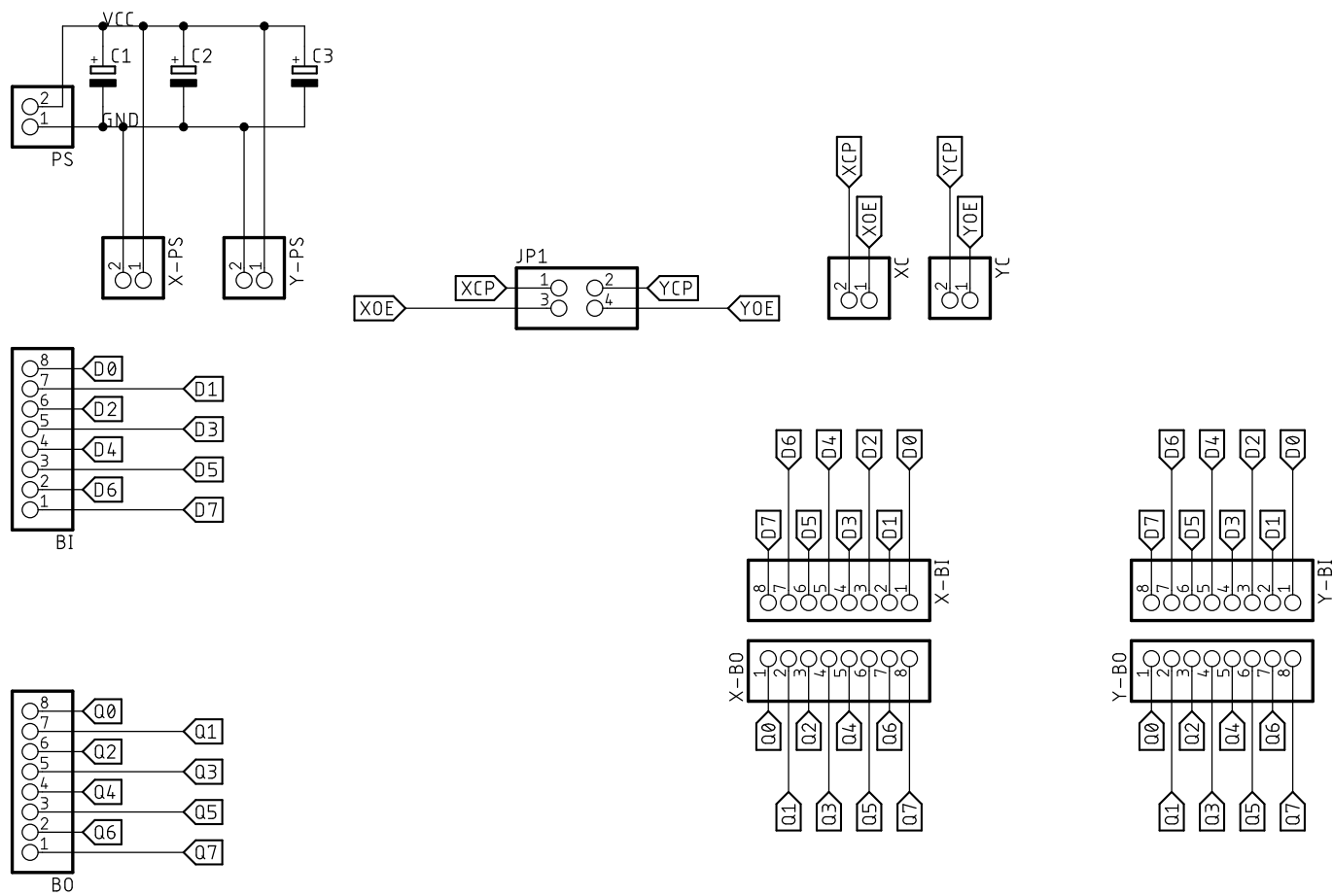
Document Number:

1

REV:
1.1

Date: 4. 1. 2022 16:18

Sheet: 1/1



Connection form bus to Registers modules.

TITLE: Register-Bus

Document Number:

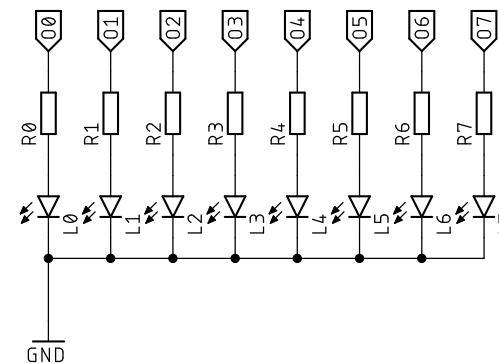
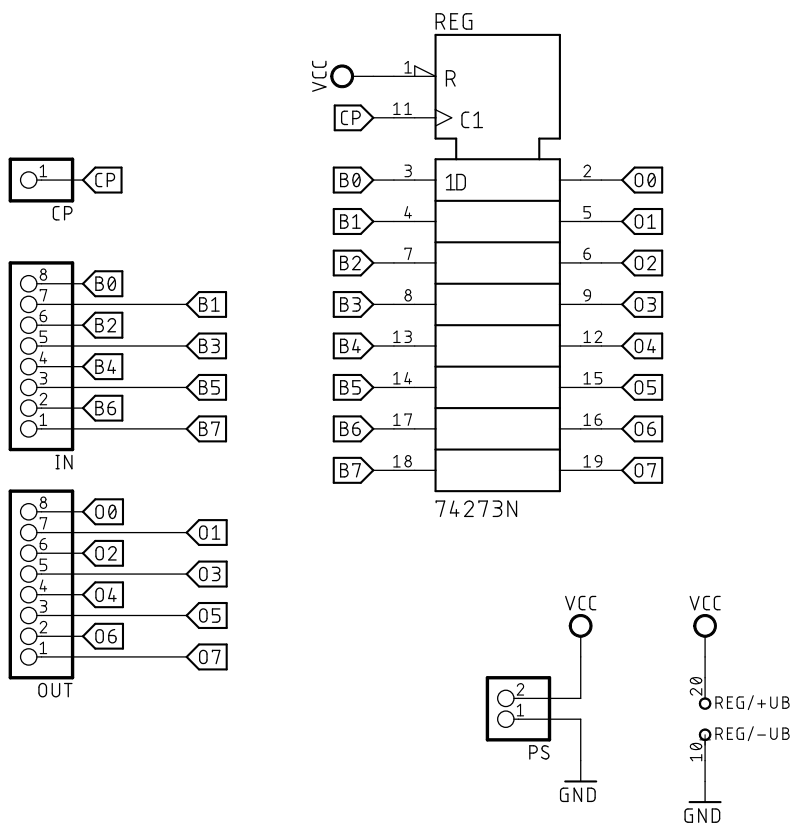
1.1

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Date: 16. 10. 2021 17:17

Sheet: 1/1



RAM register hold half of RAM ADDR

TITLE: RAM register

Document Number:

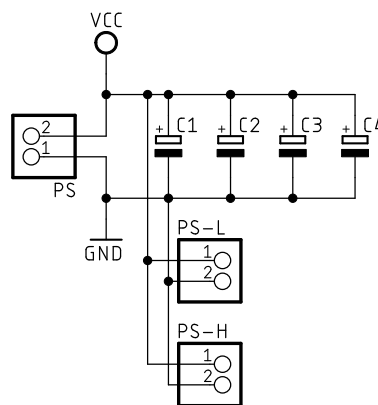
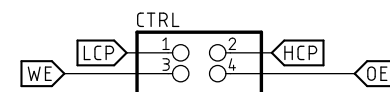
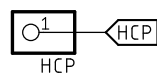
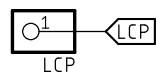
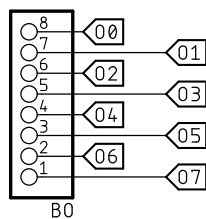
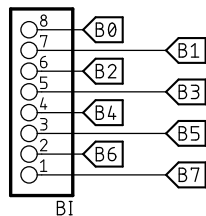
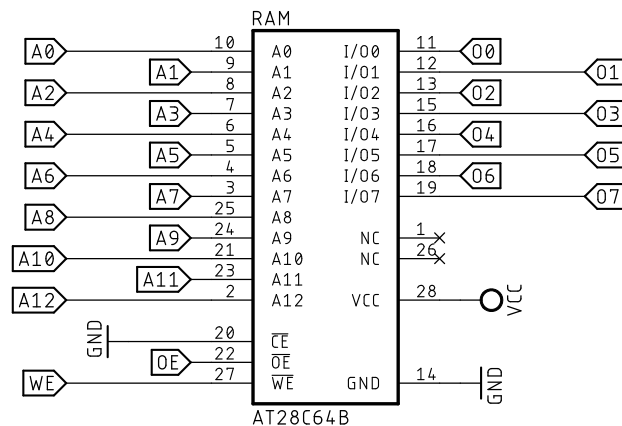
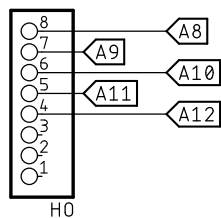
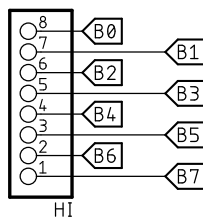
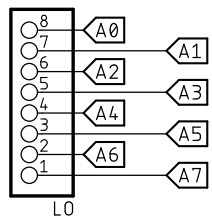
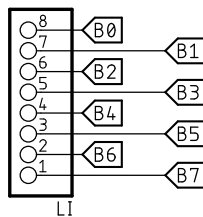
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Date: 29.10.2021 21:44

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RAM with registers

TITLE: RAM

Document Number:

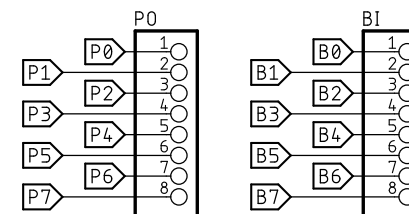
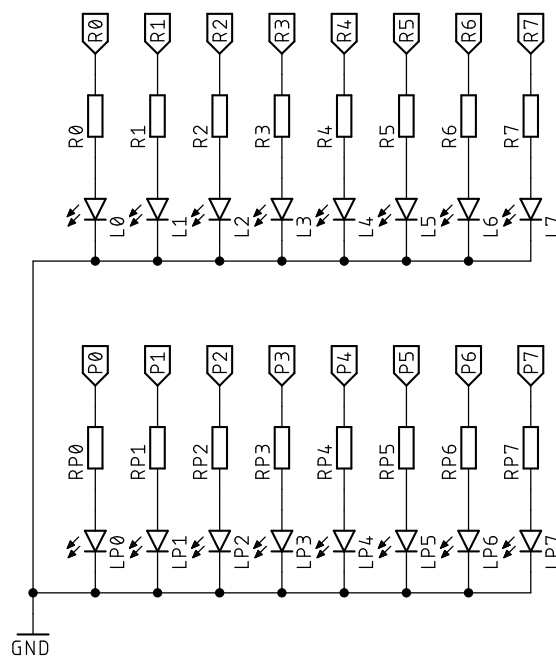
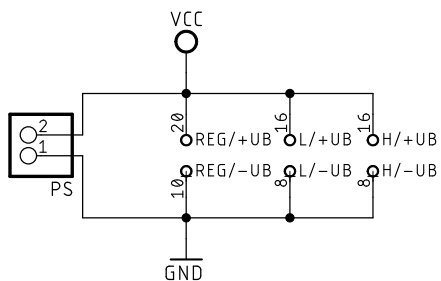
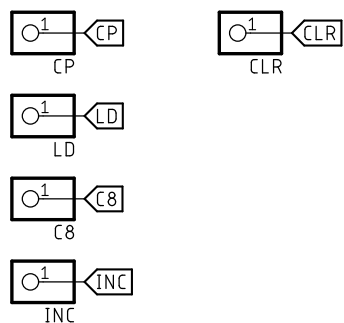
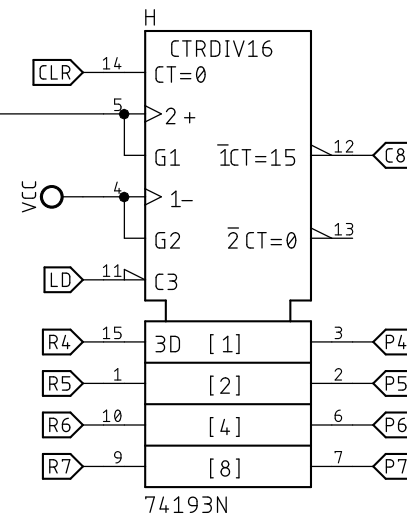
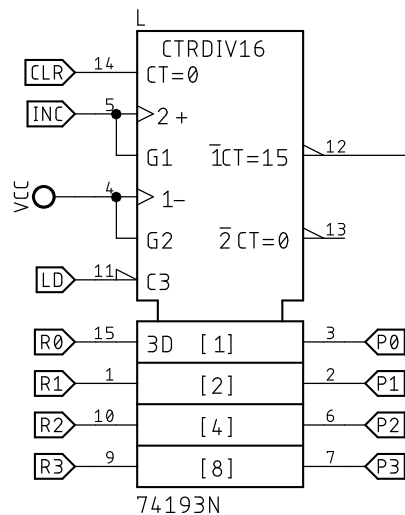
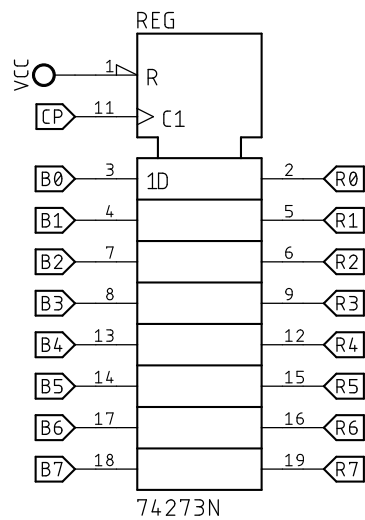
2.1

REV:

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Date: 29.10.2021 22:27

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Counter with register and LED

TITLE: Program Counter

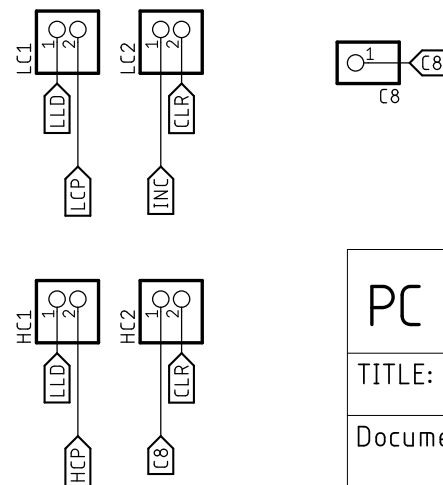
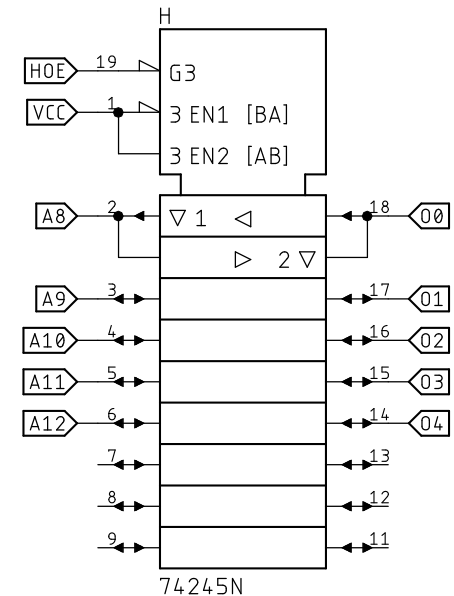
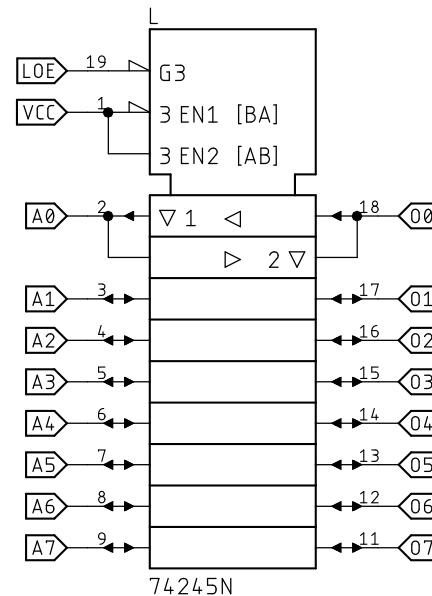
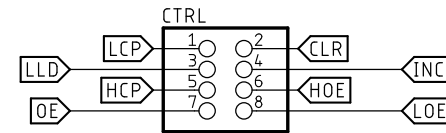
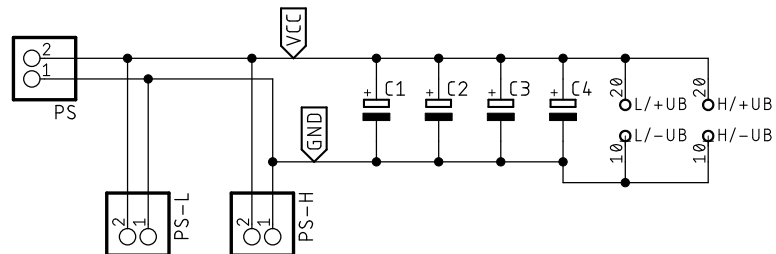
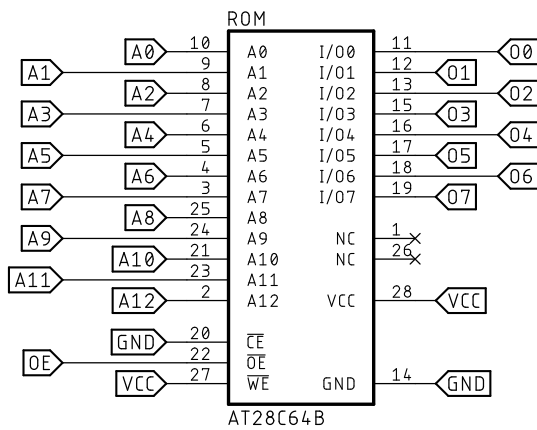
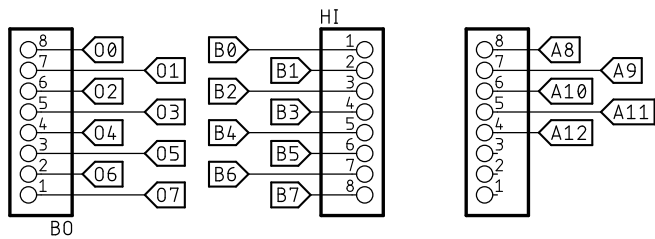
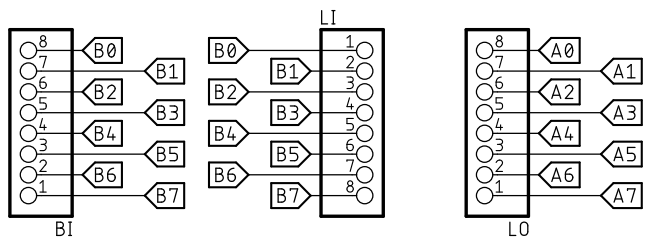
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Date: 16. 10. 2021 22:15

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PC and RAM

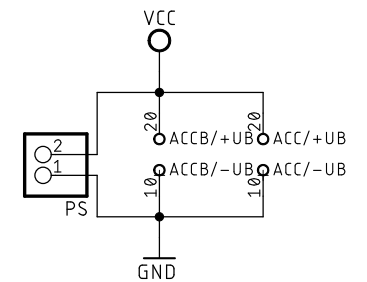
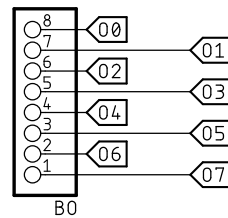
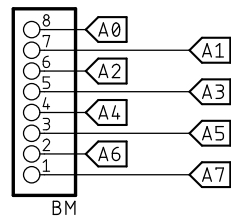
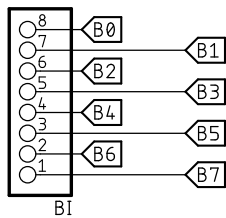
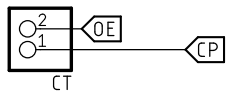
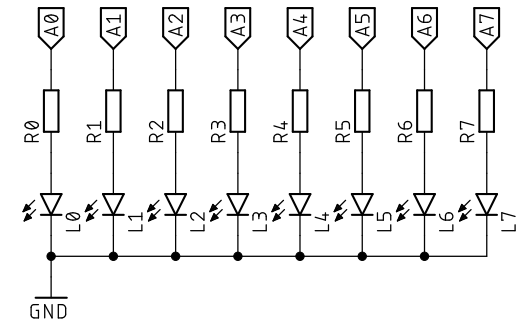
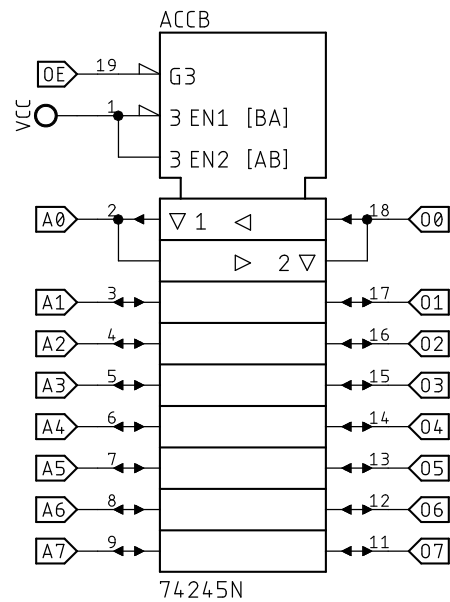
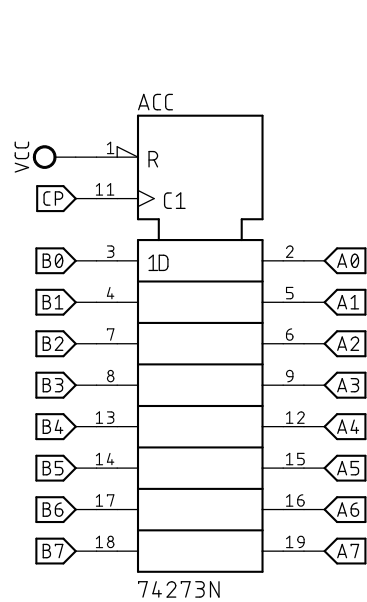
TITLE: PC BUS

Document Number: 3.1

REV: 1

Date: 26. 12. 2021 12:27

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ACC with output to BUS and to ALU

TITLE: ACC

Document Number:

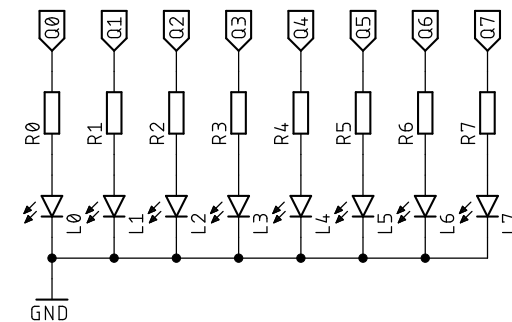
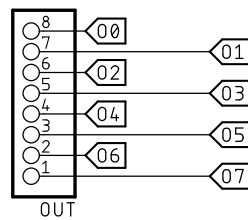
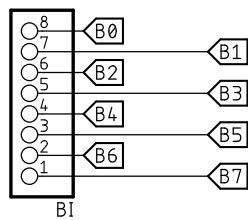
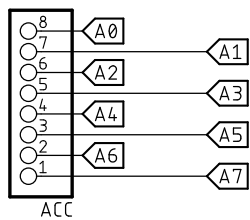
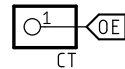
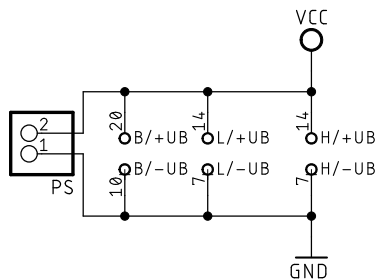
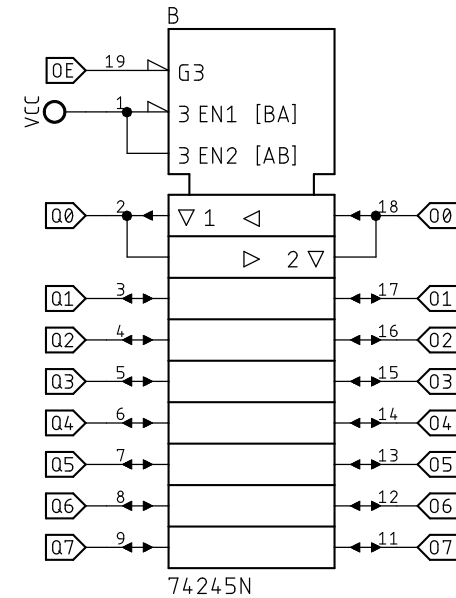
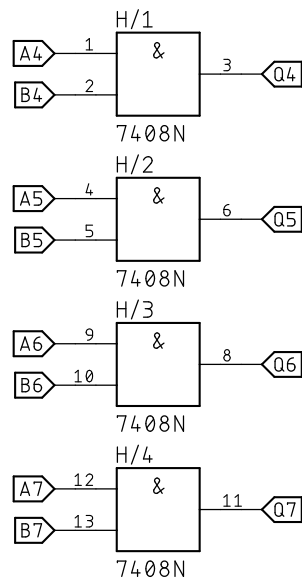
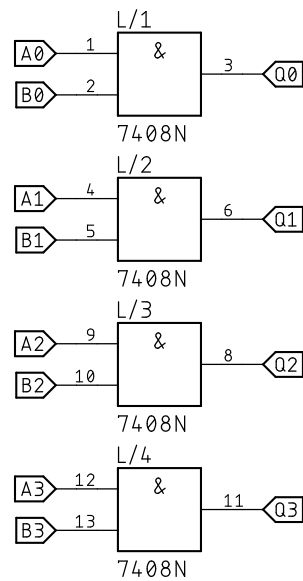
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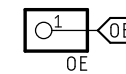
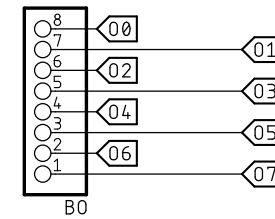
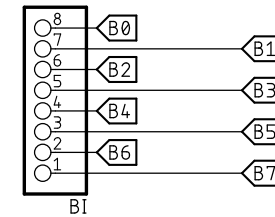
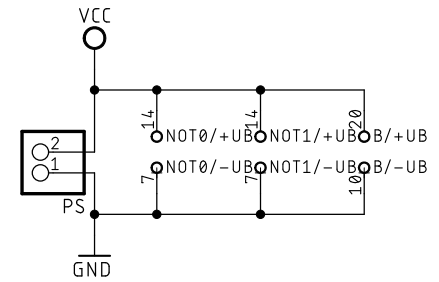
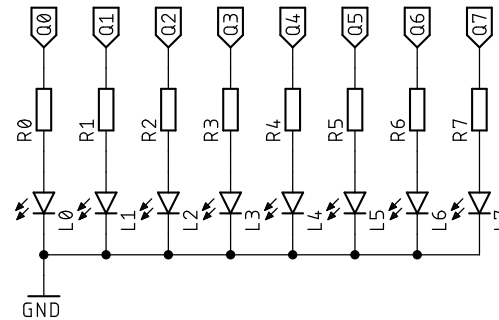
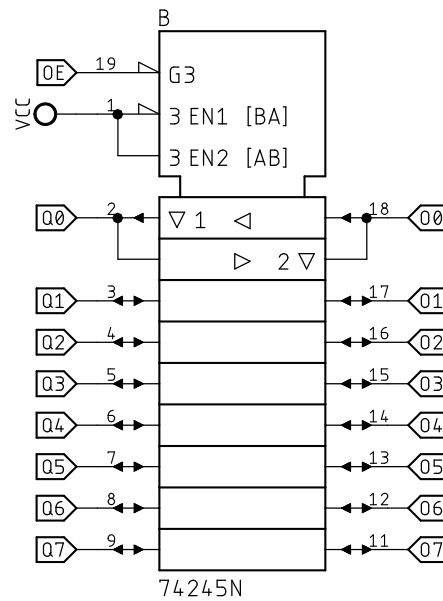
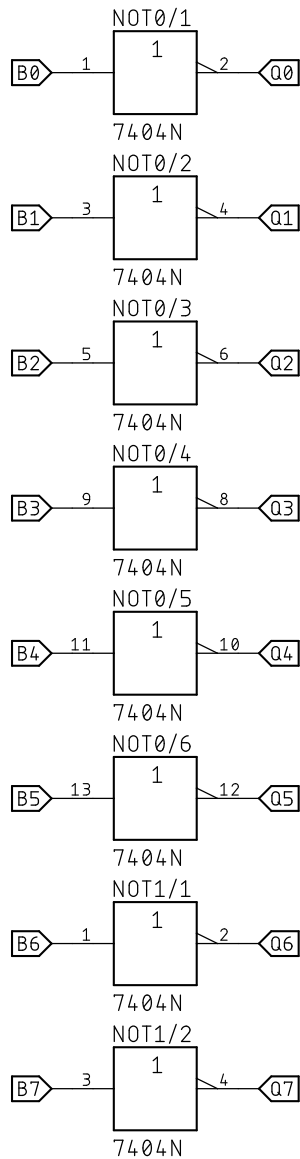
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Date: 4. 1. 2022 16:24

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Template for logic modules		
TITLE: Logic		
Document Number: 4.1		REV: 1
Date: not saved!		Sheet: 1/1



NOT logic module

TITLE: NOT

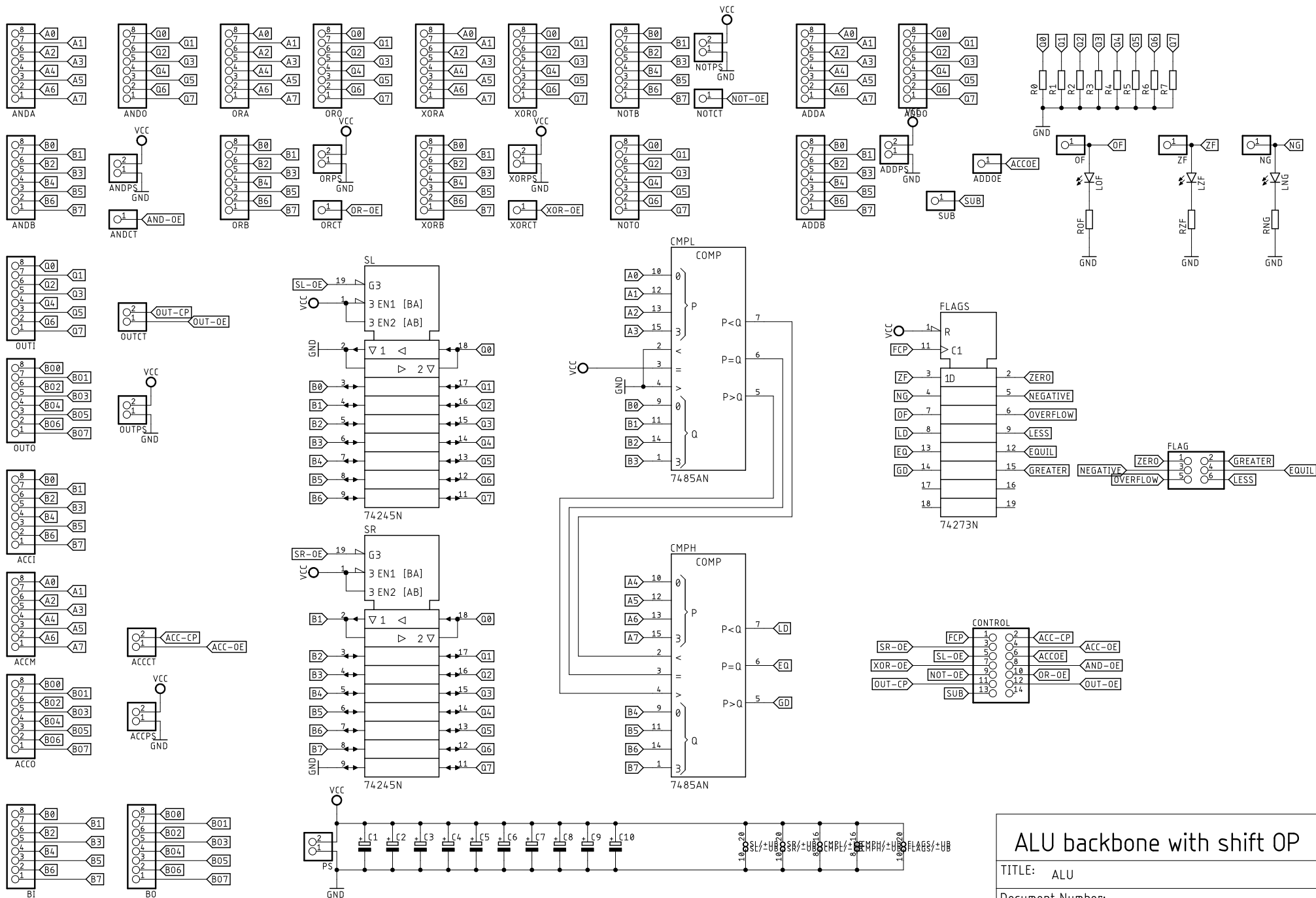
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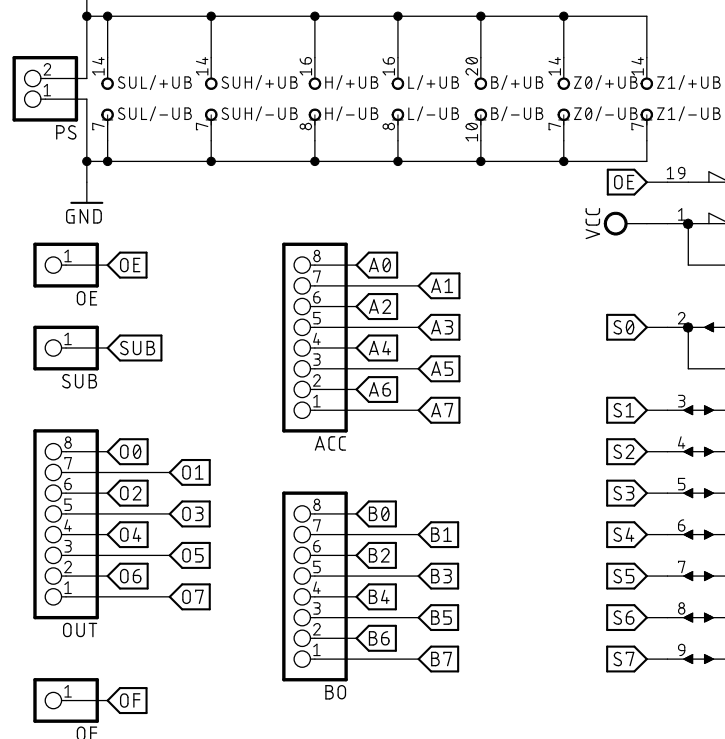
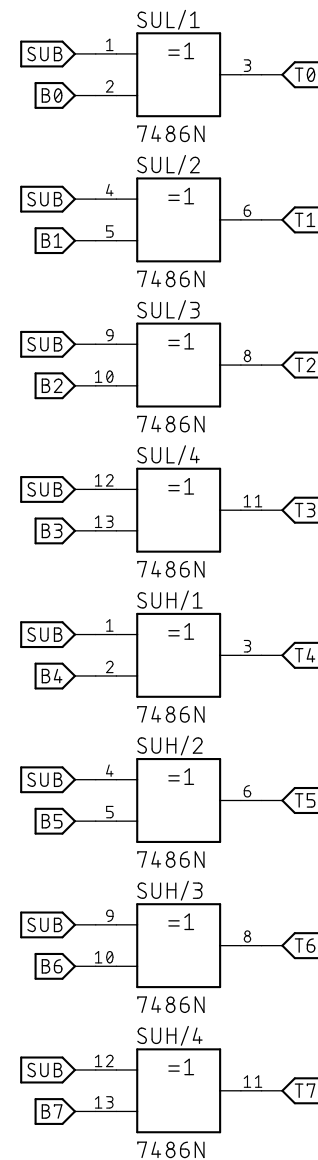
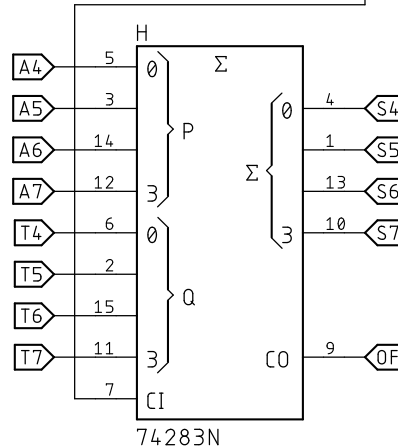
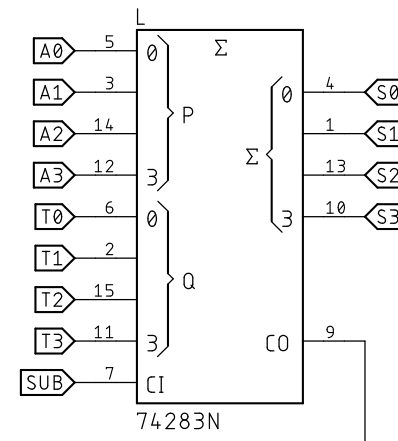
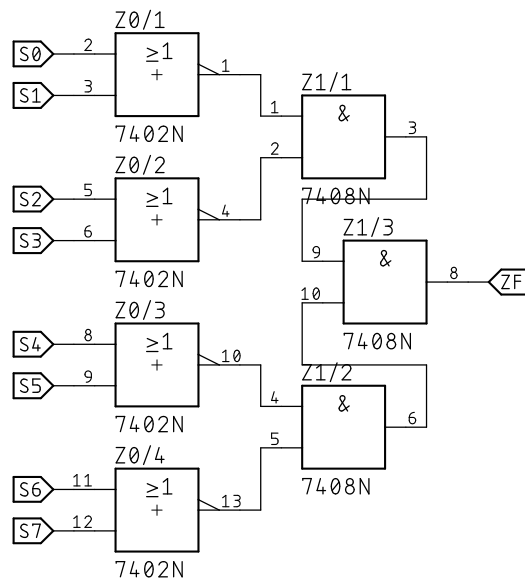
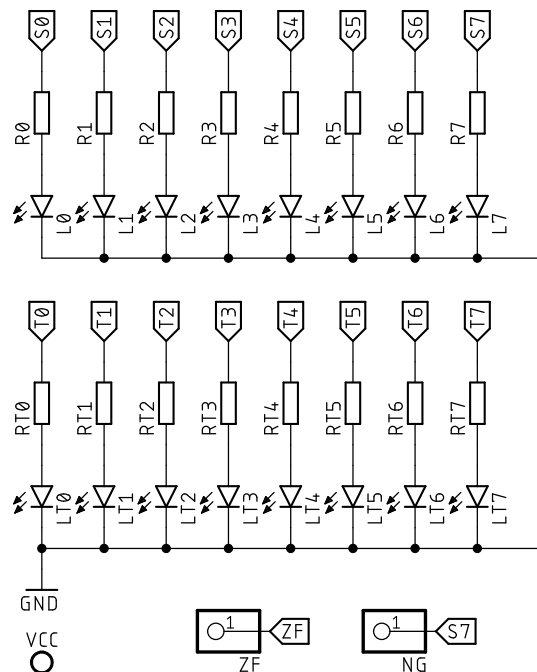
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REV:
1

Date: not saved!

Sheet: 1/1





ADD and SUB

TITLE: ADDER

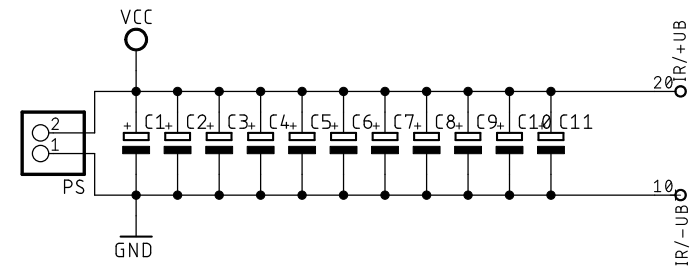
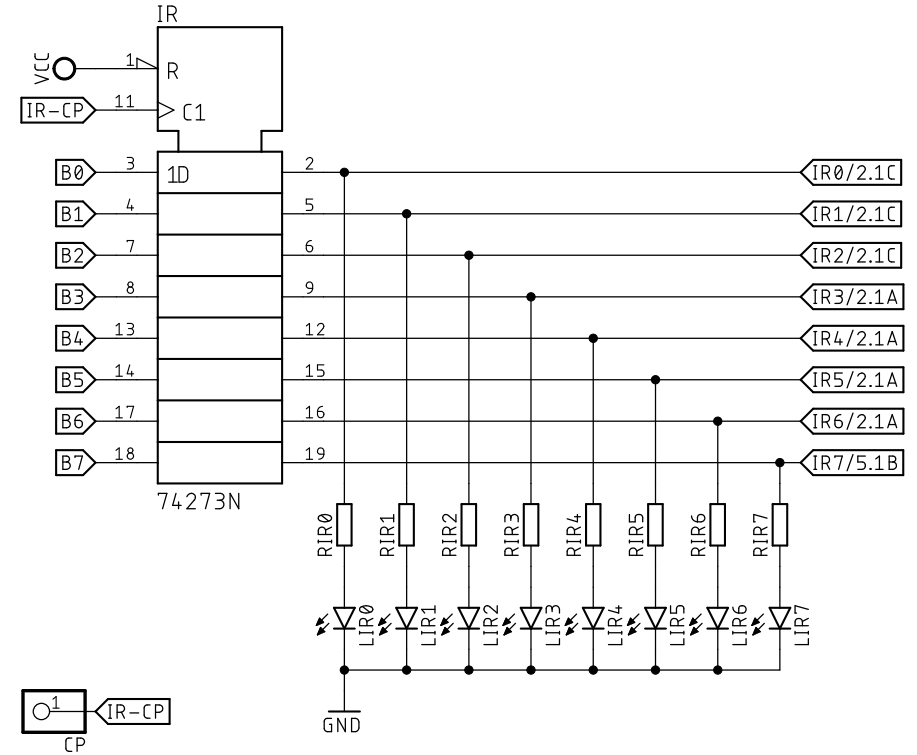
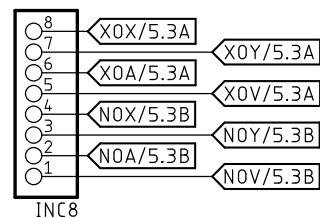
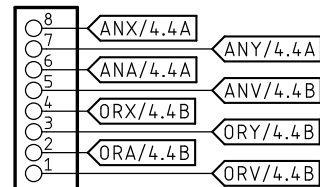
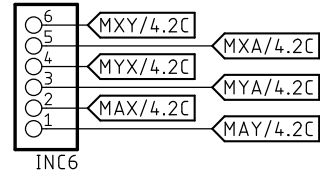
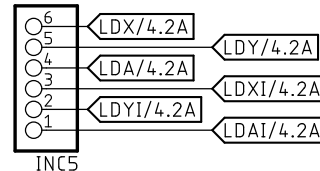
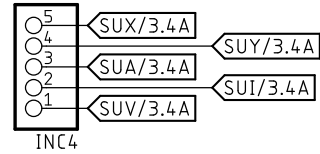
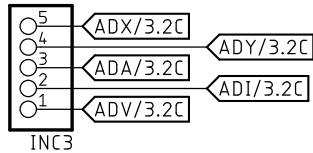
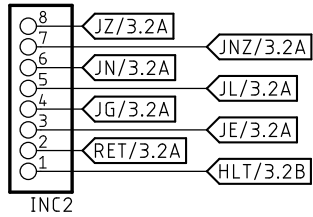
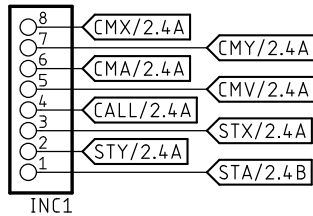
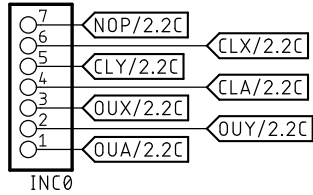
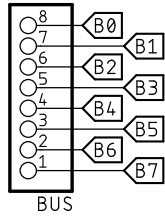
Document Number:

4.4

REV: 1

Date: 23. 10. 2021 21:09

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IO pins, PS, IR register

TITLE: Decoder

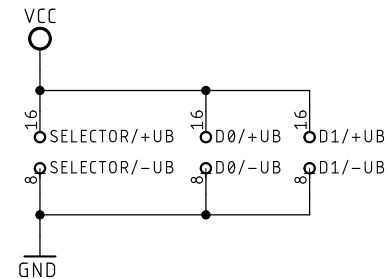
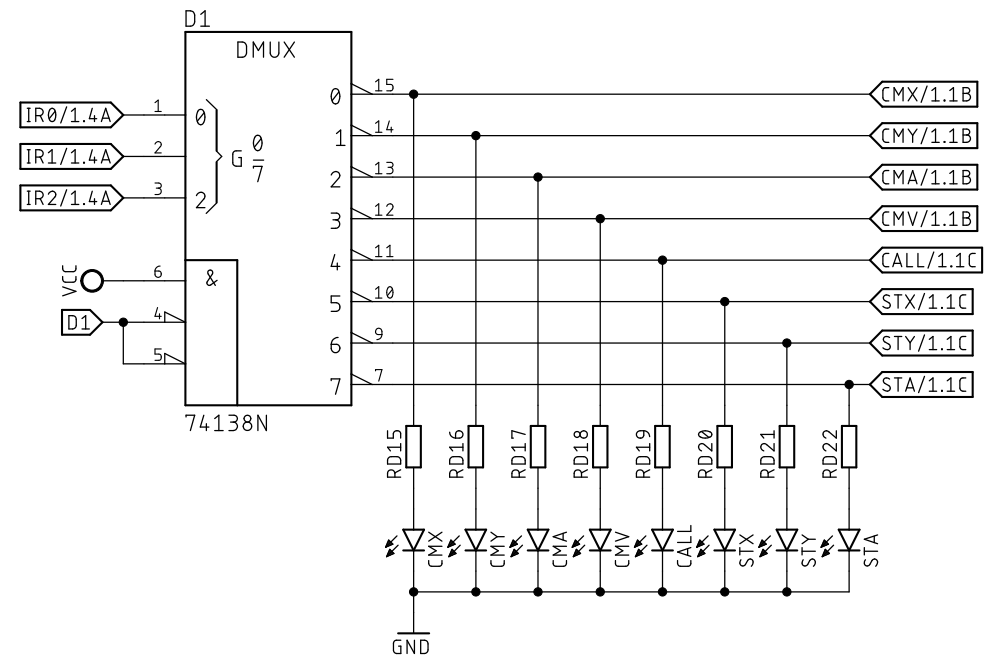
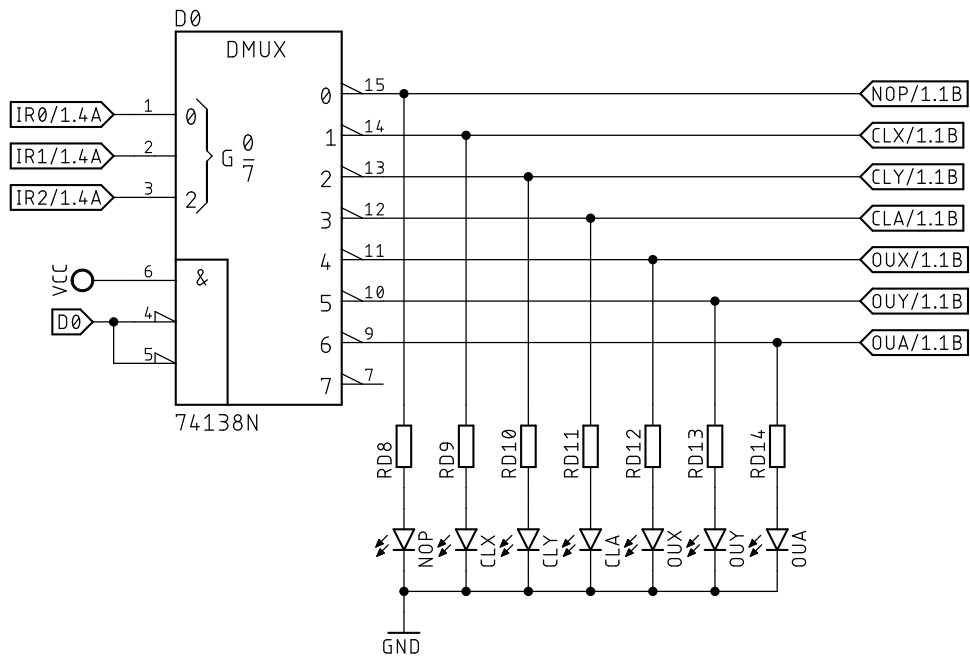
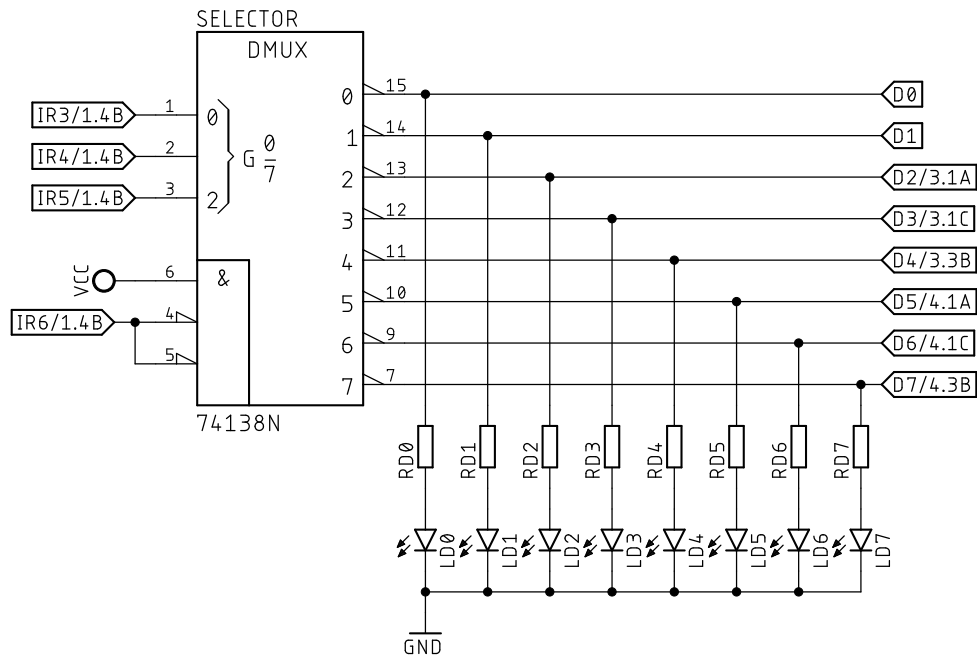
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REV:
1.0

Date: not saved!

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Selector, DEC 0, 1

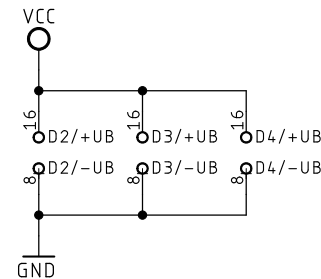
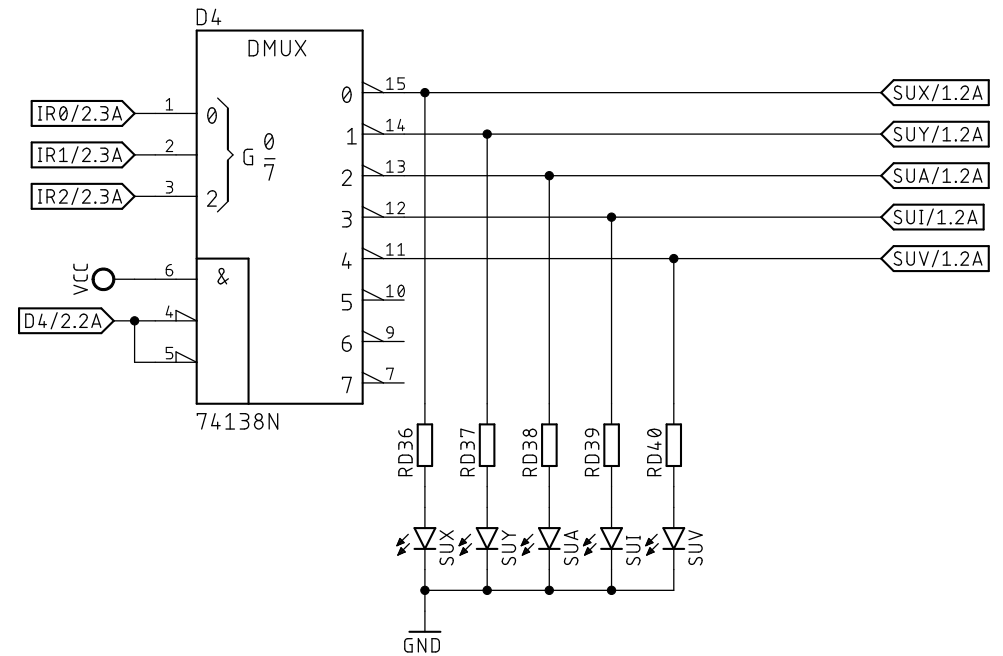
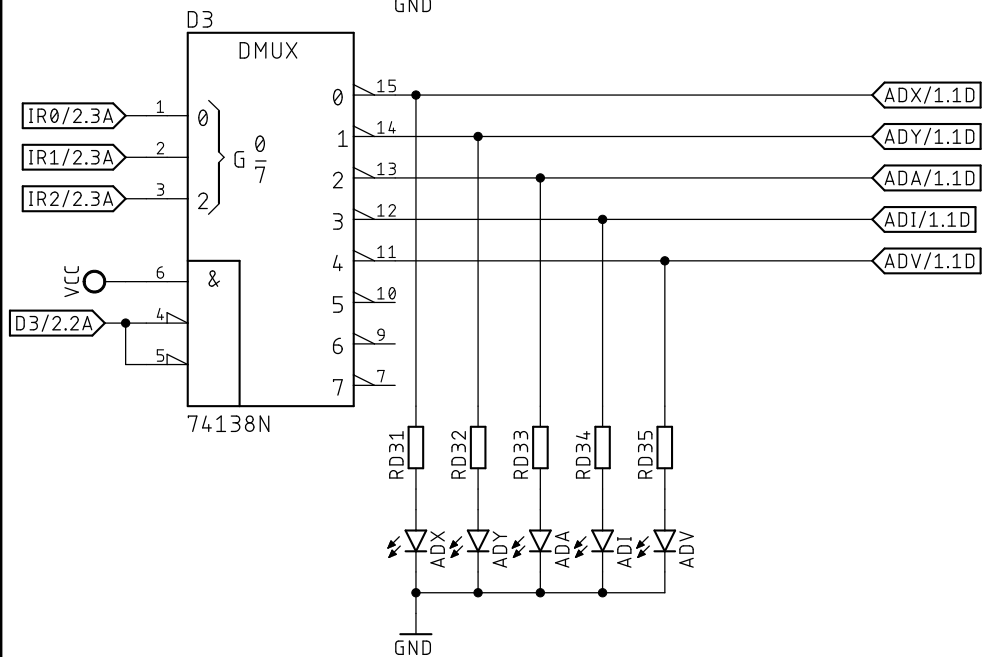
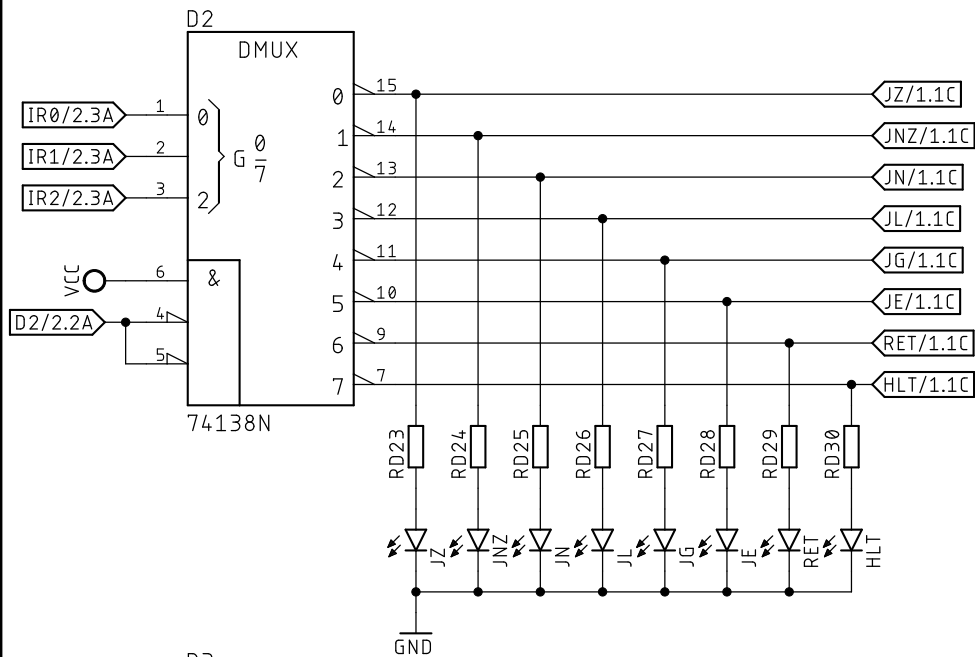
TITLE: Decoder

Document Number: 5.1

REV: 1.0

Date: not saved!

Sheet: 2/5



DEC 2, 3, 4

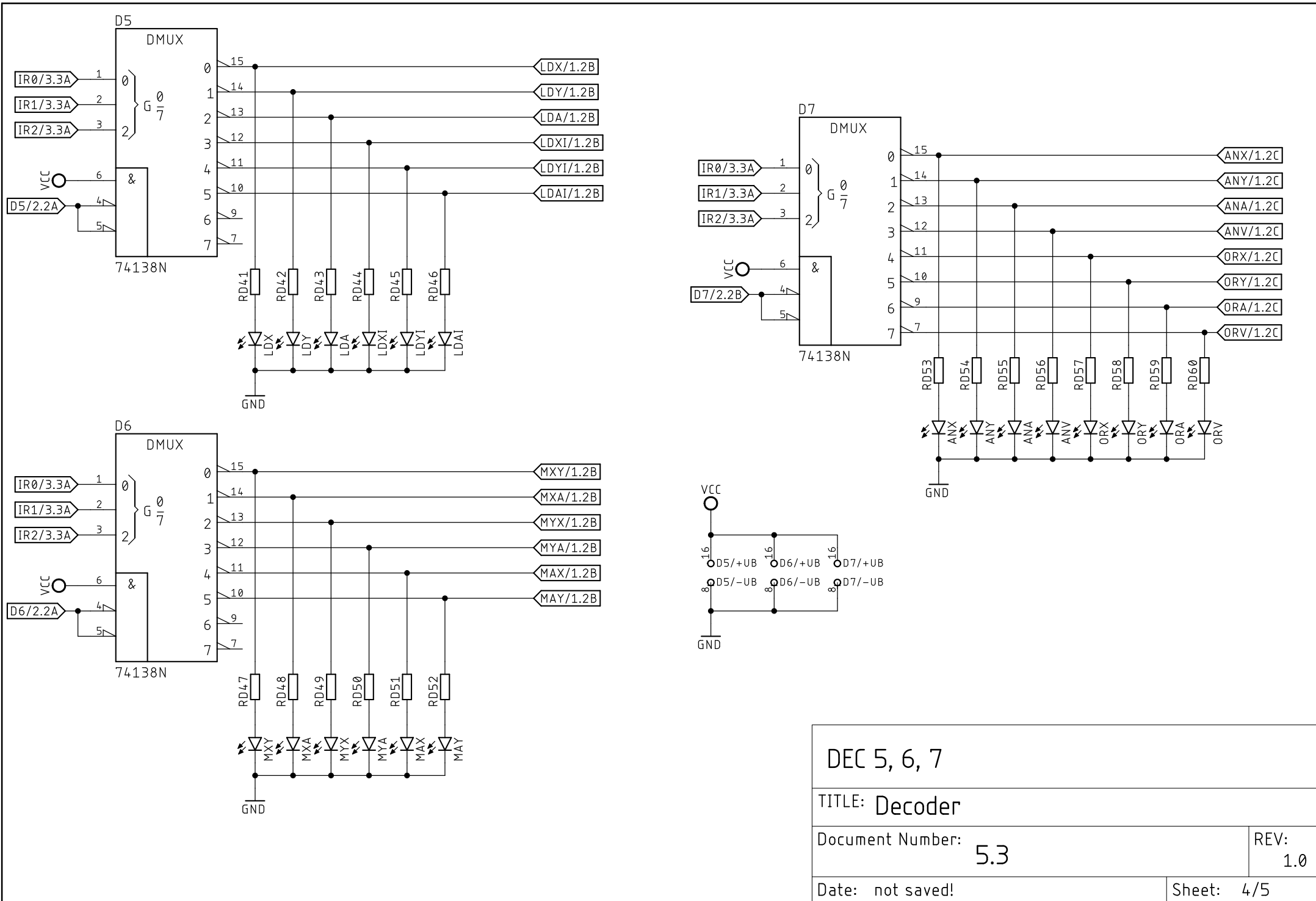
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Document Number: 5.2

REV: 1.0

Date: not saved!

Sheet: 3/5



DEC 5, 6, 7

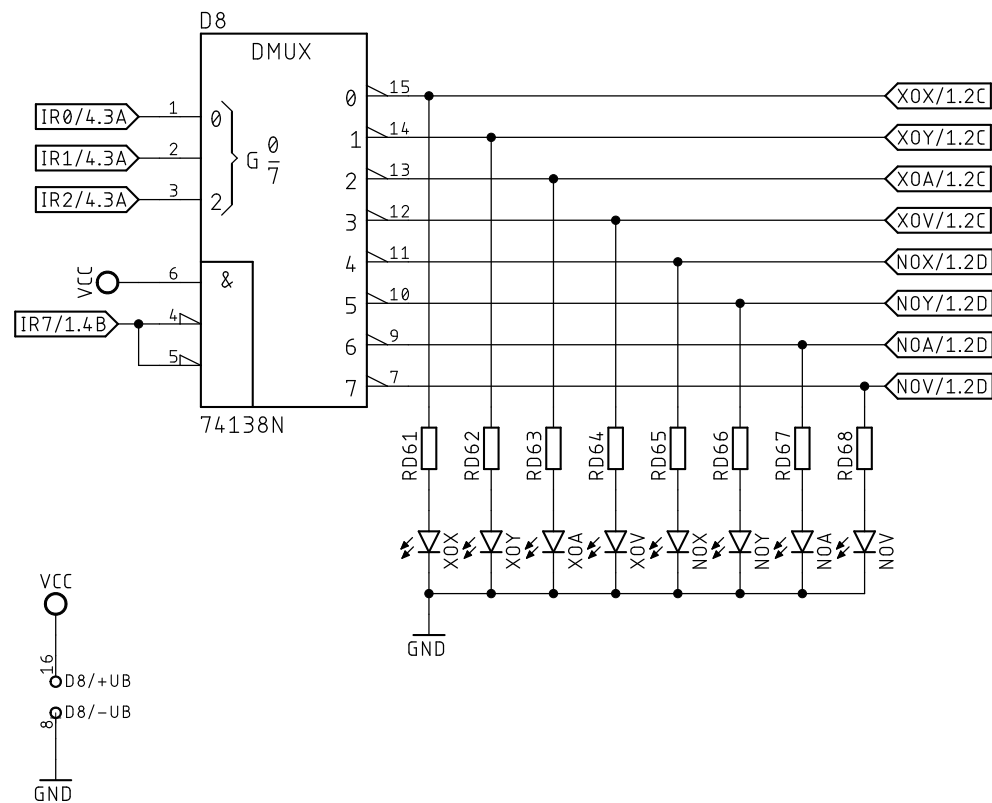
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Document Number: 5.3

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Date: not saved!

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DEC 8

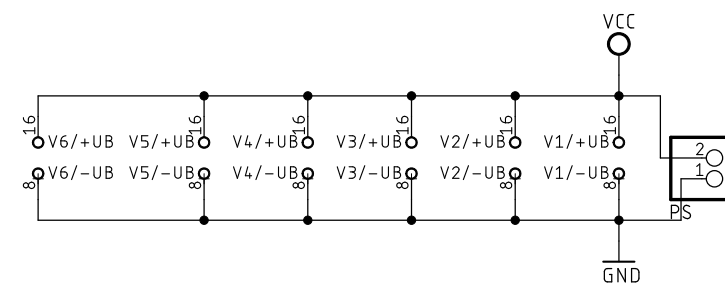
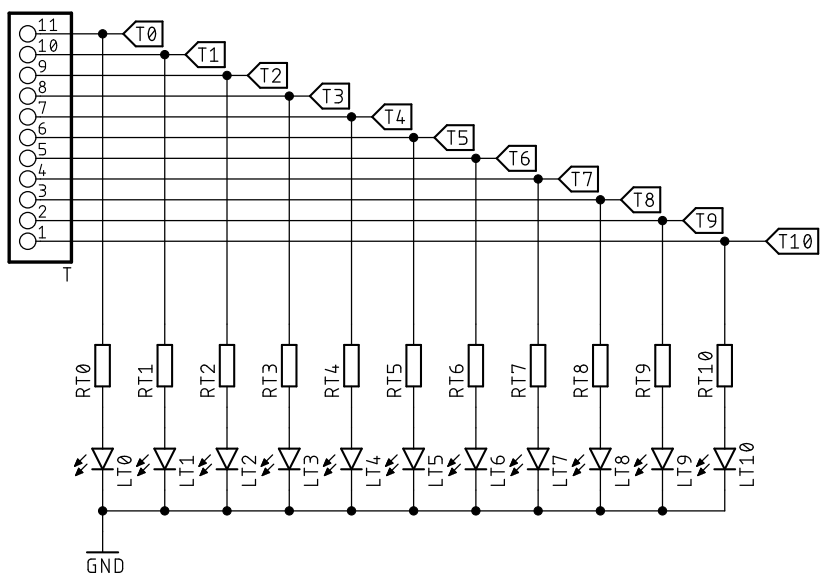
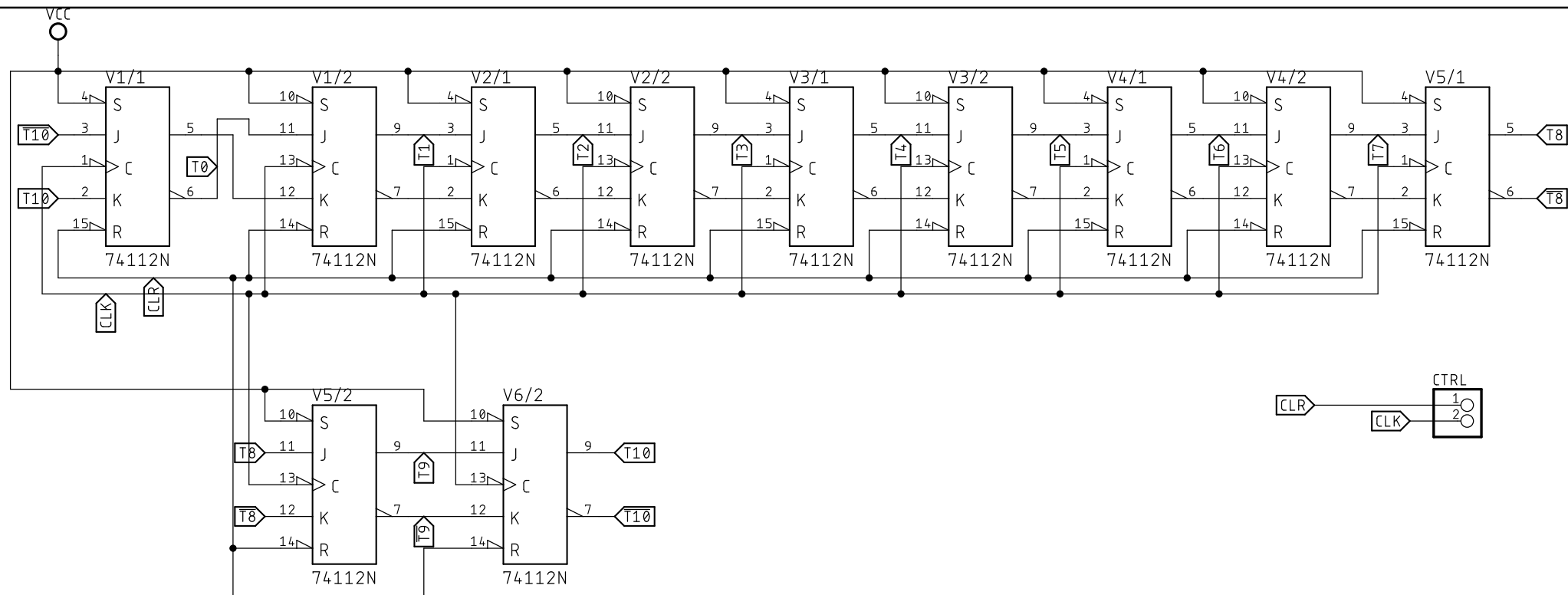
TITLE: Decoder

Document Number: 5.4

REV: 1.0

Date: not saved!

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T-RING counter

TITLE: T-RING

Document Number:

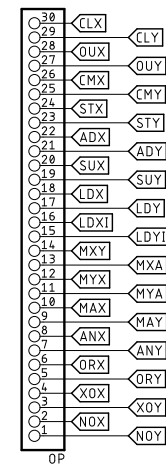
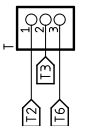
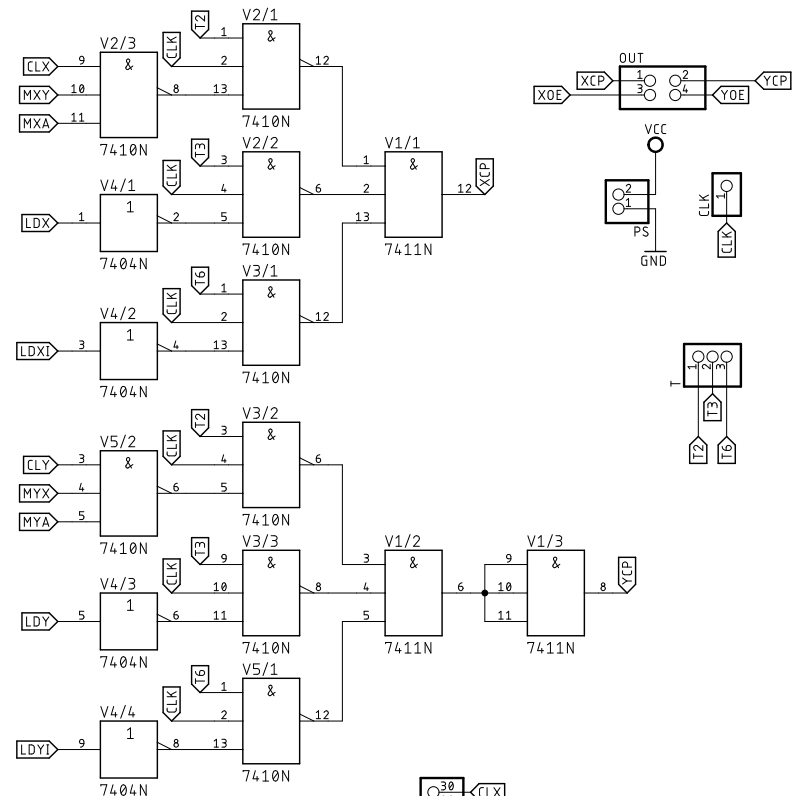
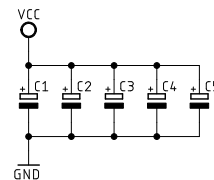
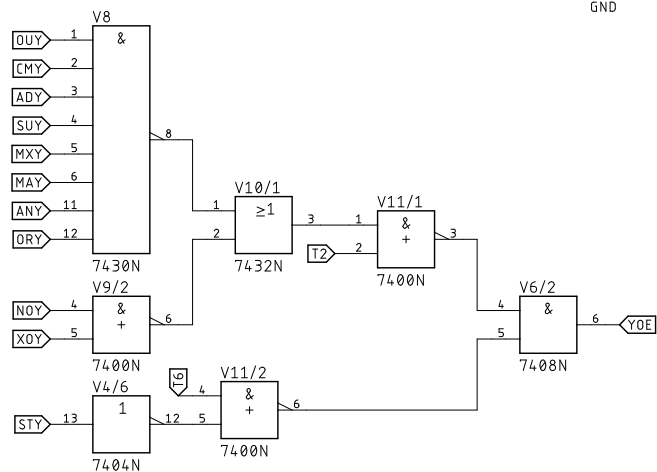
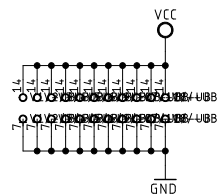
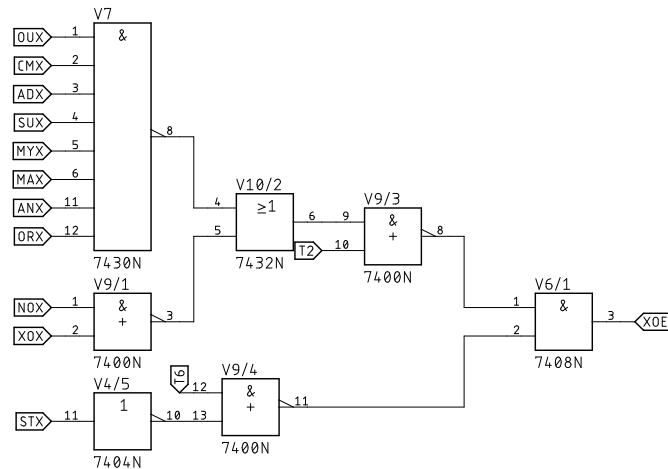
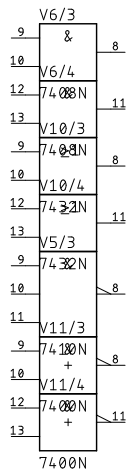
5.5

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1.0

Date: 21. 12. 2021 18:30

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Register control

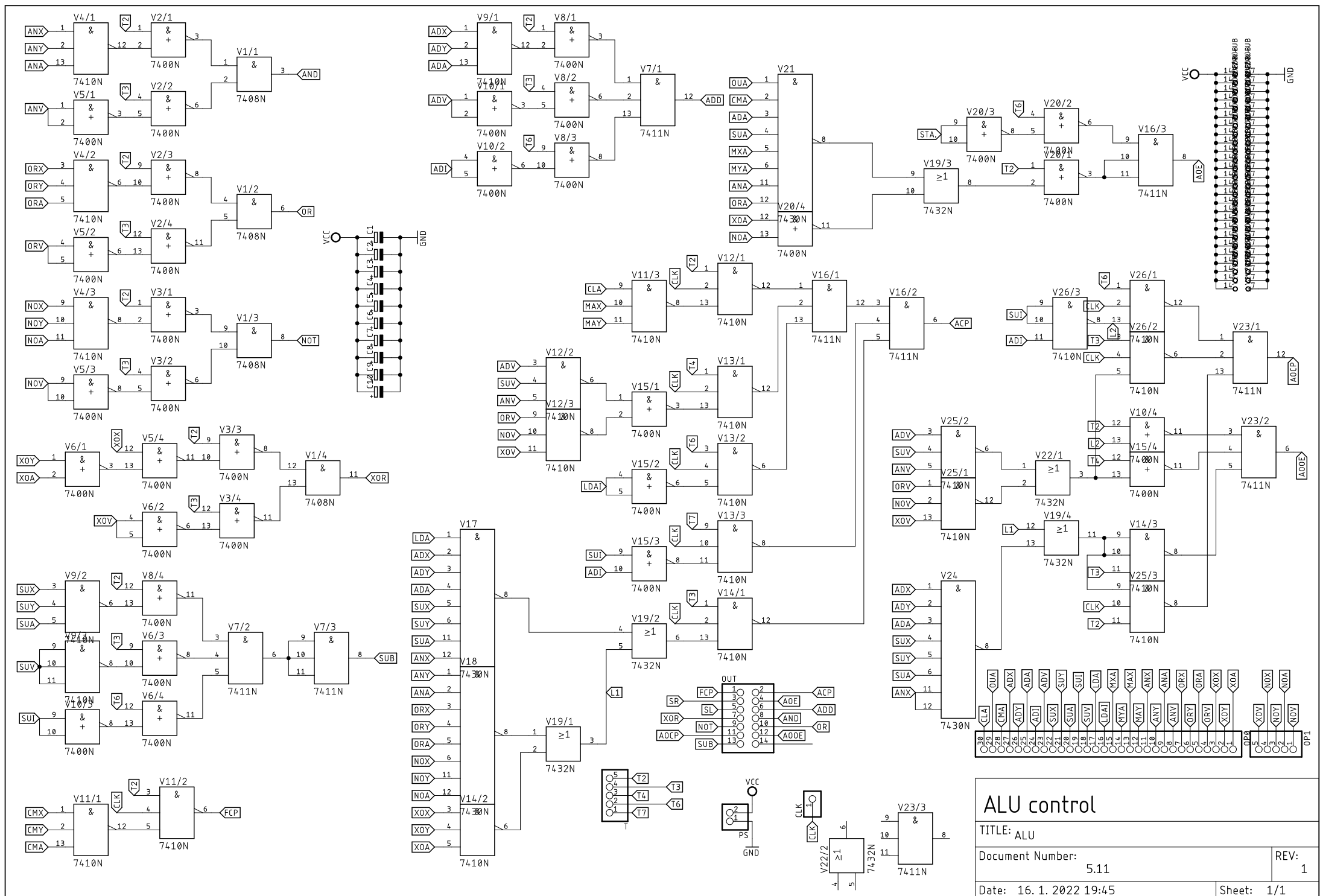
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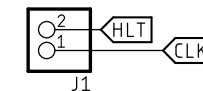
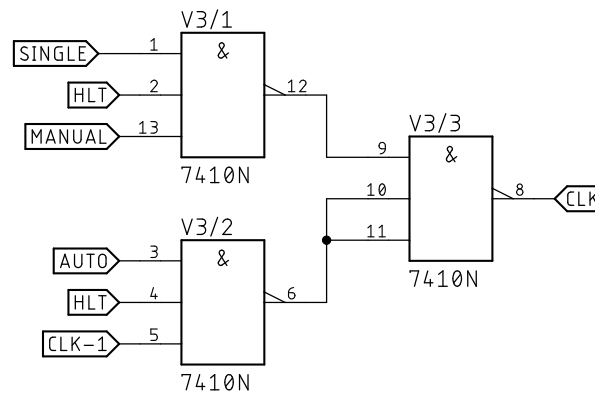
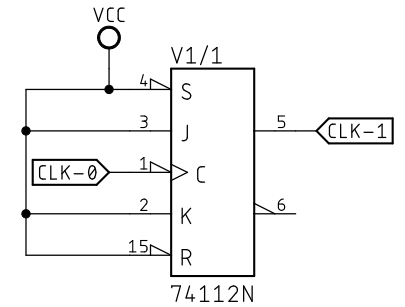
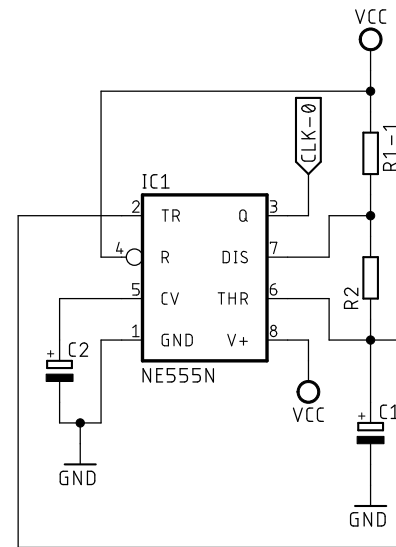
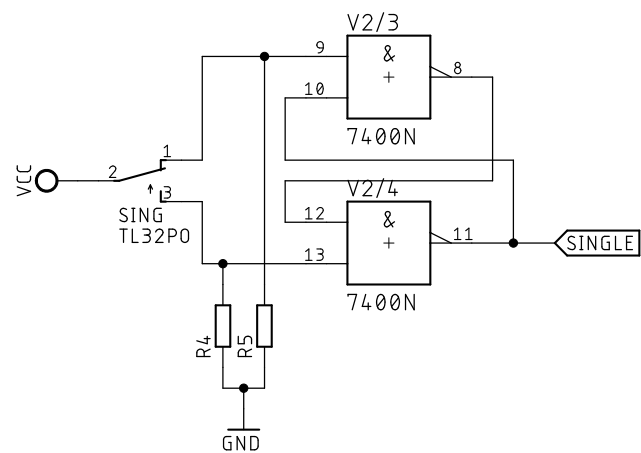
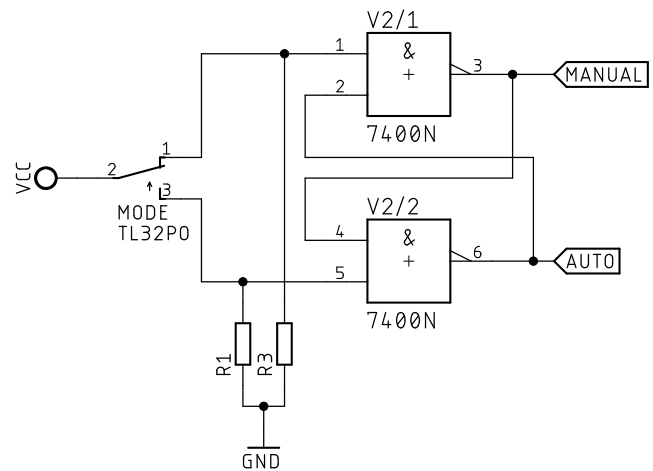
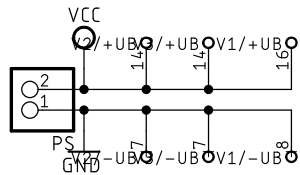
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Date: not saved!

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1kHz clock

TITLE: Clock

Document Number:

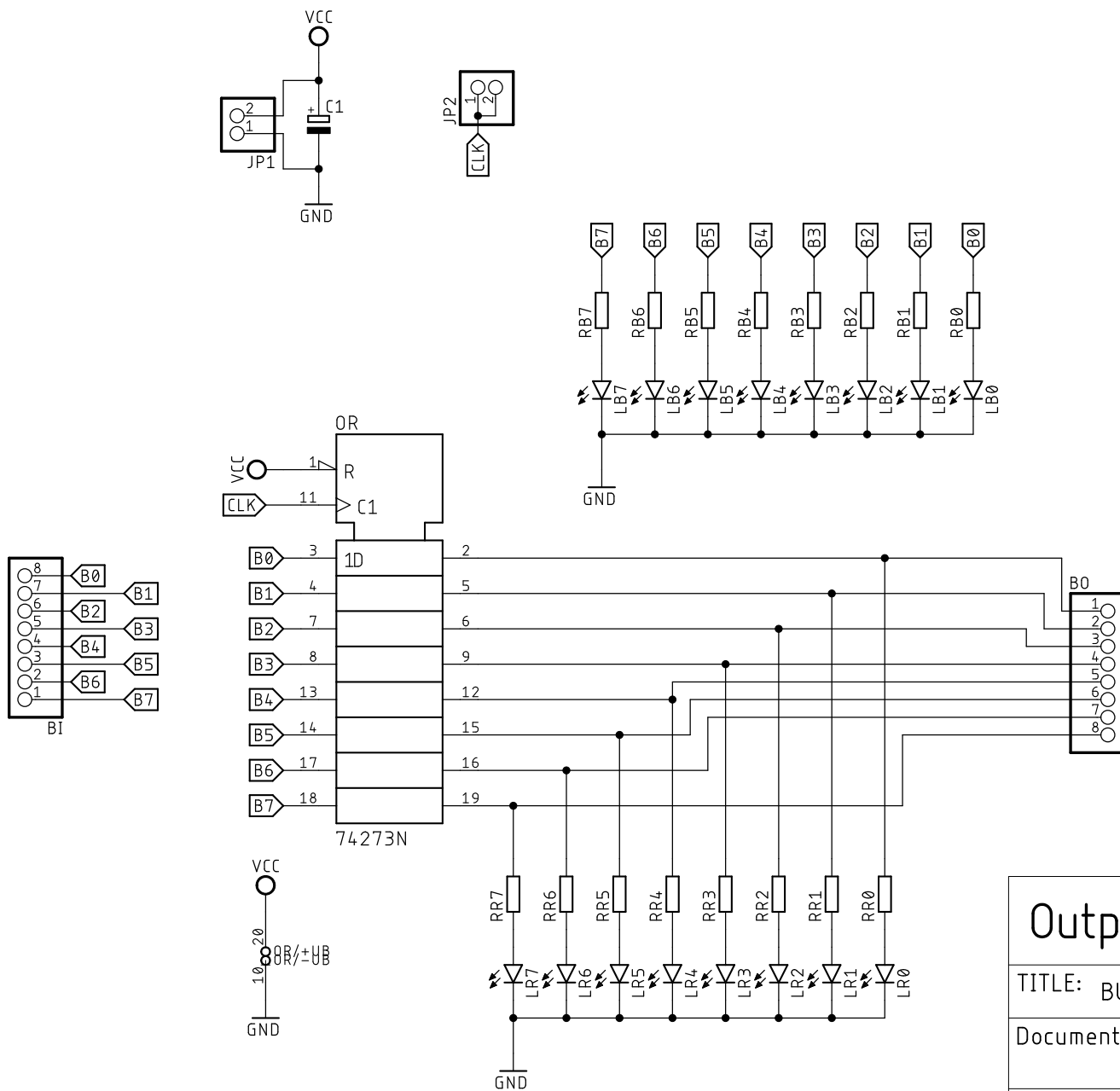
6

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Date: 7. 1. 2022 14:29

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Output register

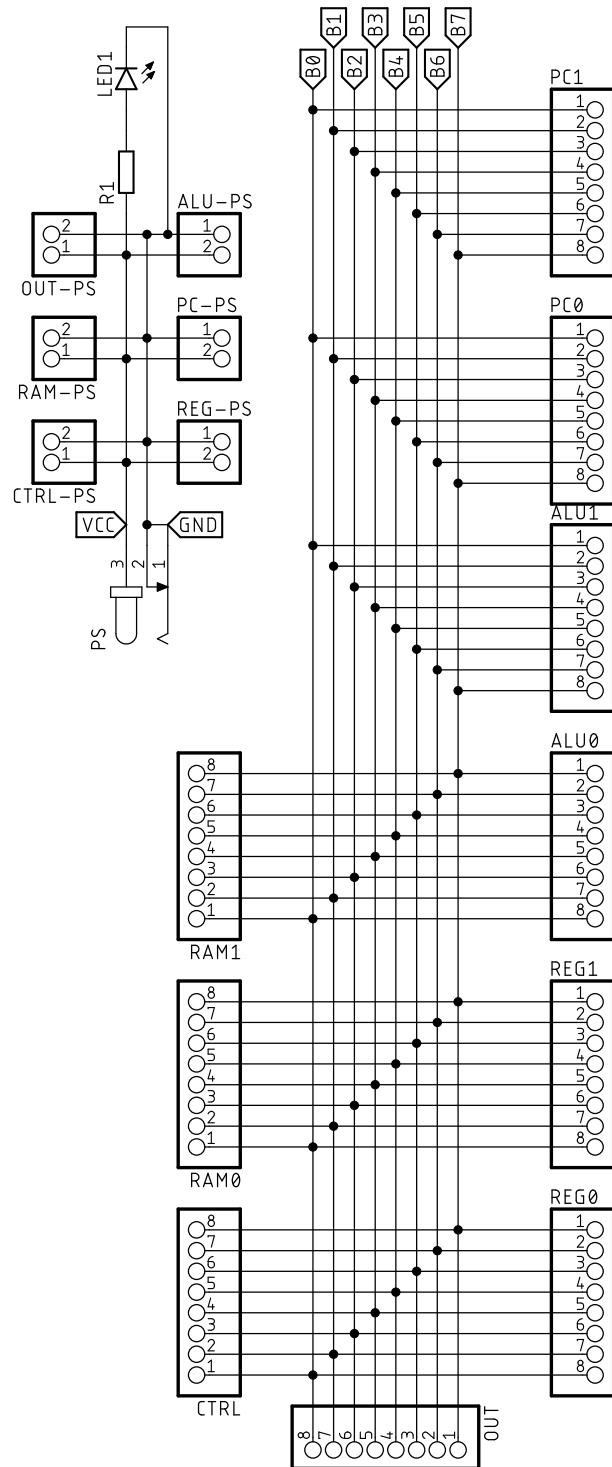
TITLE: BUS_OUT

Document Number: 7

REV: 1

Date: 16. 1. 2022 19:31

Sheet: 1/1



Main bus

TITLE: BUS

Document Number: 7.1

REV: 1

Date: 16. 1. 2022 19:35

Sheet: 1/1