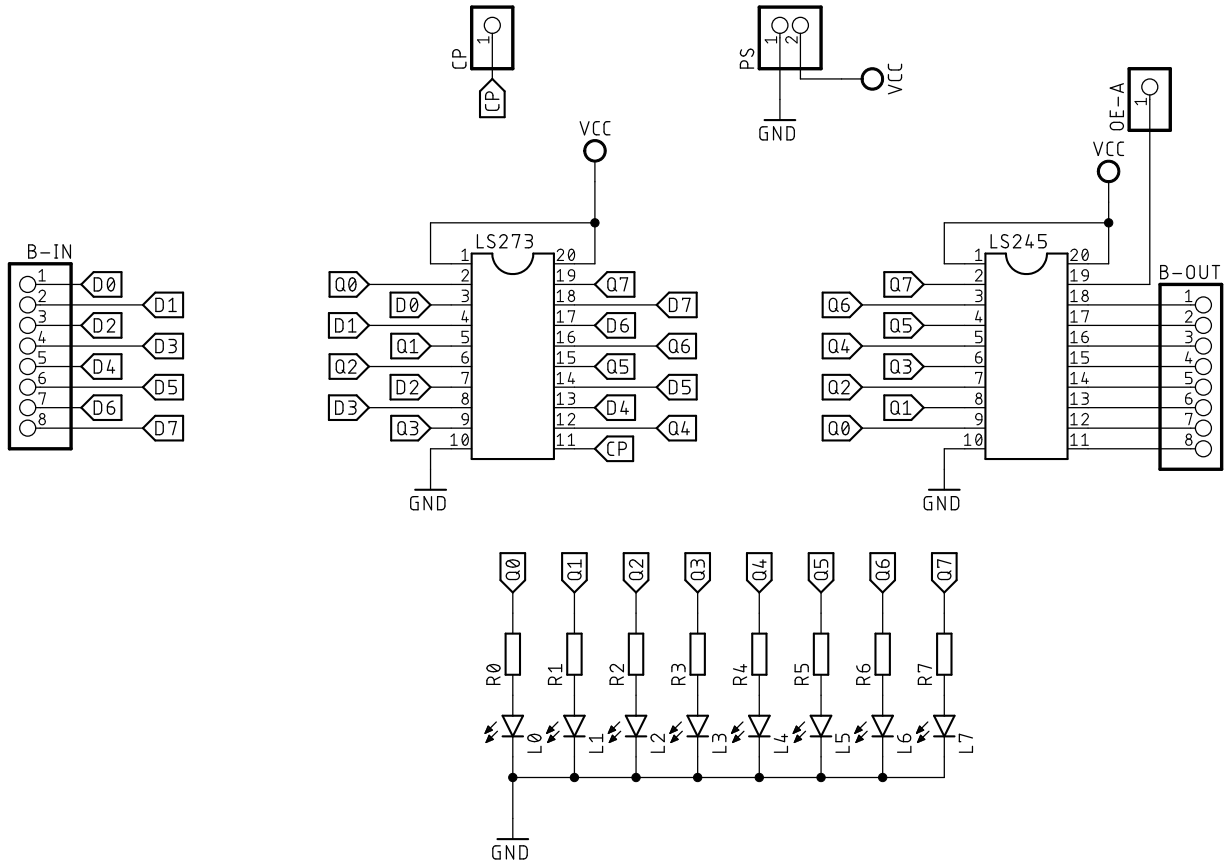
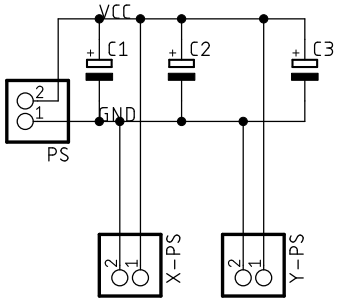
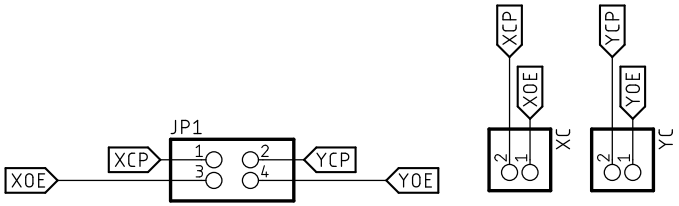
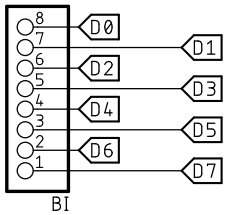


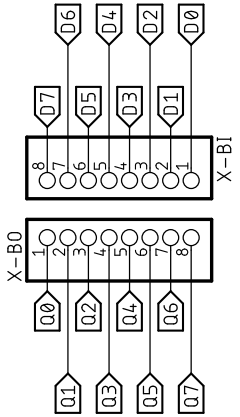
8bit Register with leds.

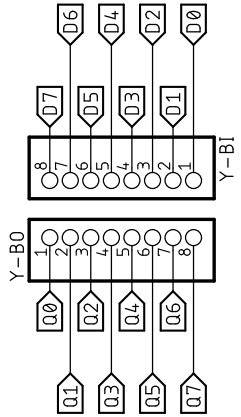
TITLE: Register		
Document Number: 1		REV: 1.1
Date: 29. 10. 2021 20:25	Sheet: 1/1	

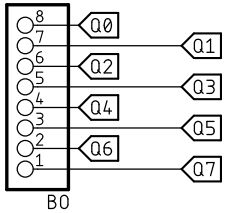






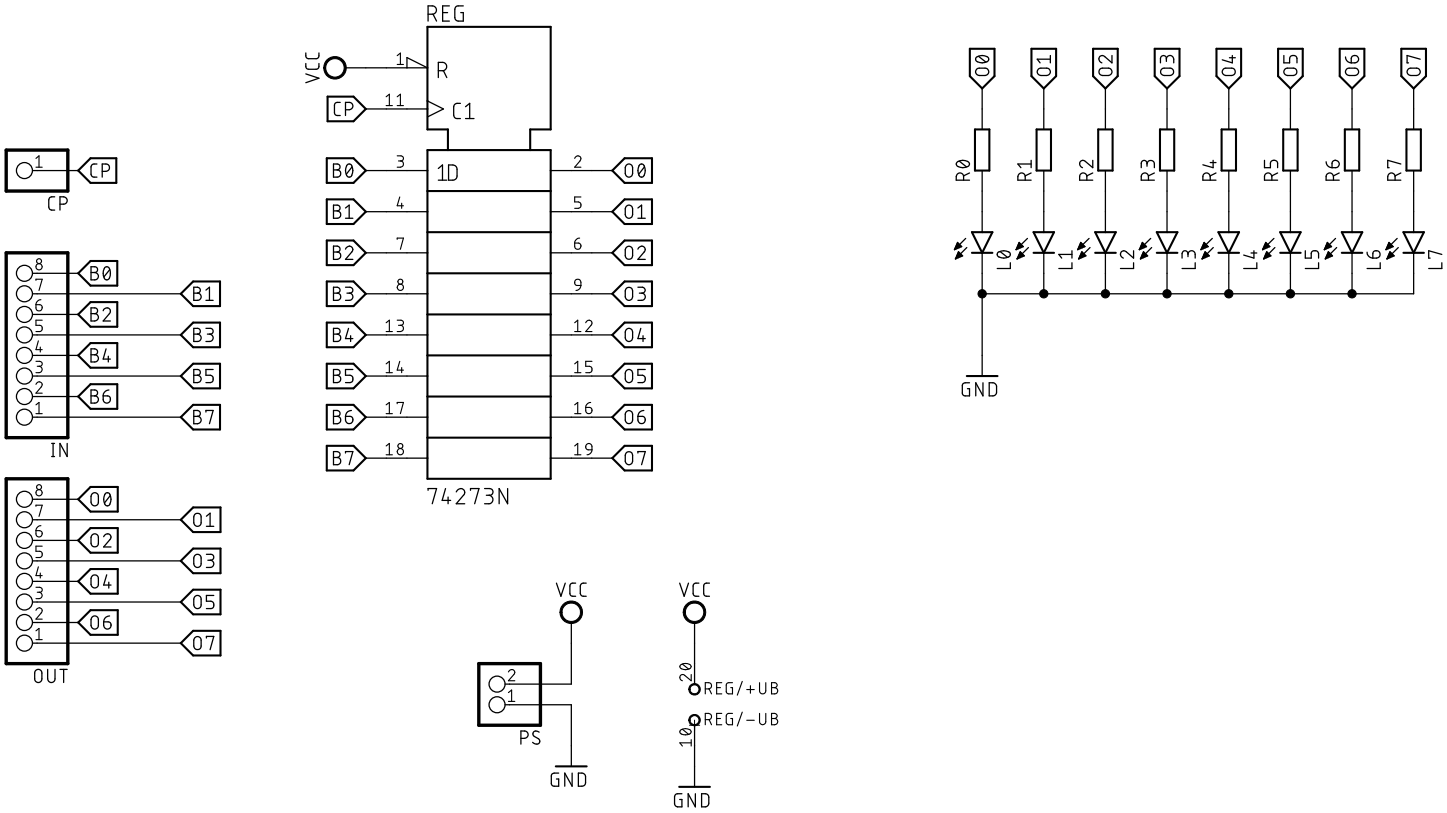






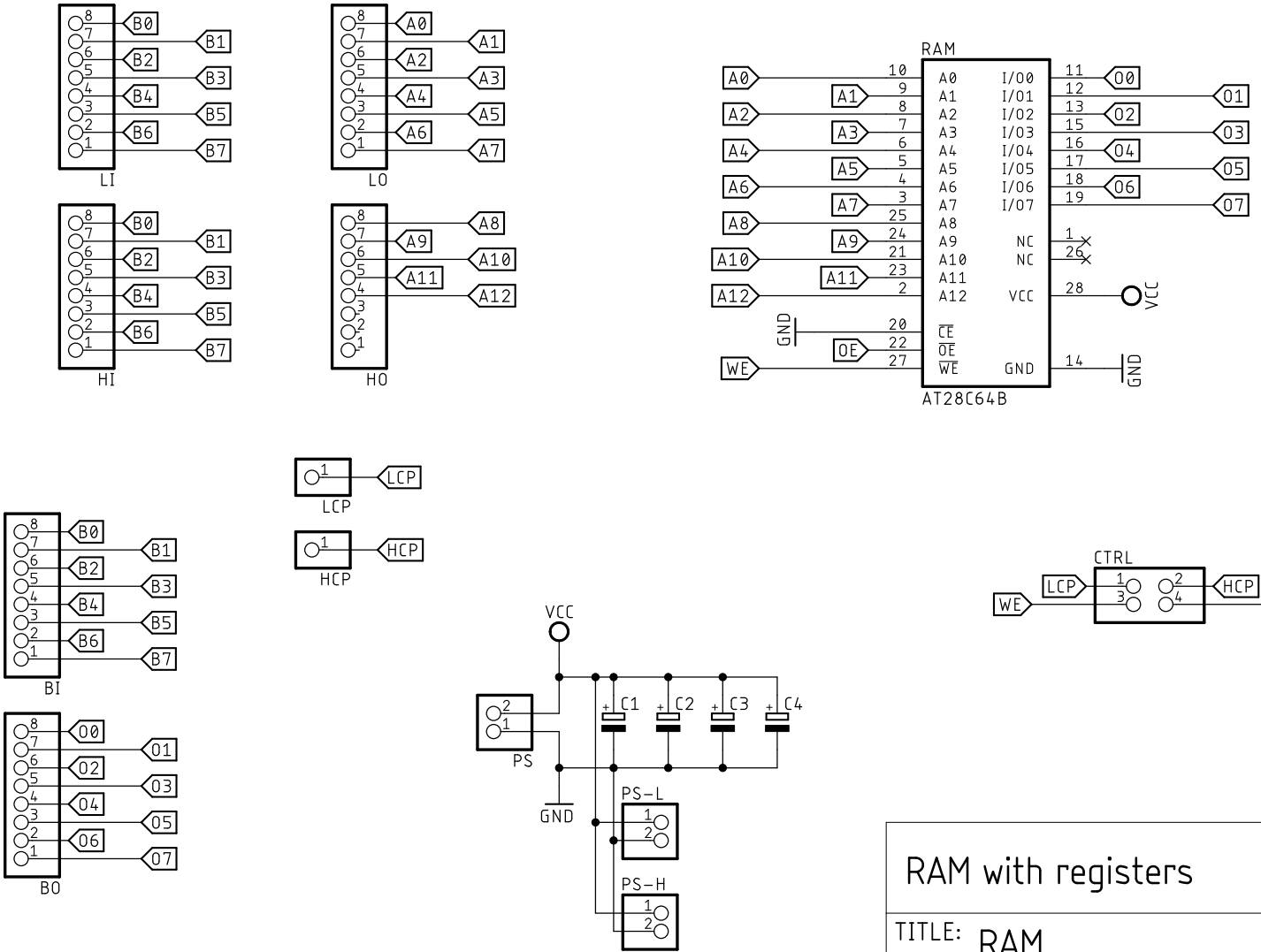
Connection form bus to Registers modules.

TITLE: Register–Bus		
Document Number: 1.1		REV: 1
Date: 16. 10. 2021 17:17	Sheet: 1/1	

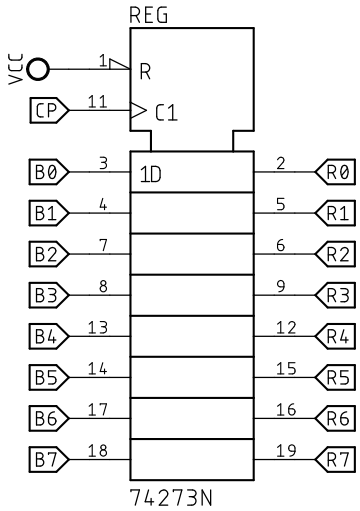


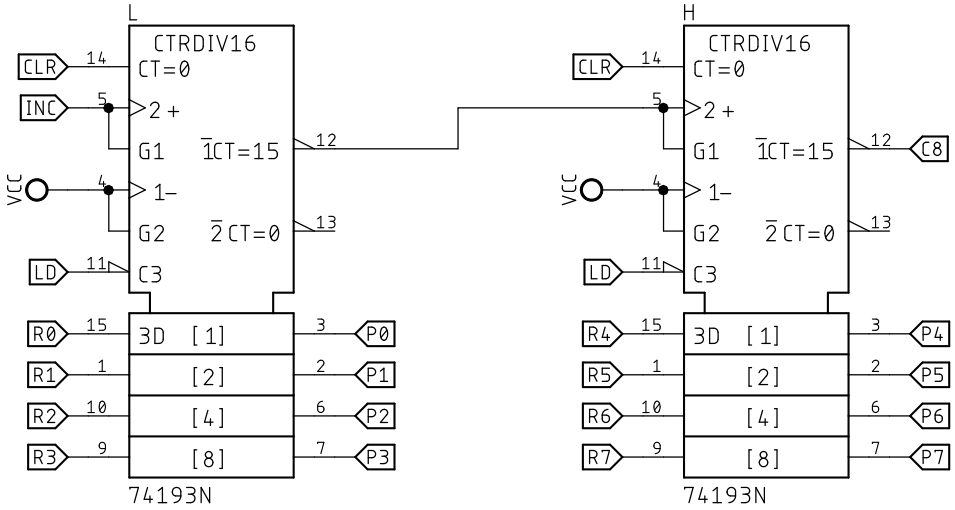
RAM register hold half of RAM ADDR

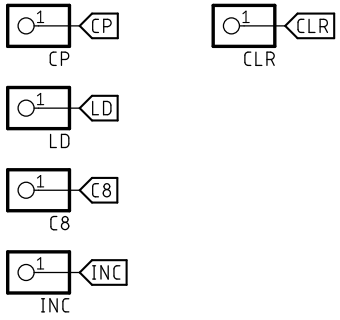
TITLE: RAM register		
Document Number: 2		REV: 1
Date: 29. 10. 2021 21:44	Sheet: 1/1	

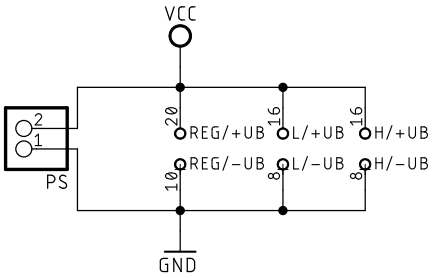


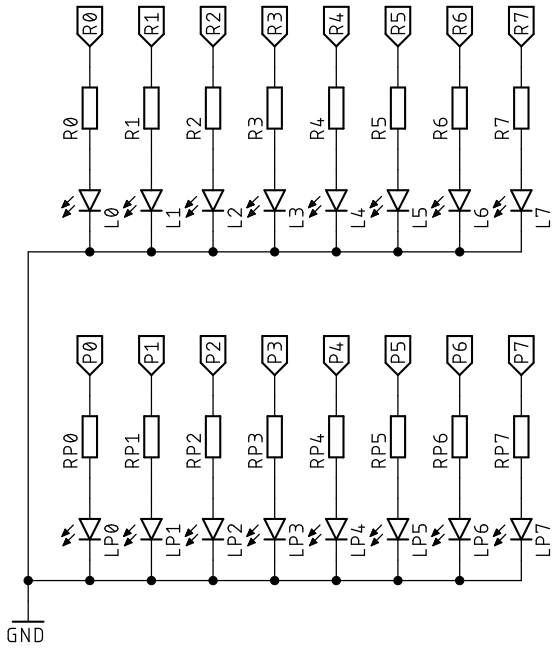
RAM with registers		
TITLE: RAM		
Document Number: 2.1		REV: 1
Date: 29. 10. 2021 22:27	Sheet: 1/1	

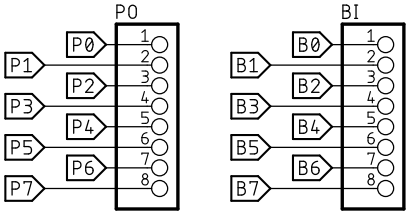






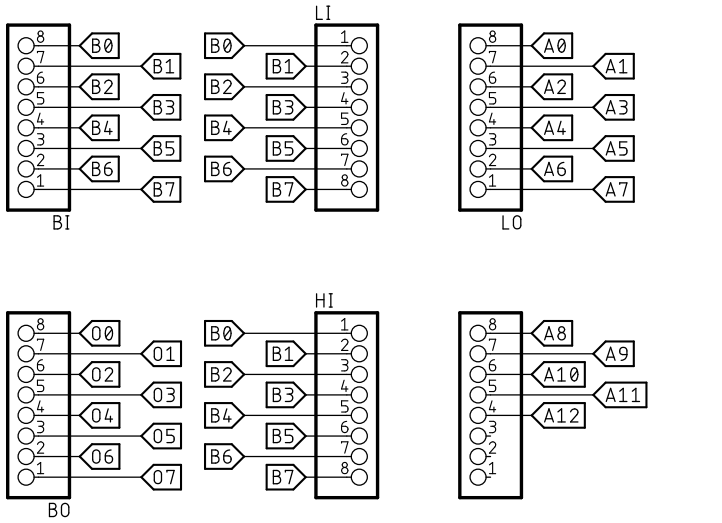


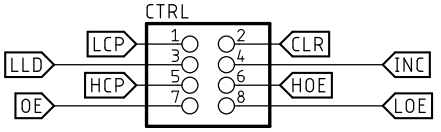


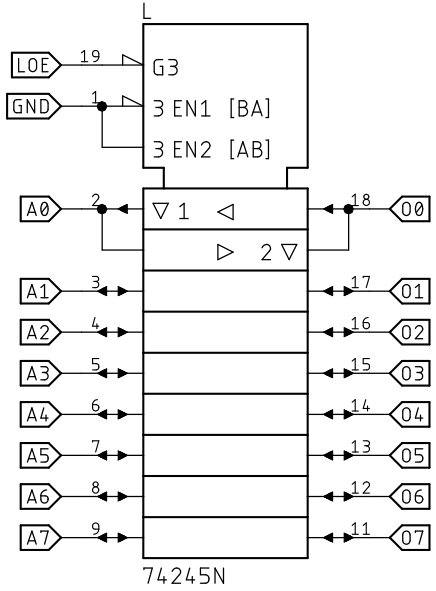


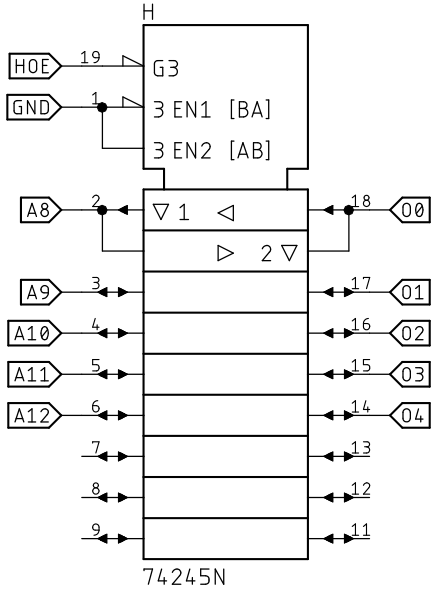
Counter with register and LED

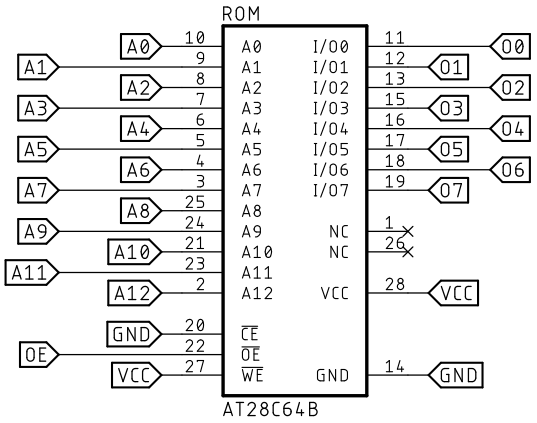
TITLE: Program Counter		
Document Number: 3		REV: 1.1
Date: 16. 10. 2021 22:15	Sheet: 1/1	

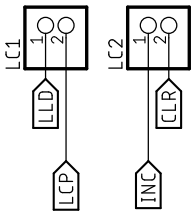


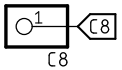


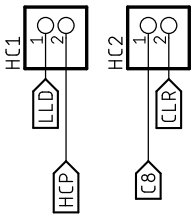


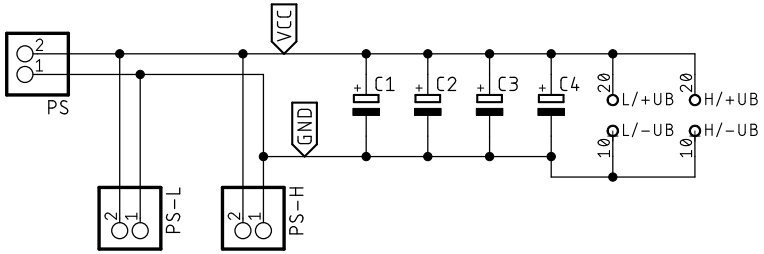






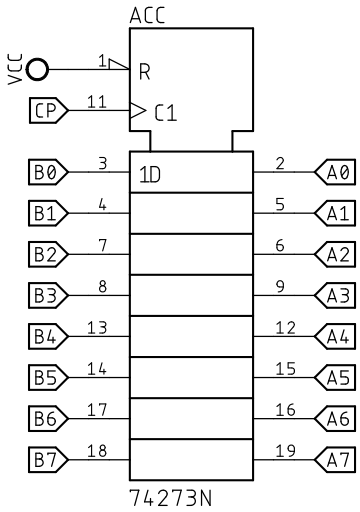


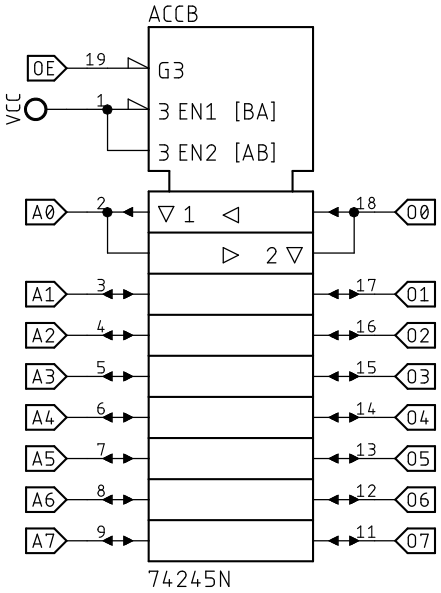


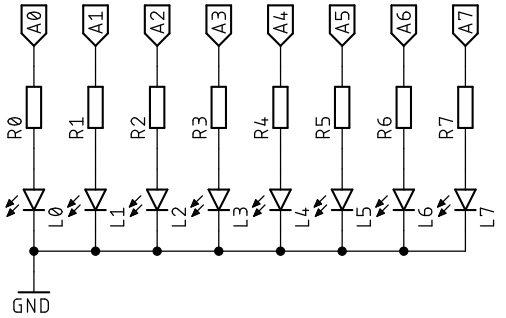


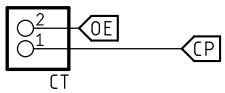
PC and RAM

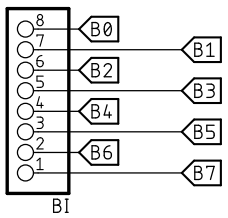
TITLE: PC BUS		
Document Number: 3.1		REV: 1
Date: 29. 10. 2021 20:54	Sheet: 1/1	

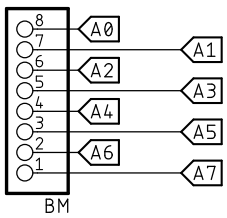


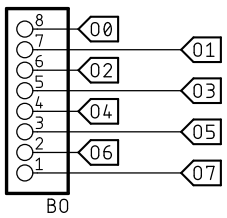


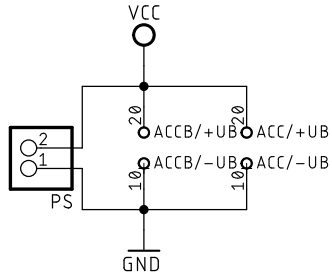






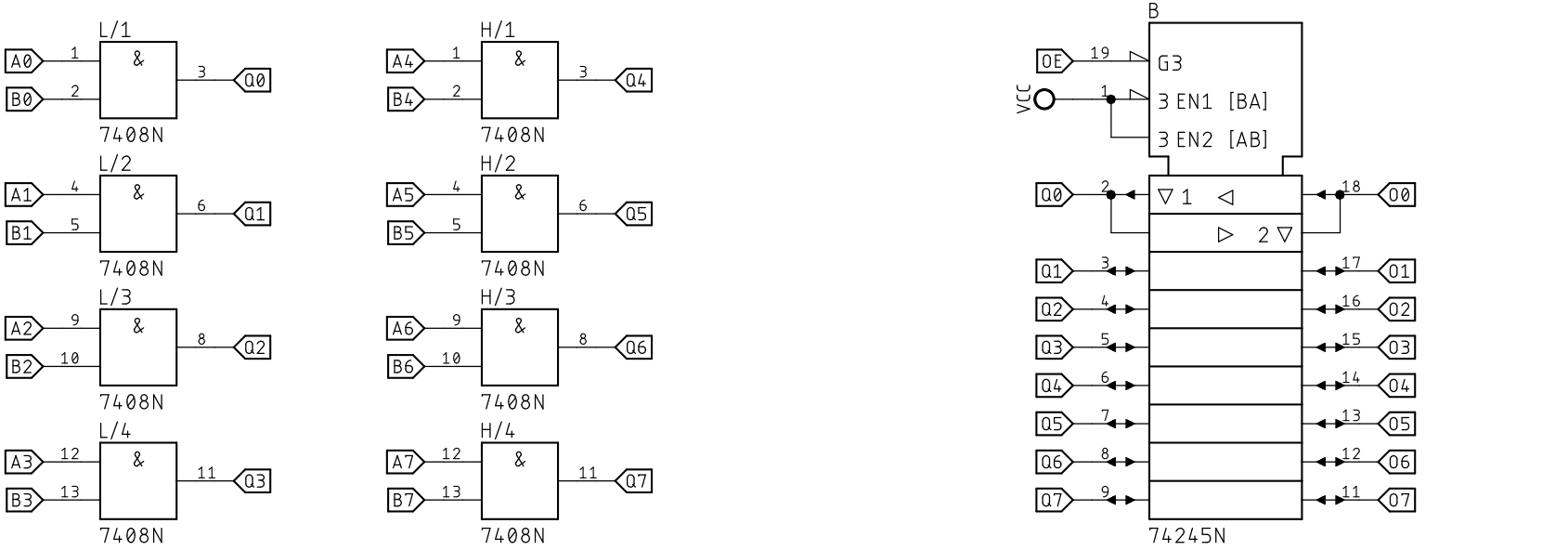


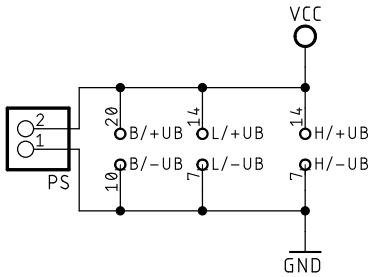


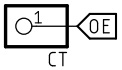


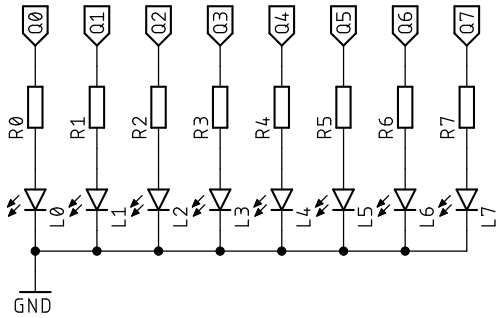
ACC with output to BUS and to ALU

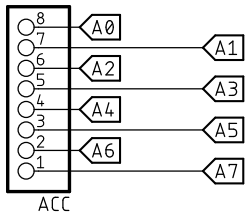
TITLE: ACC		
Document Number: 4		REV: 1
Date: 23. 10. 2021 21:09	Sheet: 1/1	

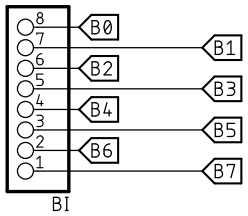


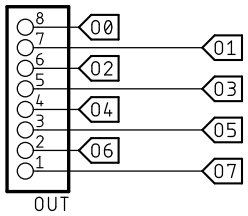






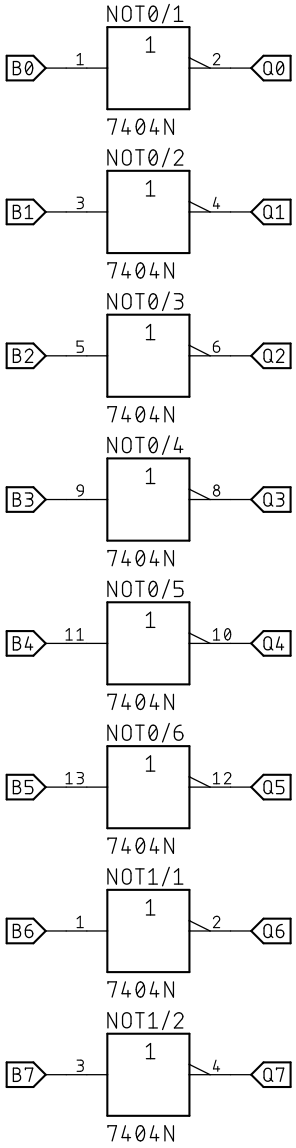


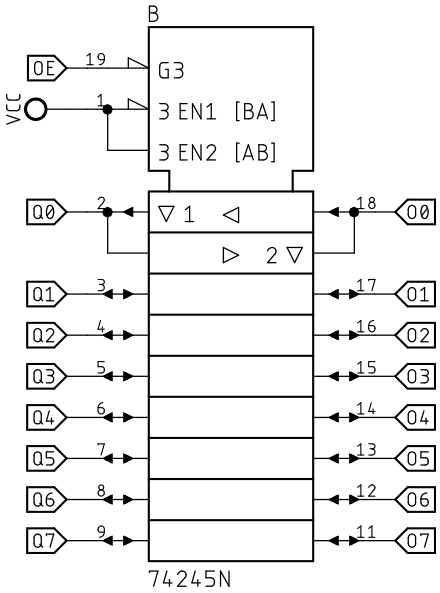


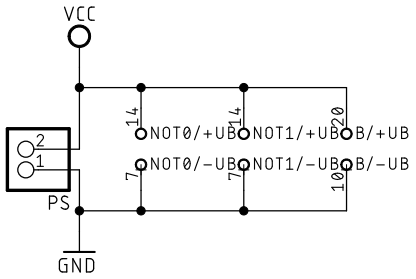


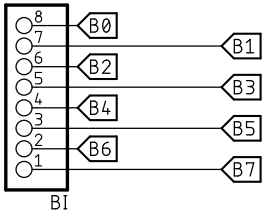
Template for logic modules

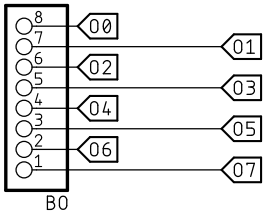
TITLE: Logic		
Document Number: 4.1		REV: 1
Date: 23. 10. 2021 21:09	Sheet: 1/1	

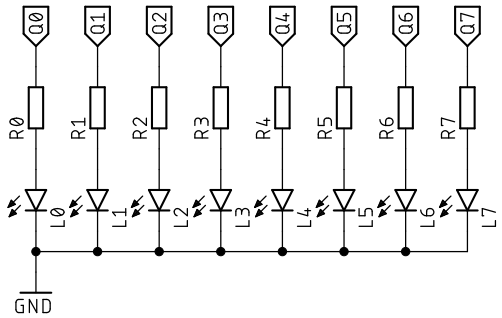


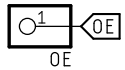






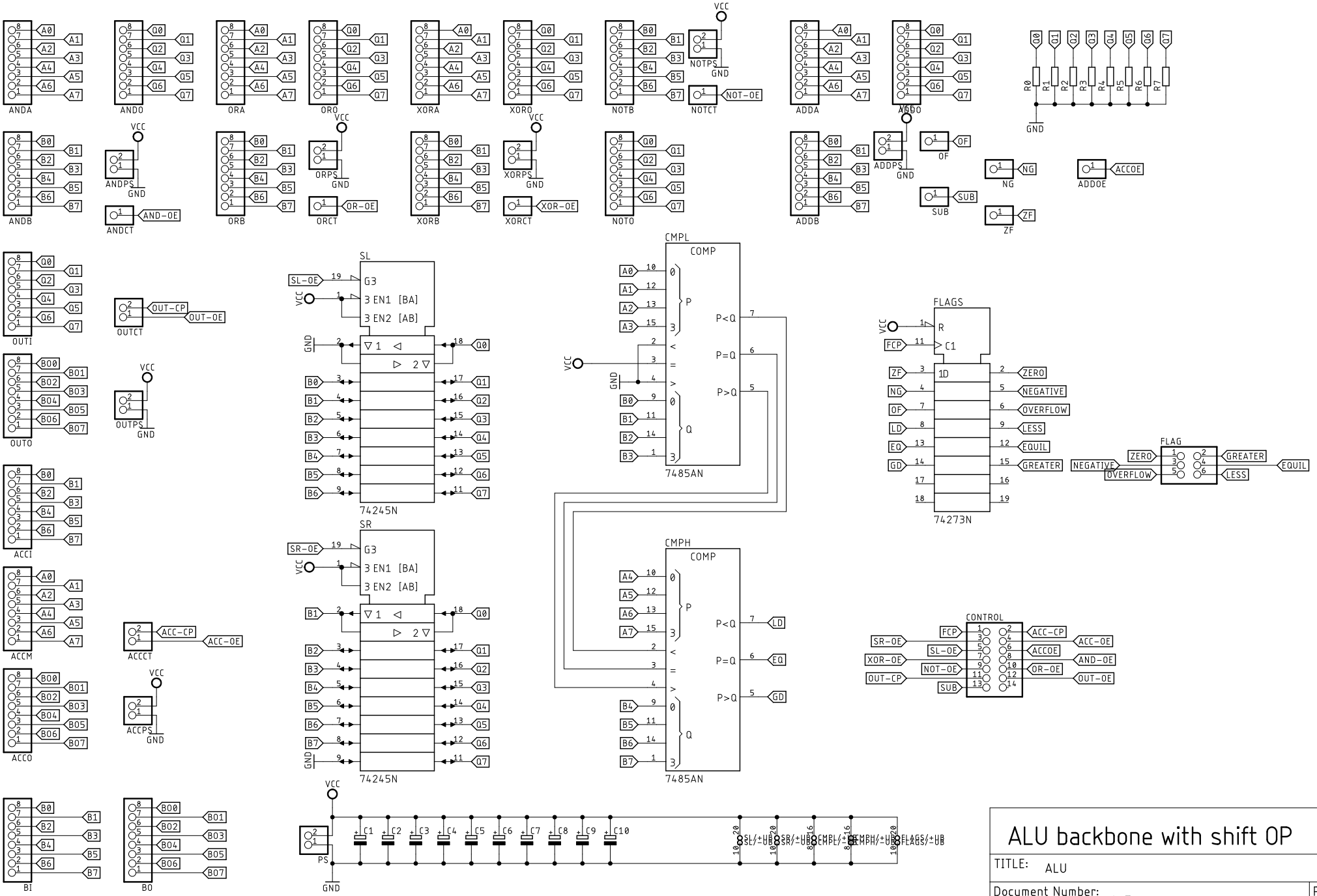






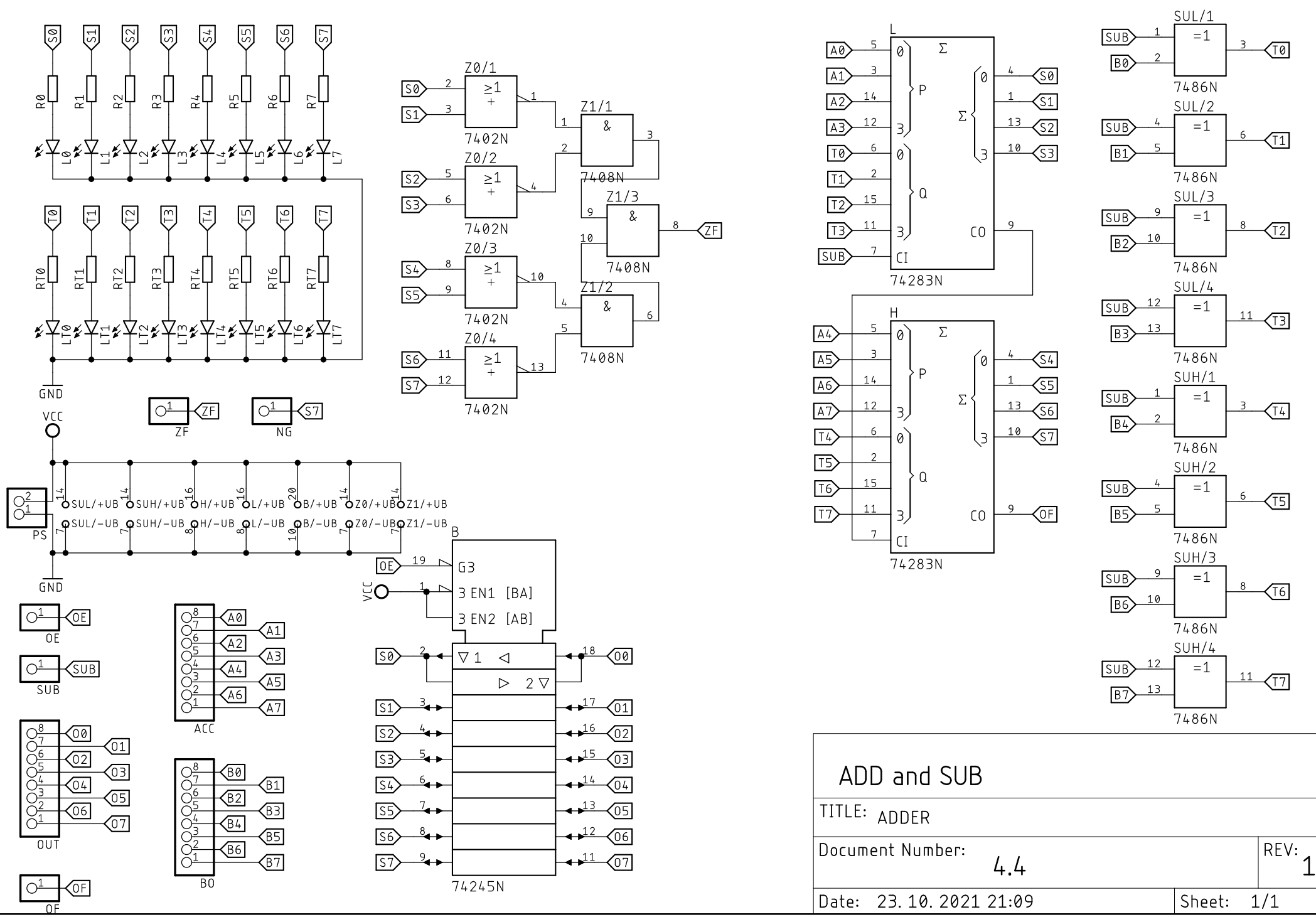
NOT logic module

TITLE: NOT		
Document Number: 4.2		REV: 1
Date: 23. 10. 2021 21:09	Sheet: 1/1	



ALU backbone with shift OP

TITLE: ALU		
Document Number: 4.3		REV: 1.1
Date: 23. 10. 2021 21:09	Sheet: 1/1	



ADD and SUB

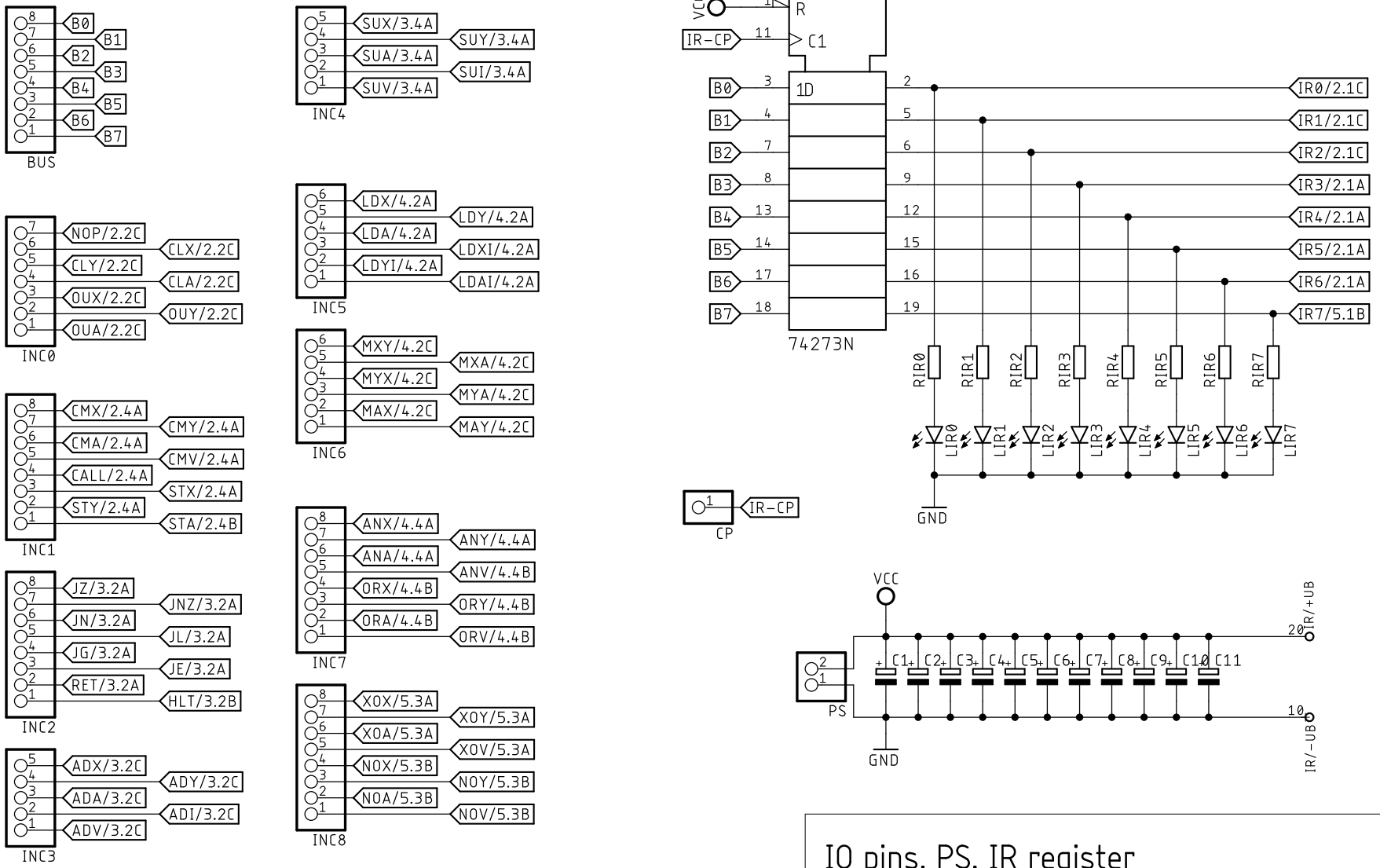
TITLE: ADDER

Document Number: 4.4

REV: 1

Date: 23. 10. 2021 21:09

Sheet: 1/1



IO pins, PS, IR register

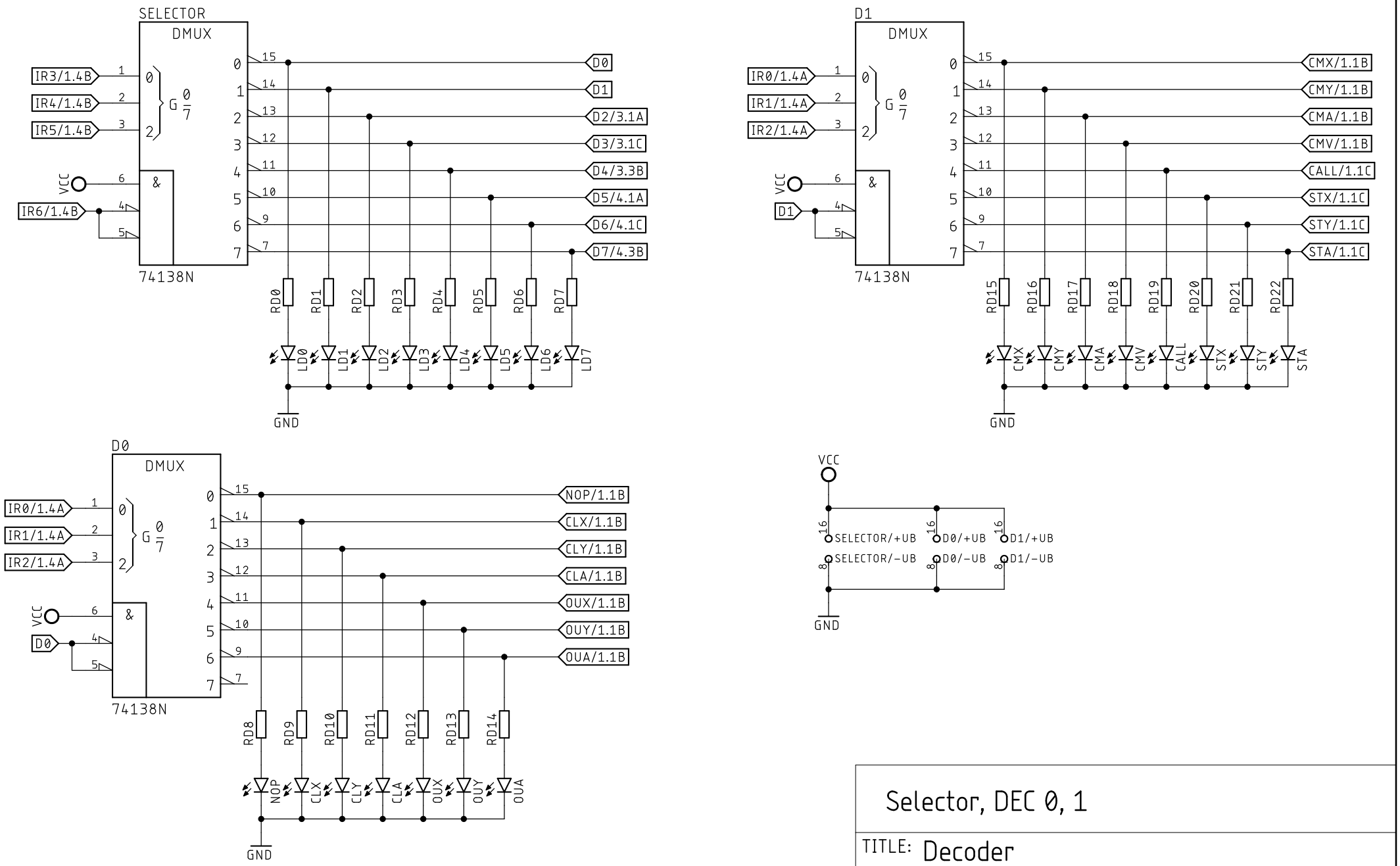
TITLE: Decoder

Document Number: 5.0

REV: 1.0

Date: 30. 10. 2021 22:52

Sheet: 1/5



Selector, DEC 0, 1

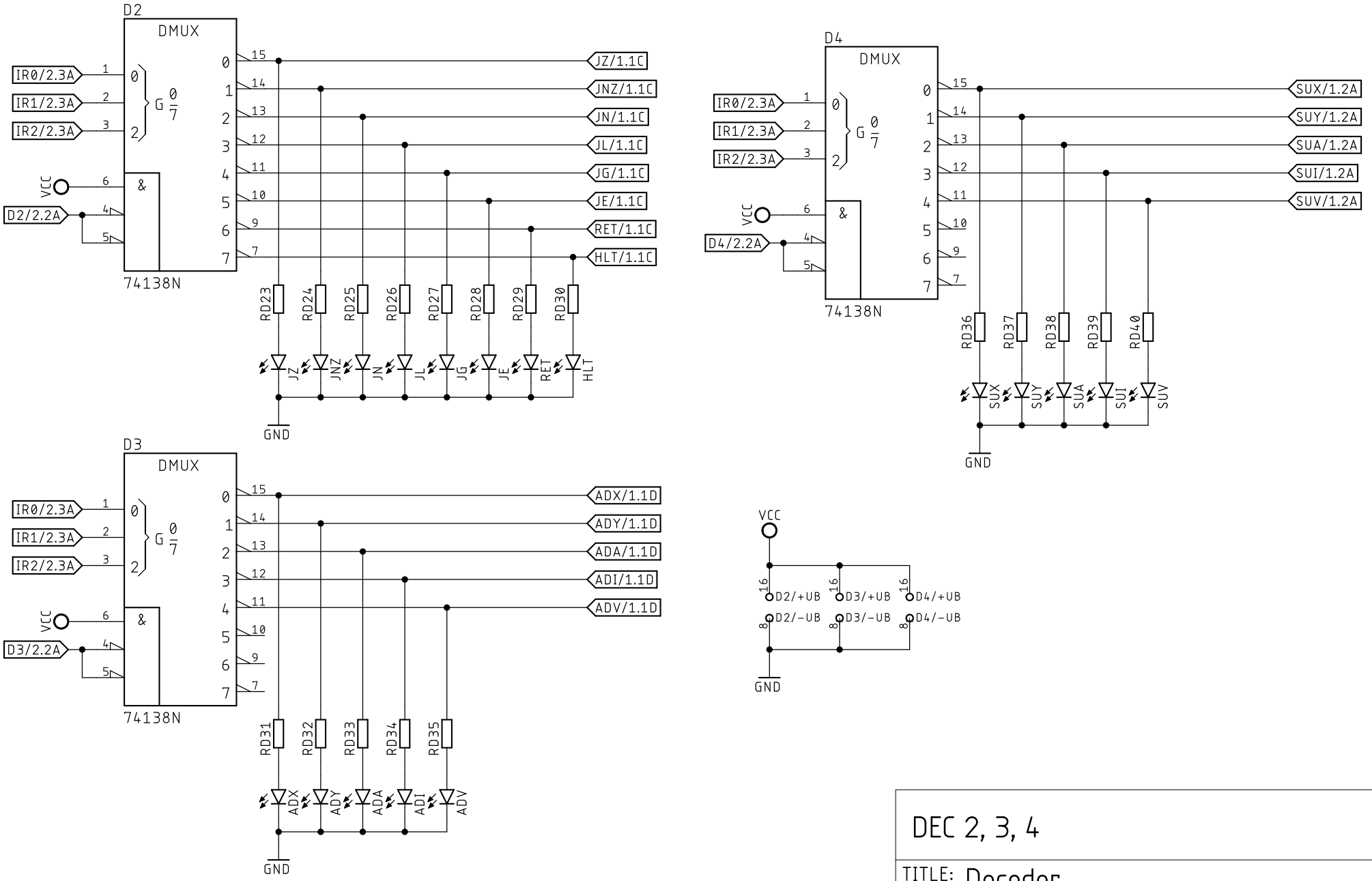
TITLE: Decoder

Document Number: 5.1

REV: 1.0

Date: 30. 10. 2021 22:52

Sheet: 2/5



DEC 2, 3, 4

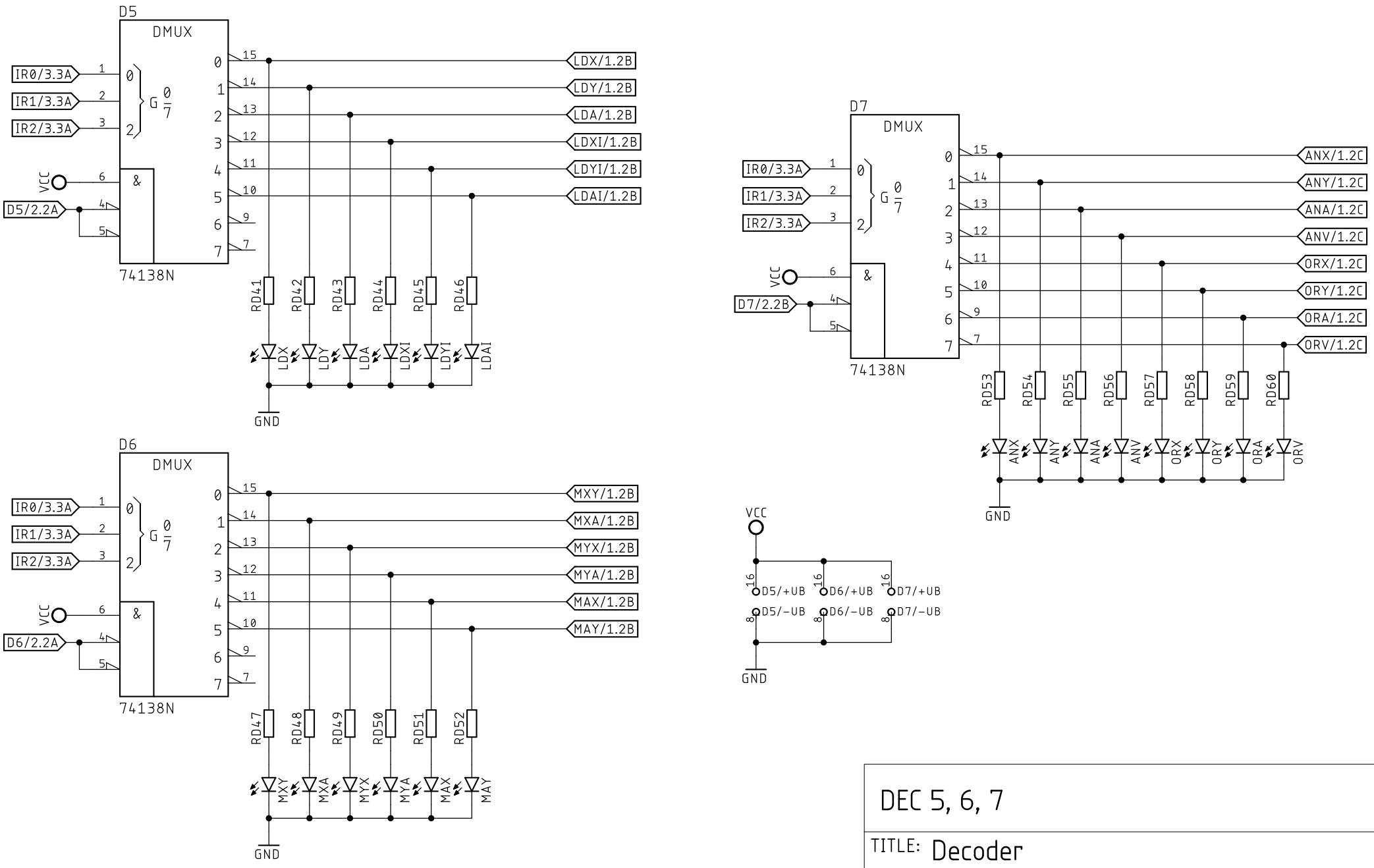
TITLE: Decoder

Document Number: 5.2

REV: 1.0

Date: 30. 10. 2021 22:52

Sheet: 3/5



DEC 5, 6, 7

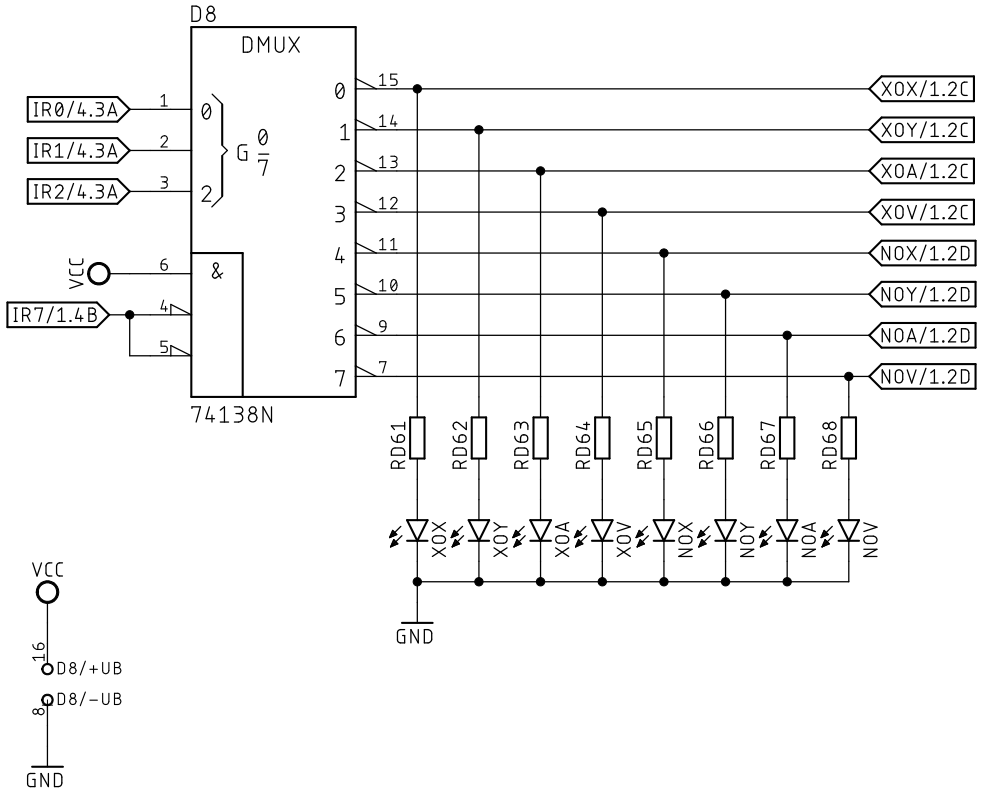
TITLE: Decoder

Document Number: 5.3

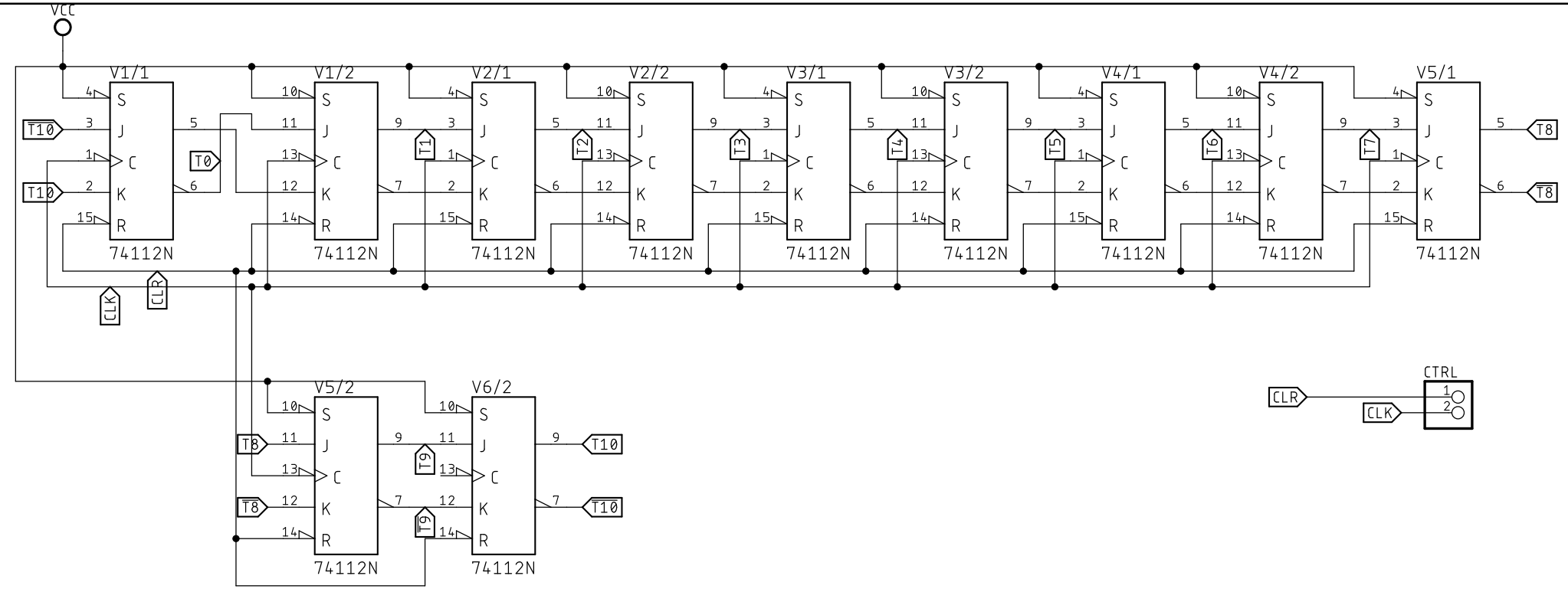
REV: 1.0

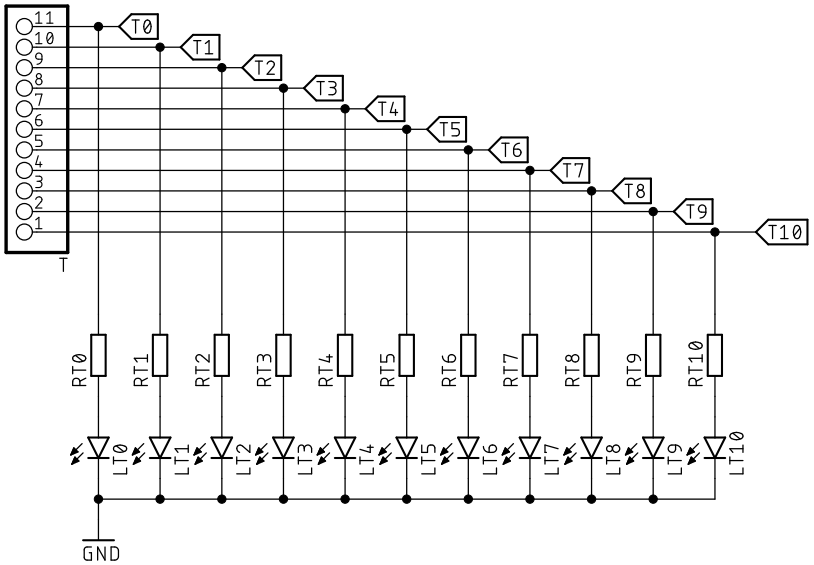
Date: 30. 10. 2021 22:52

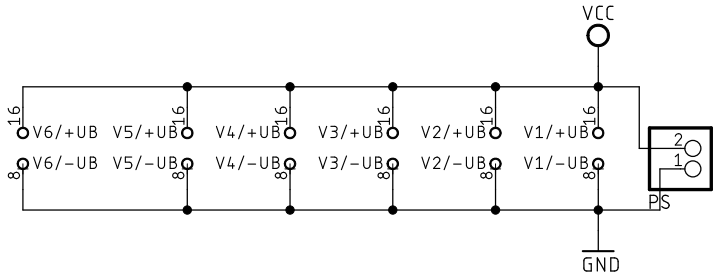
Sheet: 4/5



DEC 8		
TITLE: Decoder		
Document Number: 5.4		REV: 1.0
Date: 30. 10. 2021 22:52	Sheet: 5/5	

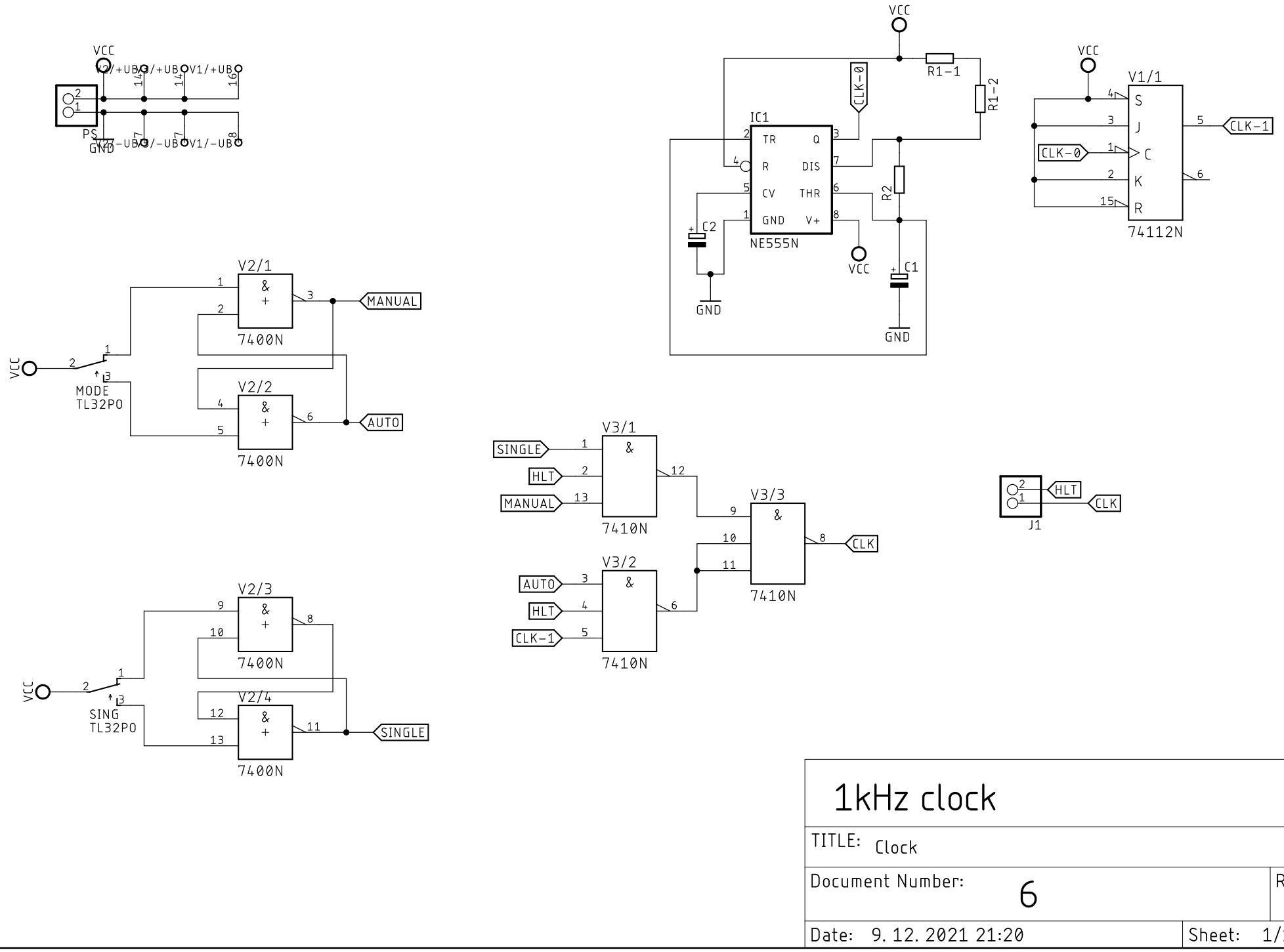






T-RING counter

TITLE: T-RING		
Document Number: 5.5		REV: 1.0
Date: 6. 12. 2021 8:08	Sheet: 1/1	



1kHz clock

TITLE: Clock		
Document Number: 6		REV: 1
Date: 9. 12. 2021 21:20	Sheet: 1/1	