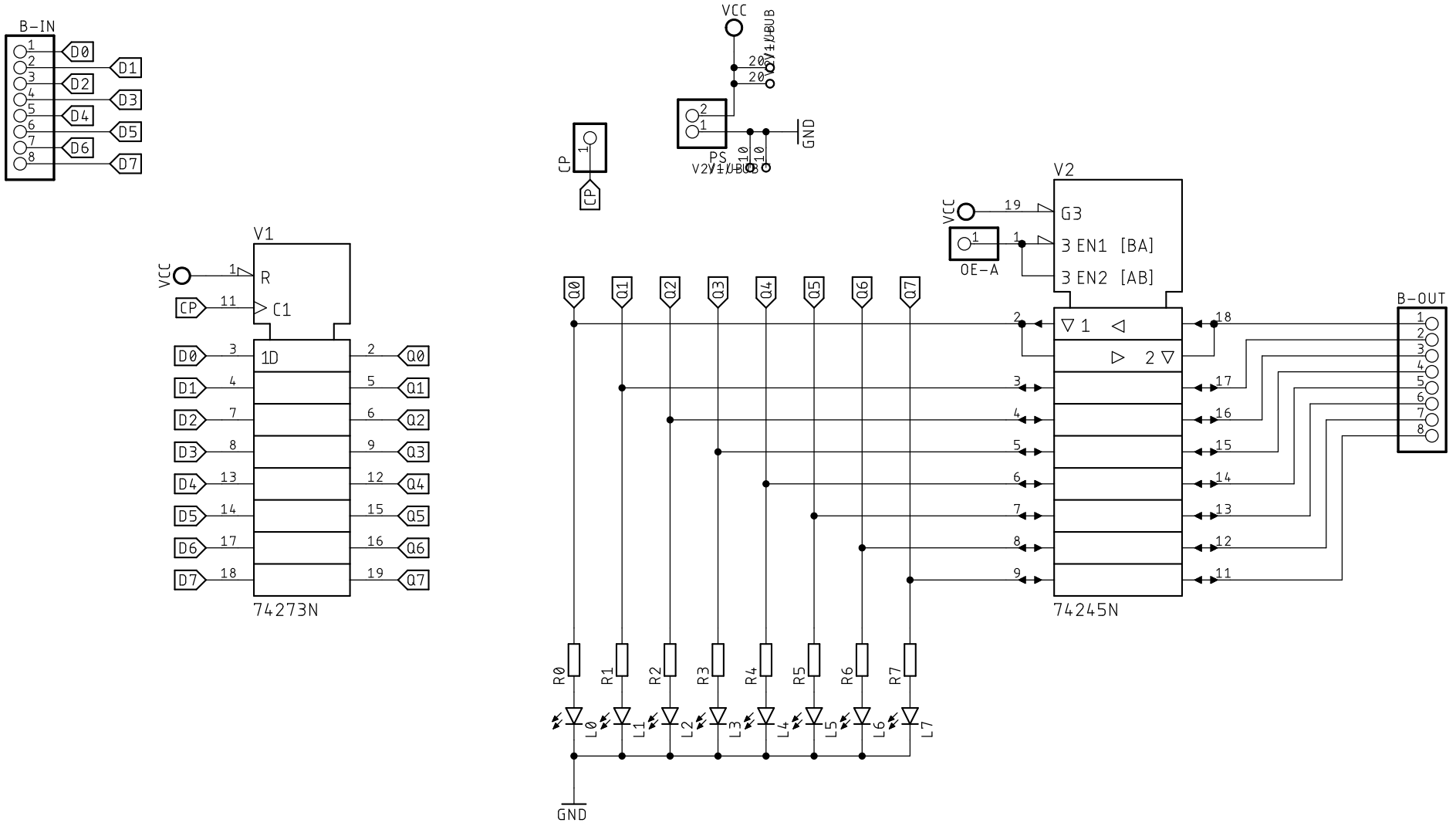
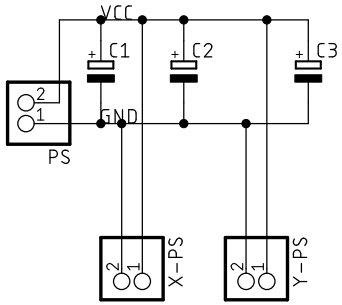
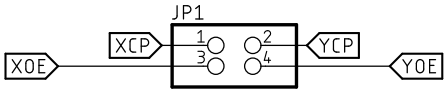
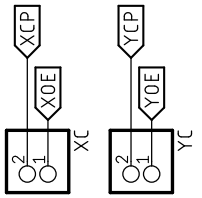


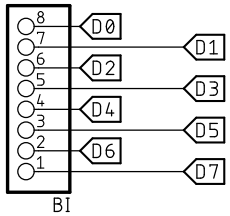
Register

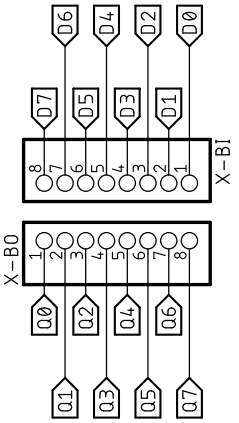
TITLE: Register		
Document Number: 1		REV: 1.1
Date: 9. 5. 2022 11:45	Sheet: 1/1	

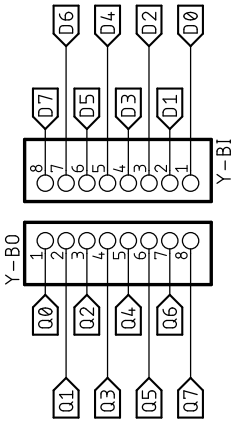


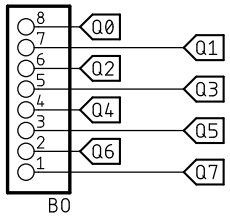






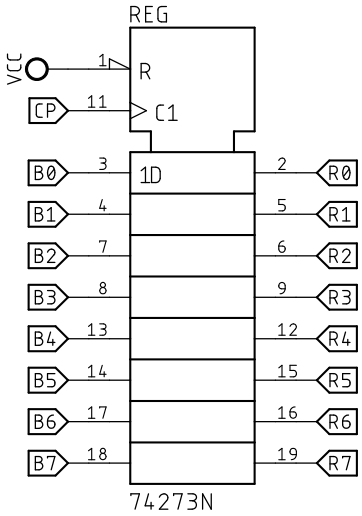


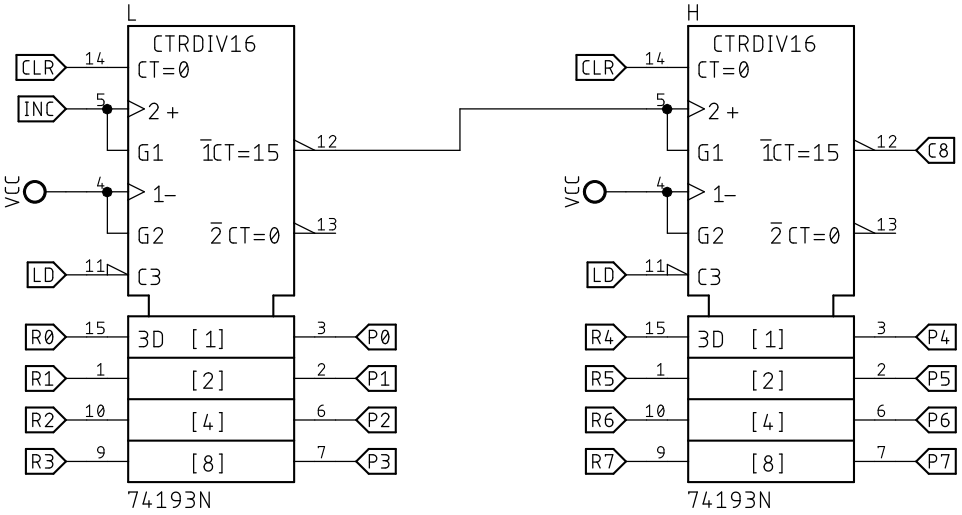


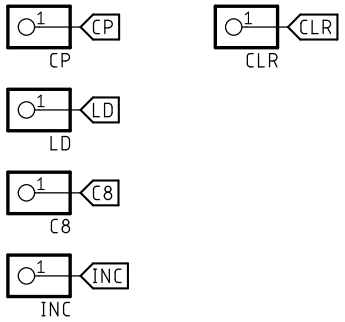


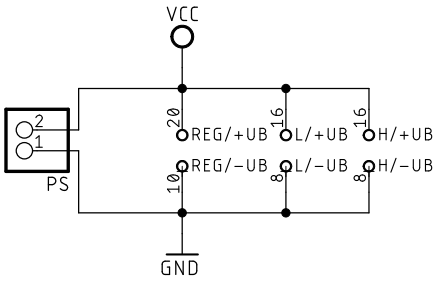
Prepojenie registrov X, Y a zbernice

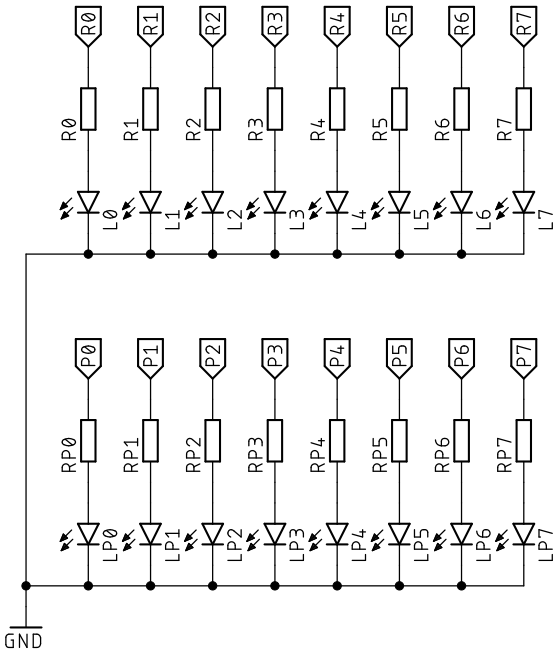
TITLE: Register–Bus		
Document Number: 1.1		REV: 1
Date: 9. 5. 2022 11:44	Sheet: 1/1	

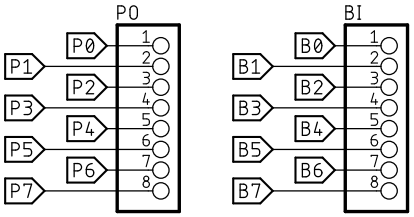






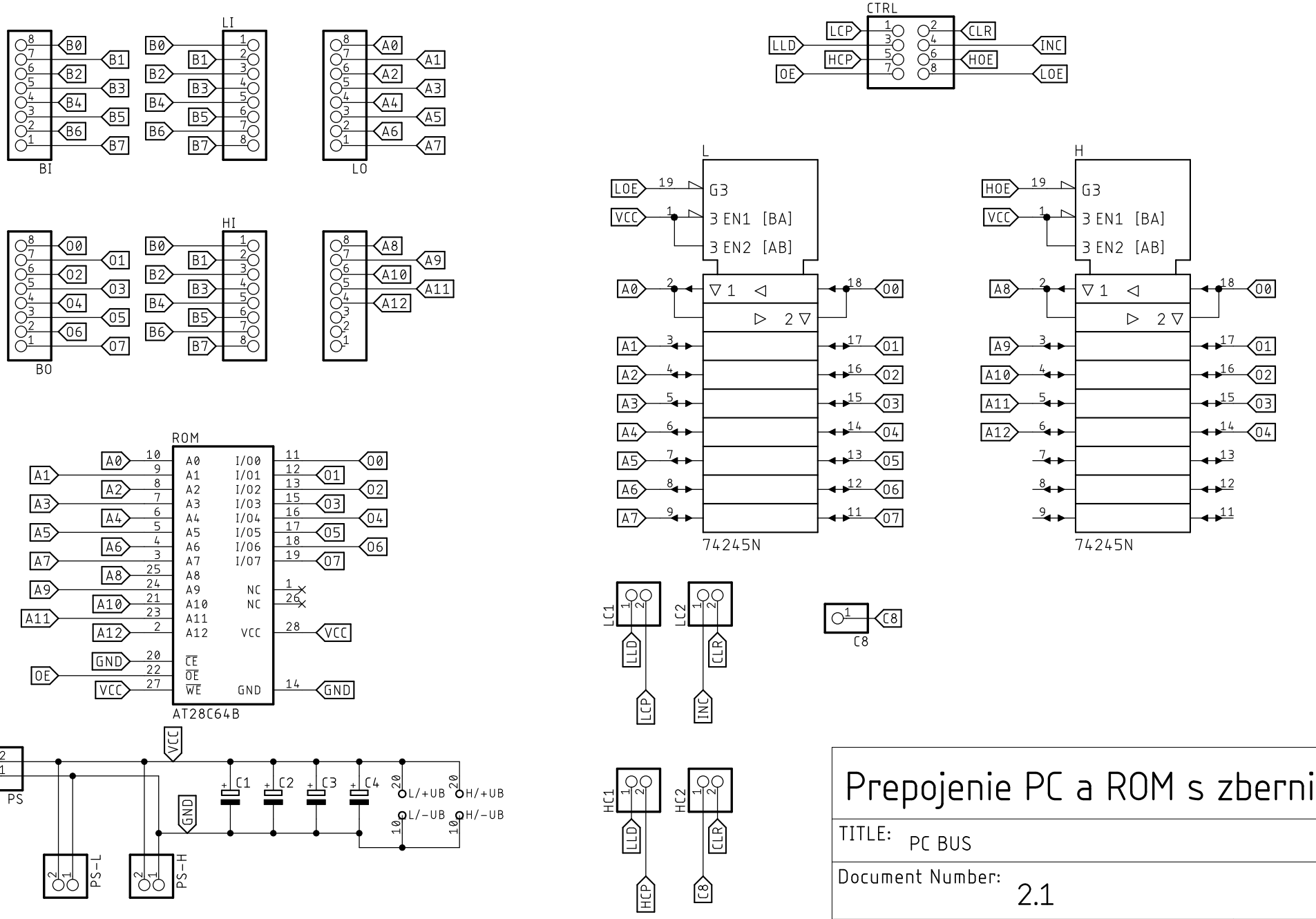






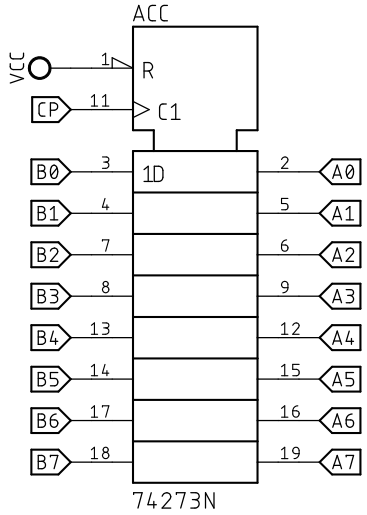
Pocitadlo s registrom

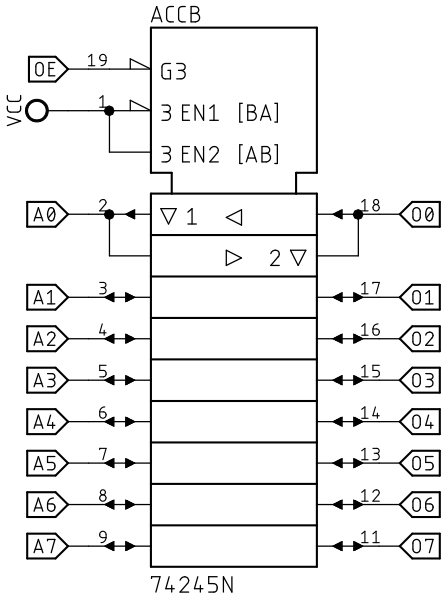
TITLE: Program Counter		
Document Number: 2		REV: 1.1
Date: 9. 5. 2022 11:49	Sheet: 1/1	

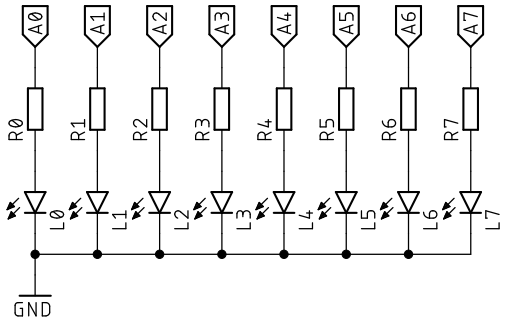


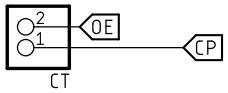
Prepojenie PC a ROM s zbernicou

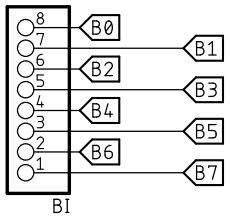
TITLE: PC BUS		
Document Number: 2.1		REV: 1
Date: 9. 5. 2022 11:48	Sheet: 1/1	

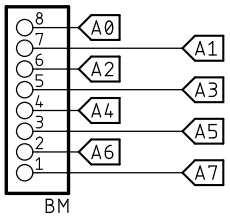


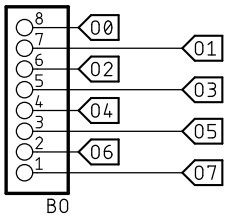


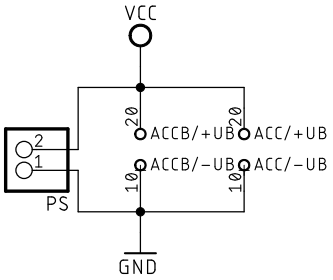






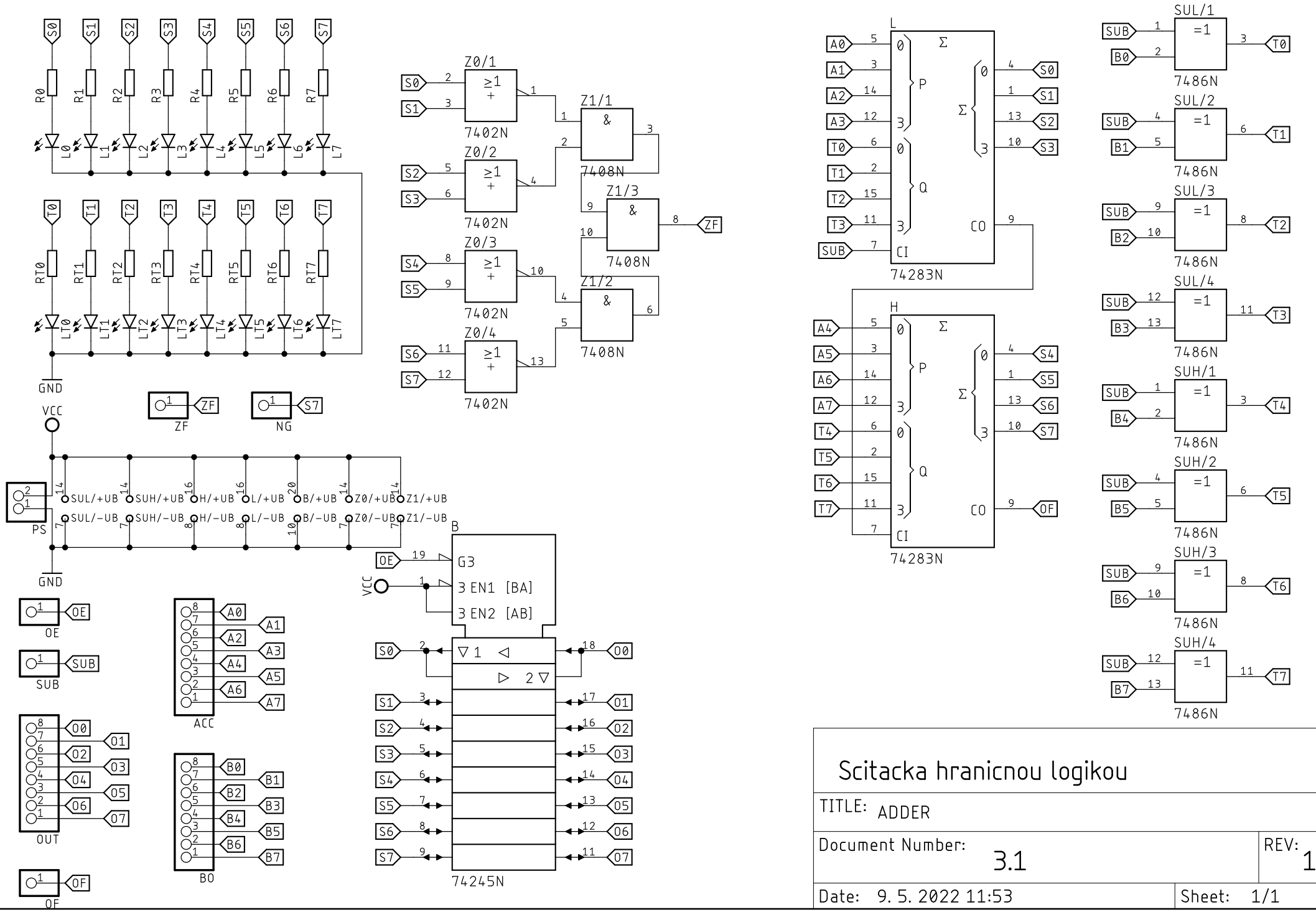






Register A

TITLE: ACC		
Document Number: 3		REV: 1
Date: 9. 5. 2022 11:50	Sheet: 1/1	



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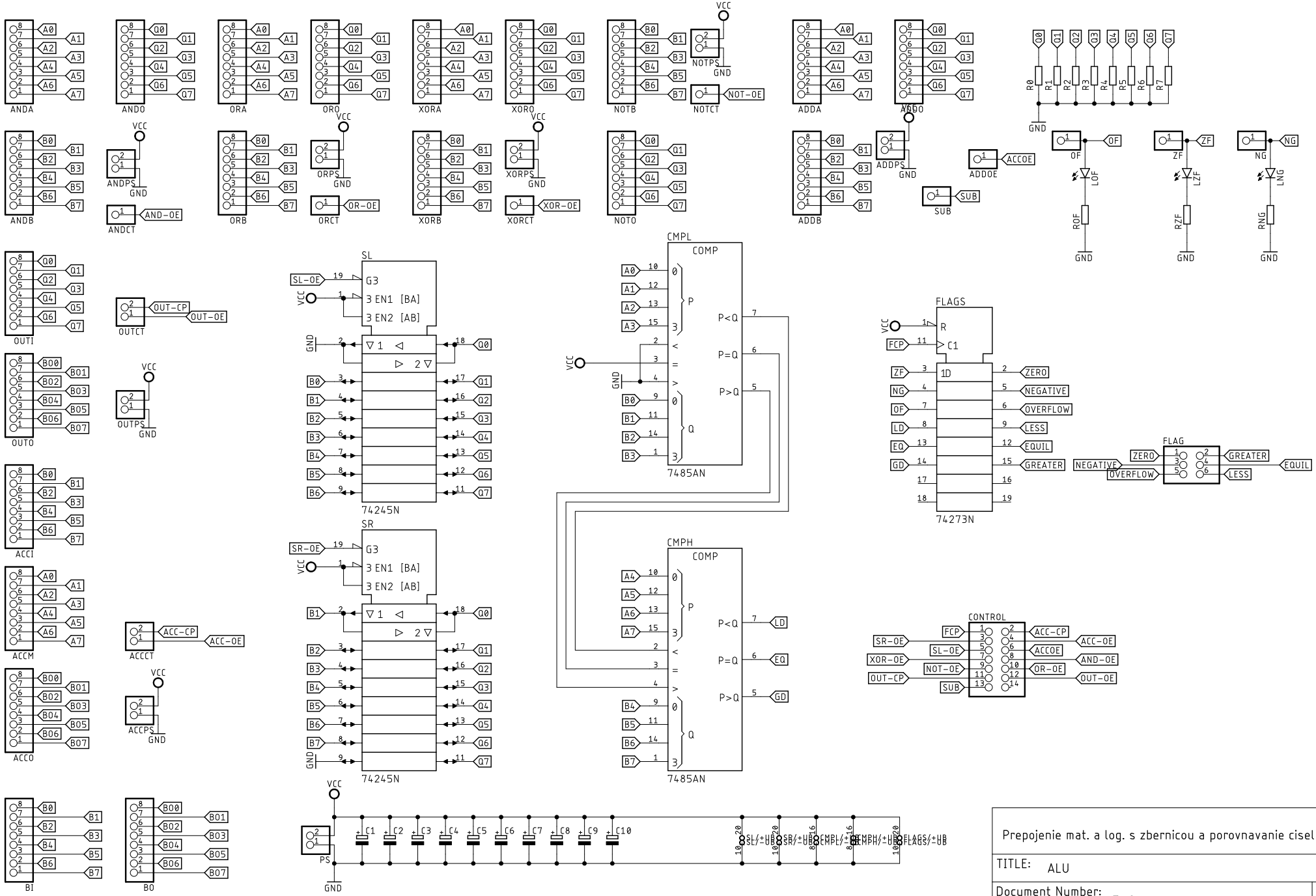
TITLE: ADDER		
Document Number: 3.1		REV: 1
Date: 9. 5. 2022 11:53	Sheet: 1/1	



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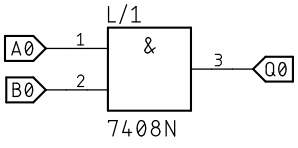
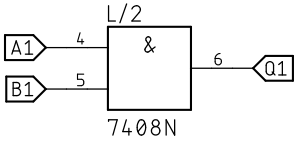
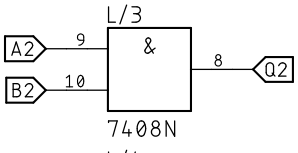
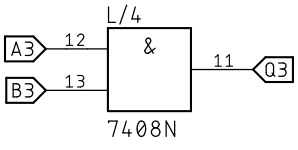
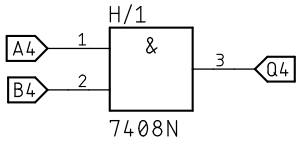
TITLE: ALU		
Document Number: 3.2		REV: 1.1
Date: 9. 5. 2022 11:54	Sheet: 1/1	

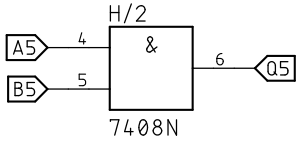


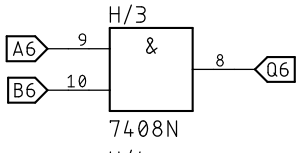


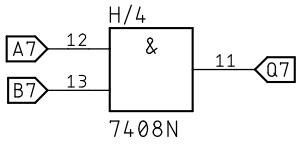


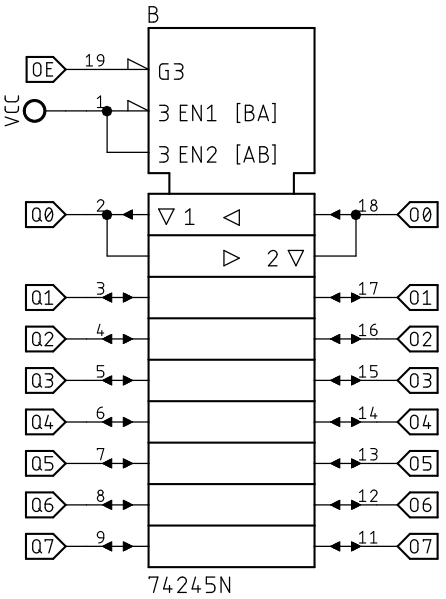


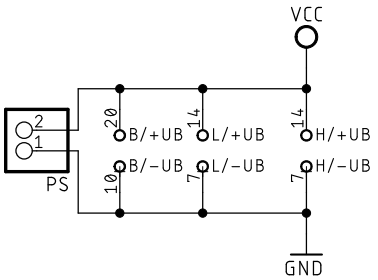


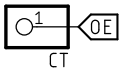


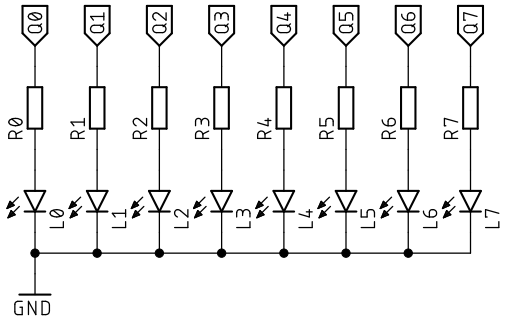


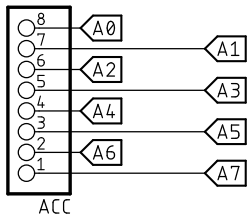


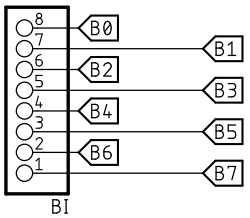


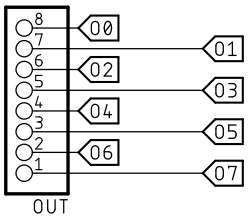






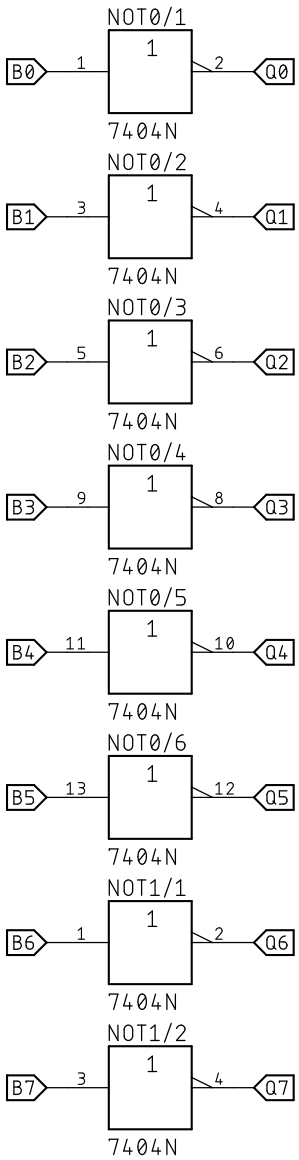


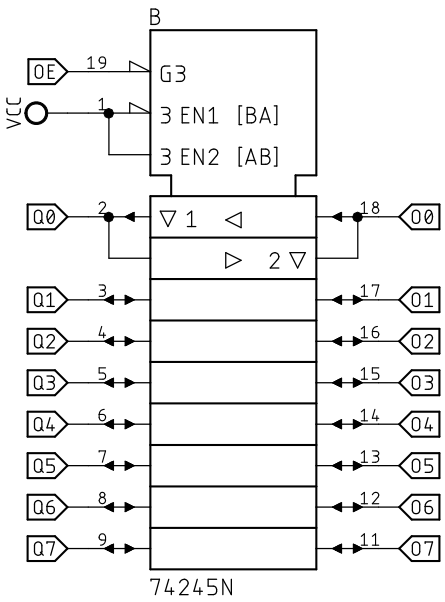


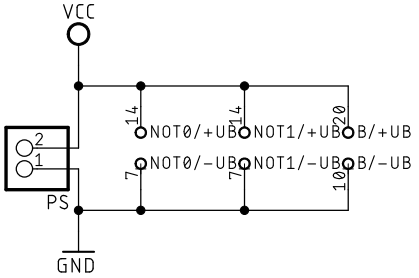


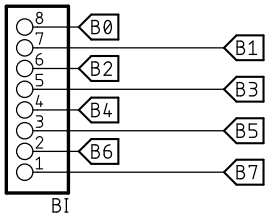
Logicky modul

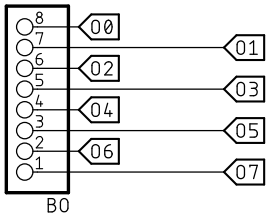
TITLE: Logic		
Document Number: 3.3		REV: 1
Date: 9. 5. 2022 11:55	Sheet: 1/1	

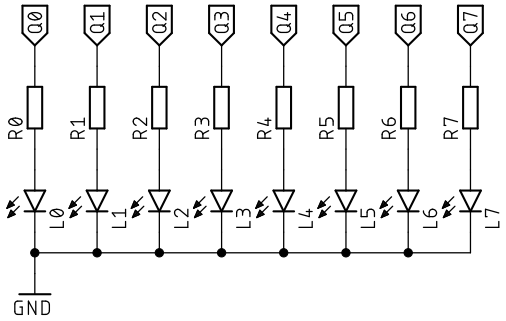


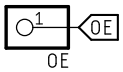












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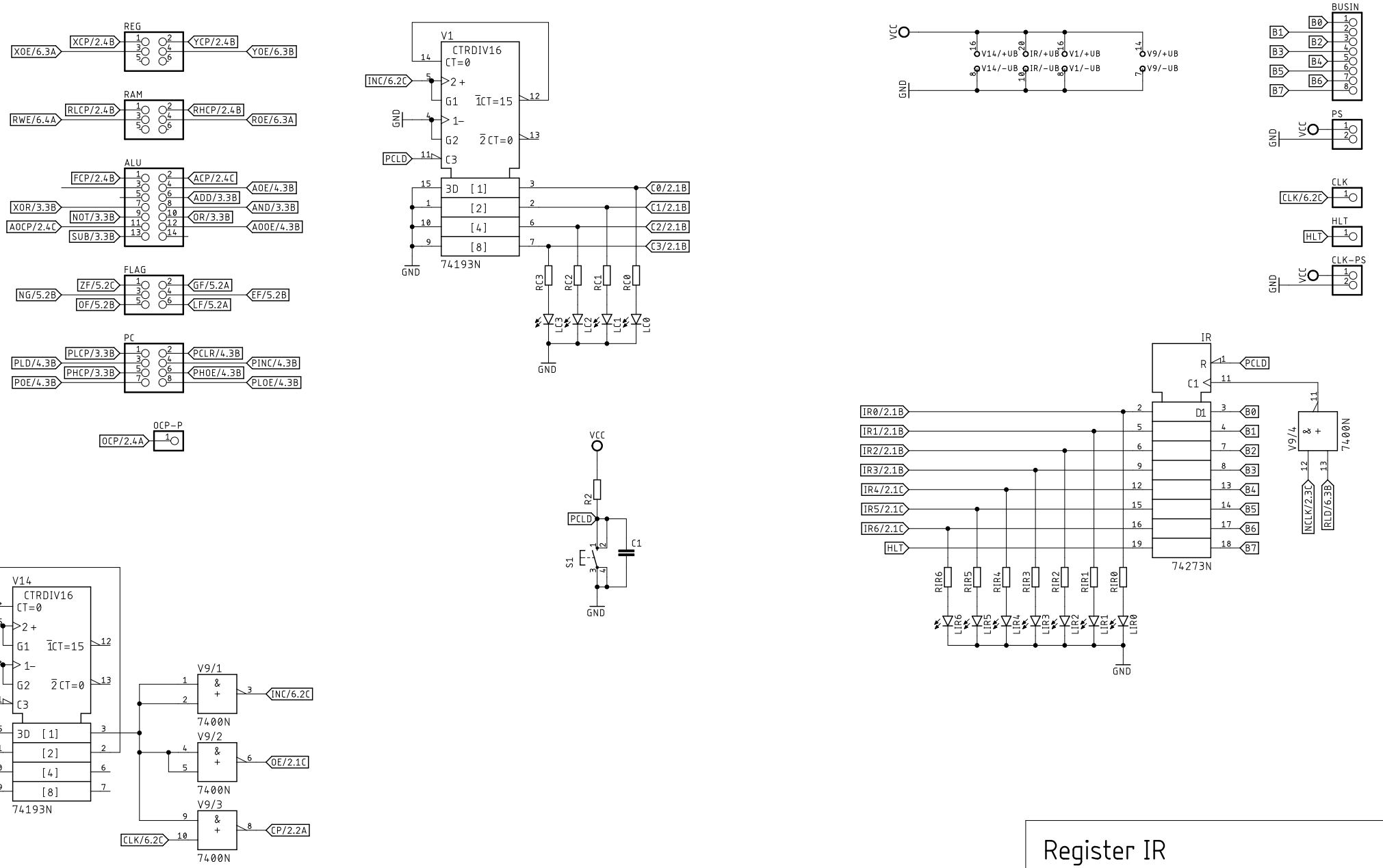
TITLE: NOT		
Document Number: 3.4		REV: 1
Date: 9. 5. 2022 11:56	Sheet: 1/1	



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TITLE:	CTRL
Document Number:	4
REV:	2
Date:	9. 5. 2022 12:02
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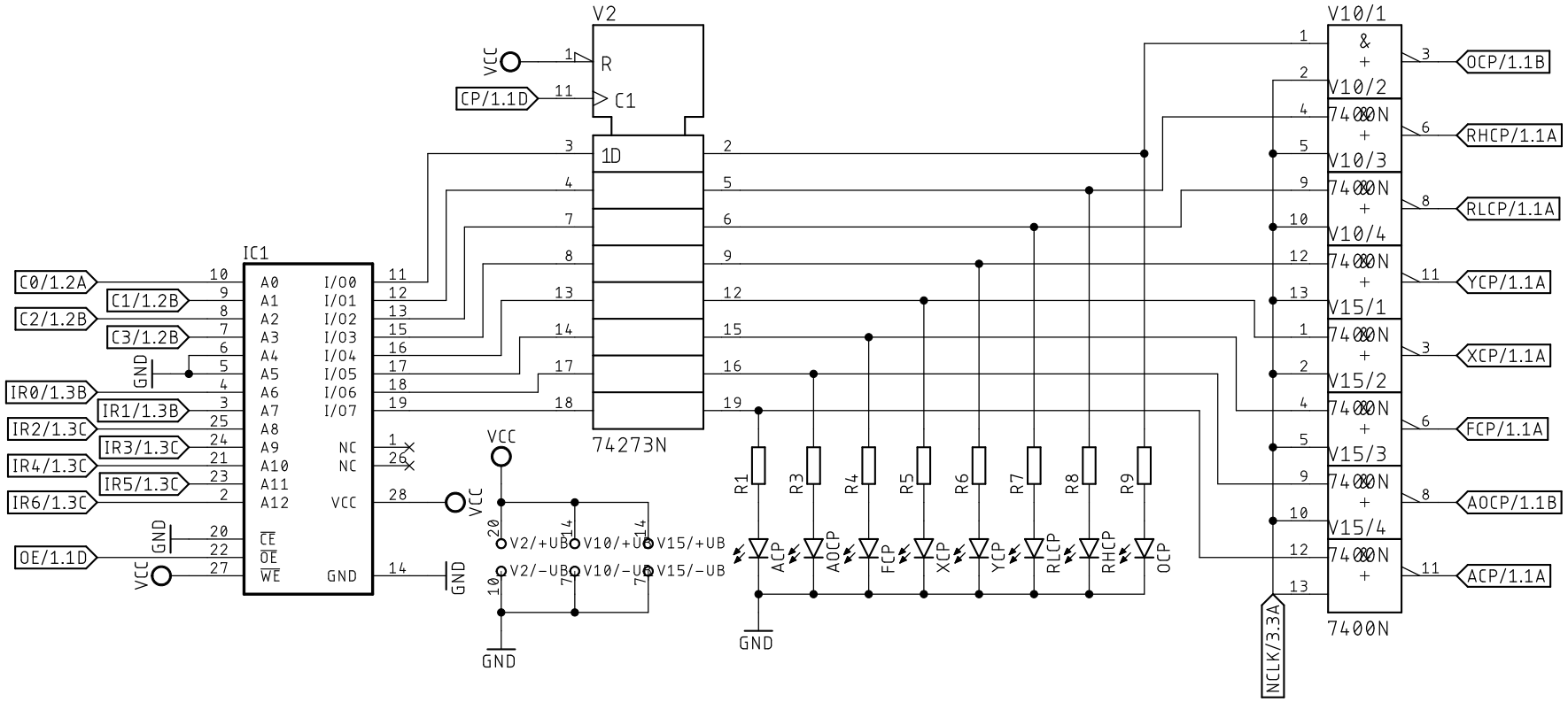

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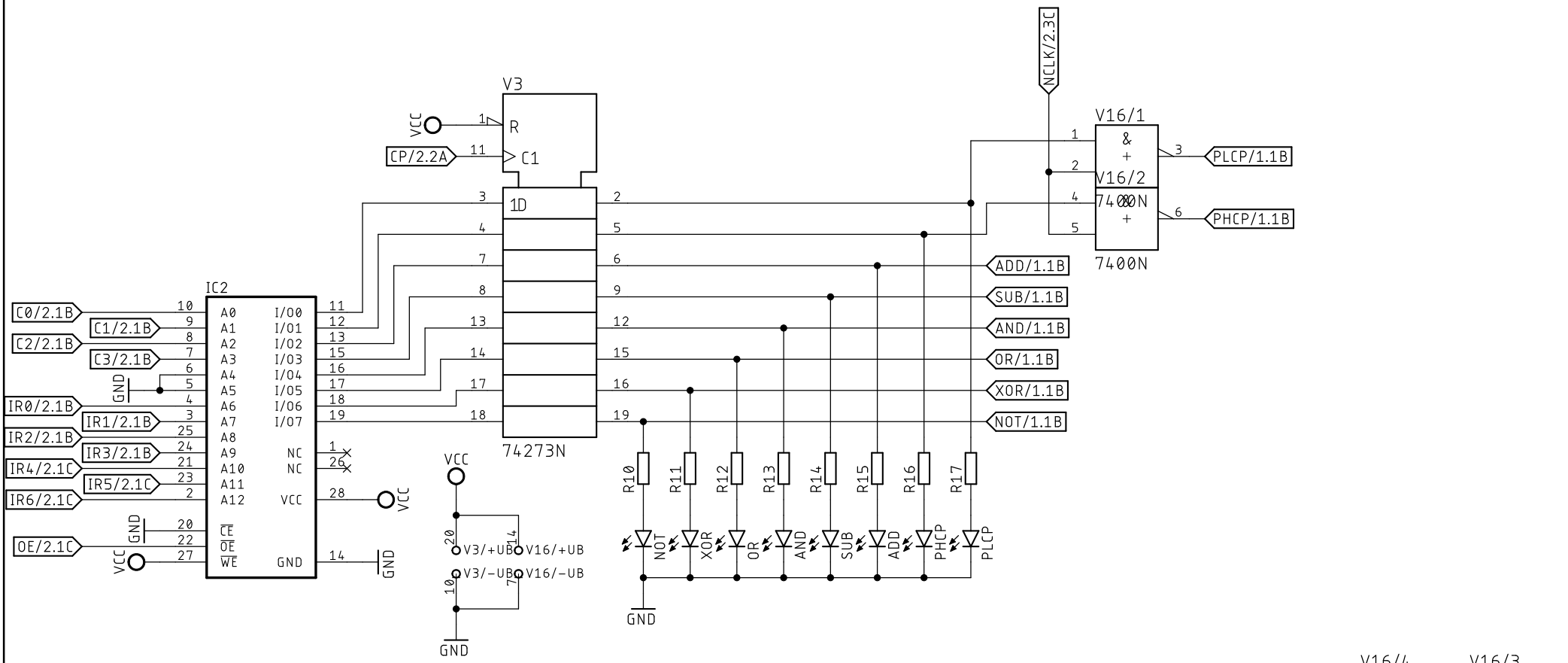
TITLE: CTRL		
Document Number: 4.1		REV: 2
Date: 9. 5. 2022 12:02	Sheet: 2/6	



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TITLE: CTRL		
Document Number: 4.2		REV: 2
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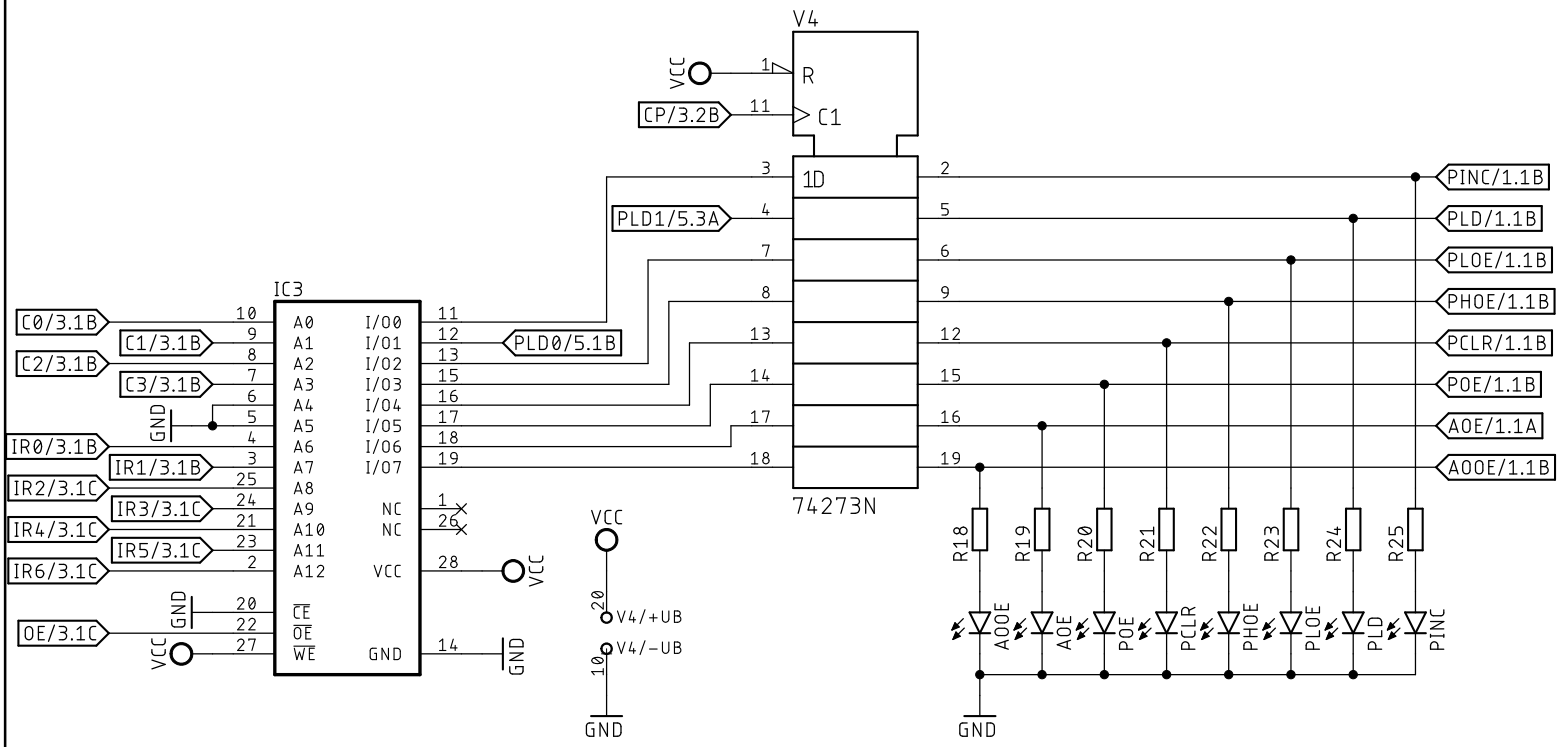

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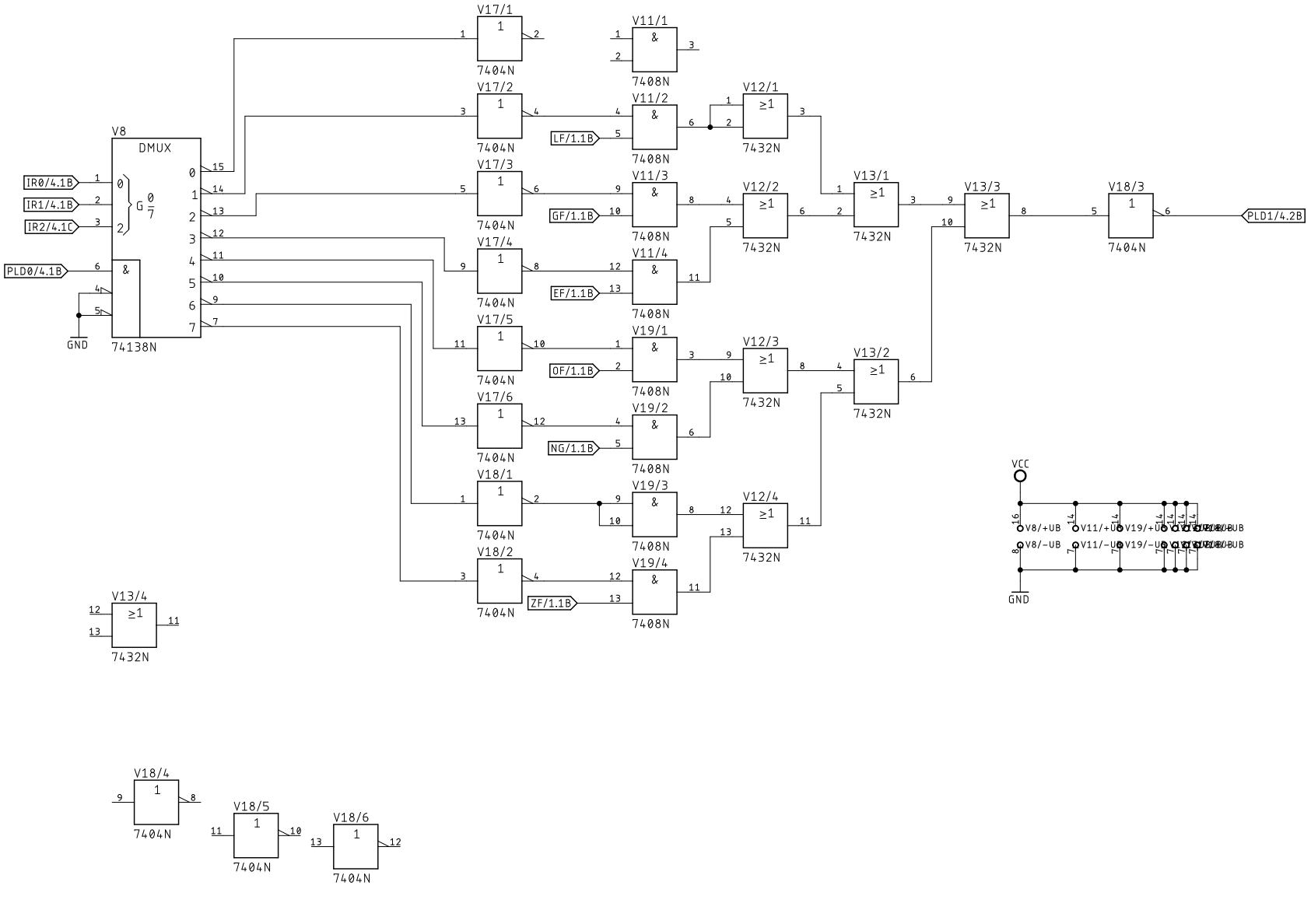
TITLE: CTRL		
Document Number: 4.3		REV: 2
Date: 9. 5. 2022 12:02	Sheet: 4/6	



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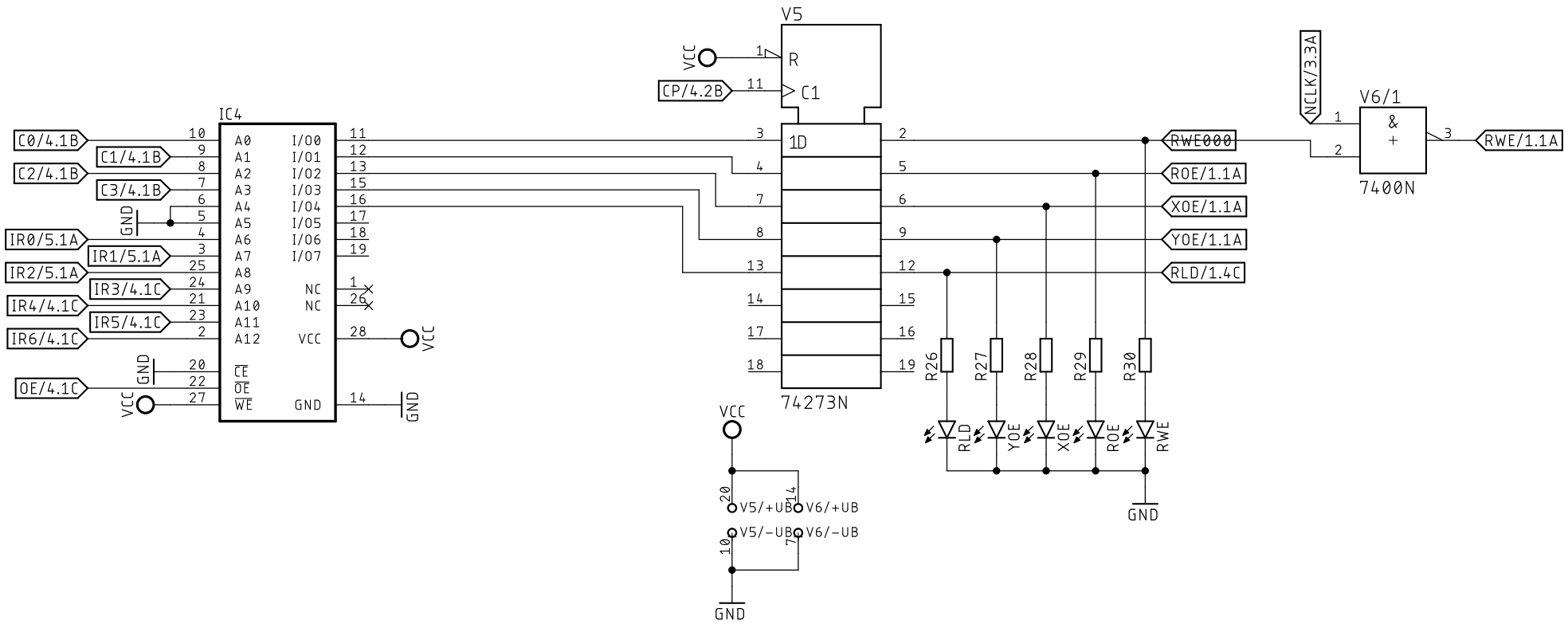
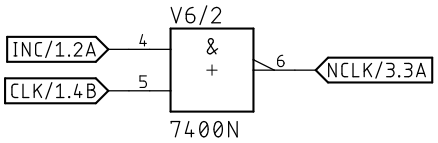
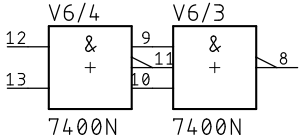
TITLE: CTRL	
Document Number: 4.4	REV: 2
Date: 9. 5. 2022 12:02	Sheet: 5/6







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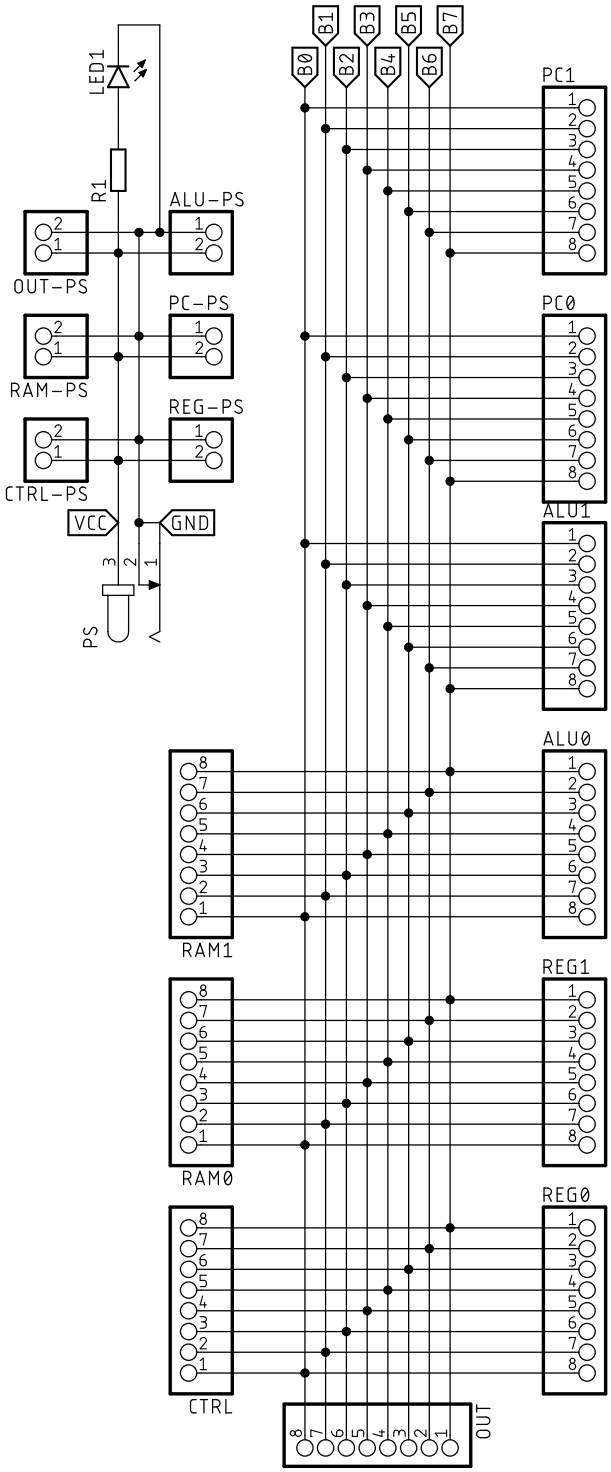
TITLE: CTRL		
Document Number: 4.5		REV: 2
Date: 9. 5. 2022 12:02	Sheet: 6/6	



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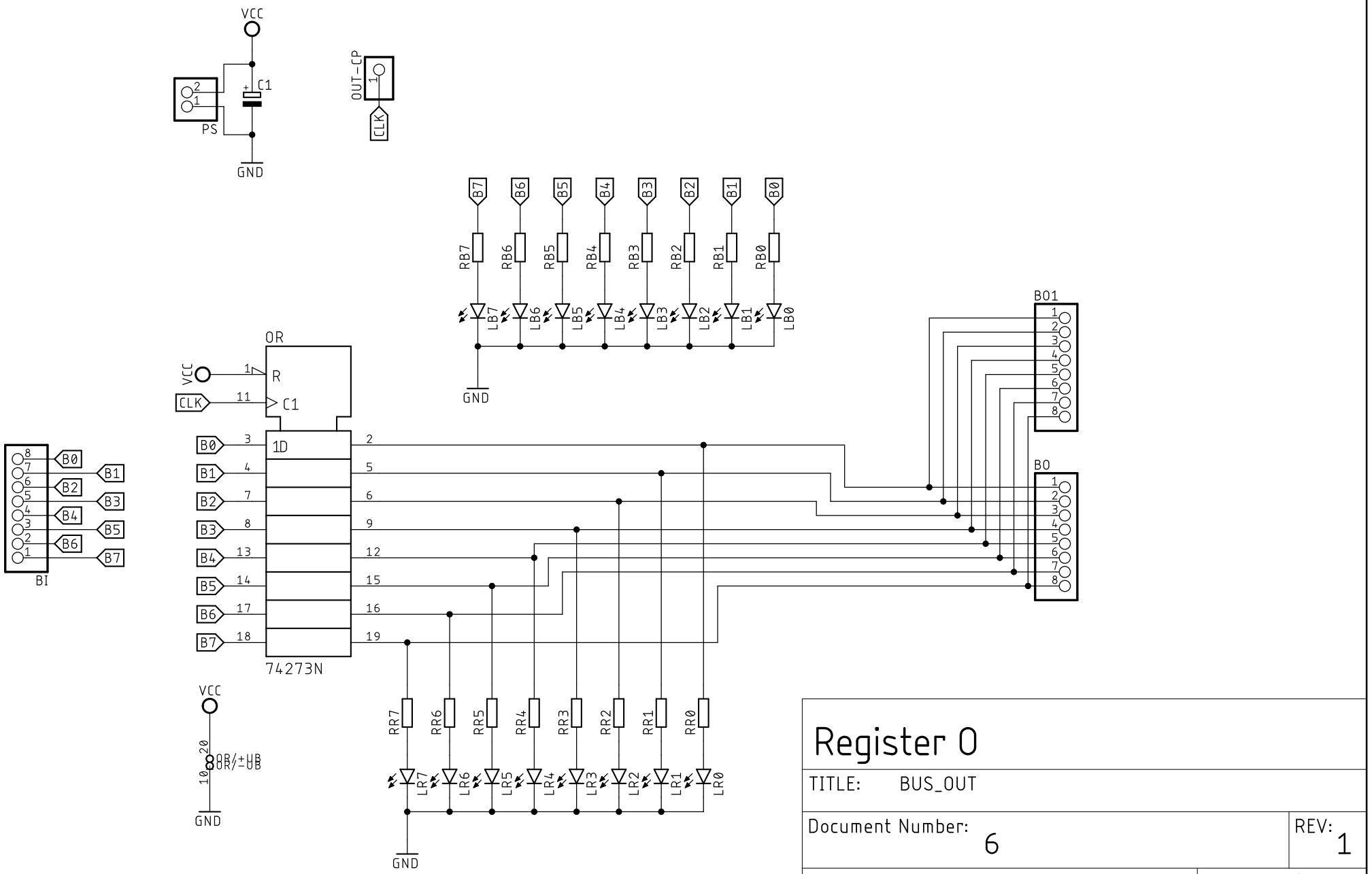
TITLE: bus		
Document Number: 5		REV: 1
Date: 9. 5. 2022 12:04	Sheet: 1/1	



Register 0

TITLE:	BUS_OUT	
Document Number:	6	REV: 1
Date: 9. 5. 2022 12:06		Sheet: 1/1