

The background features two thick, parallel diagonal lines in a vibrant green color. One line runs from the top-left towards the bottom-right, and the other runs from the top-right towards the bottom-left, creating a large 'X' shape across the white background.

Time Difference of Arrival With the DW3000

Presented by: Gabriel Kim

Trilateration

- Used in GPS positioning
- Not dependent on angles
- Location accuracy depends on distancing accuracy

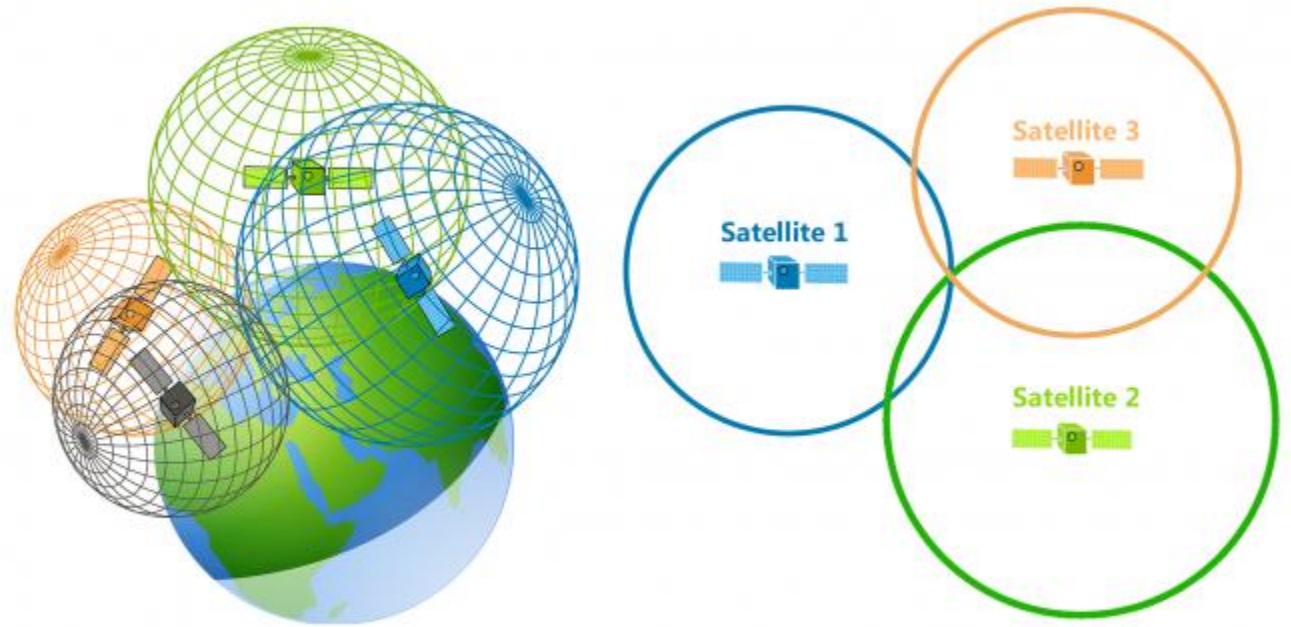


Figure 1: Intersection of Satellites
Source: [1]

Trilateration

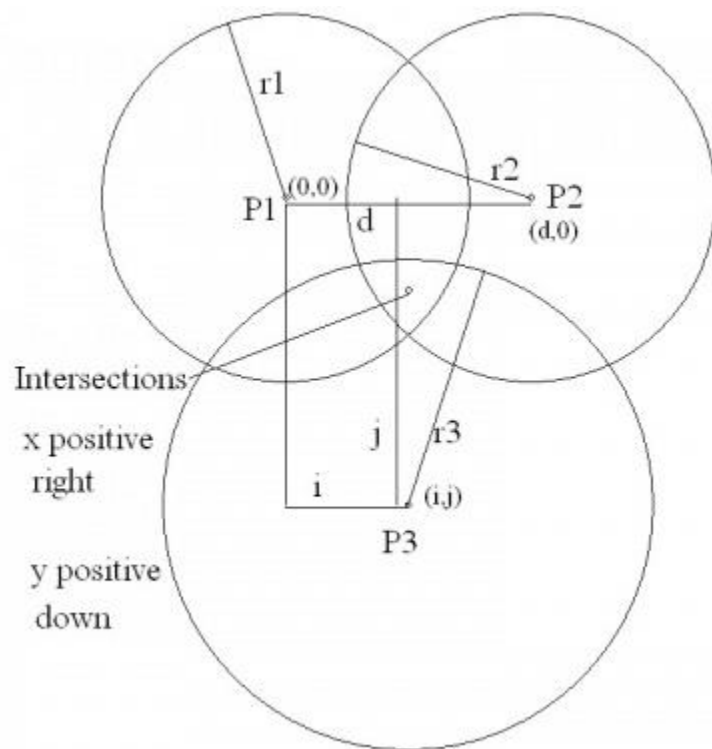


Figure 2: Sphere Radii and Coordinates

Source: [2]

- $x = \frac{r_1^2 - r_2^2 + d^2}{2d}$
- $y = \frac{r_1^2 - r_3^2 + i^2 + j^2}{2j} - \frac{i}{j}x$
- Equations can be adjusted for non (0,0) coordinates

What is UWB

- EM pulses are used to communicate
- Pulses made up of multiple frequencies stack on each other
- Bandwidth of 500MHz
- 9 channels with different middle frequencies
- Pulse position modulation

What is UWB

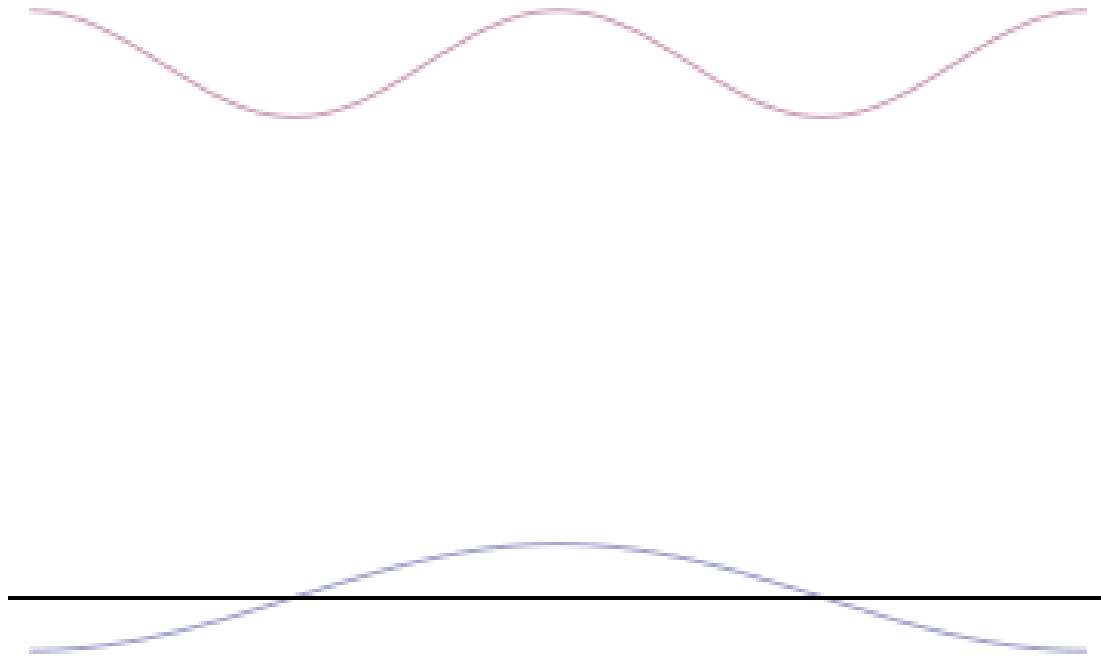


Figure 3: Pulse From Multiple Frequencies
Source: [3]

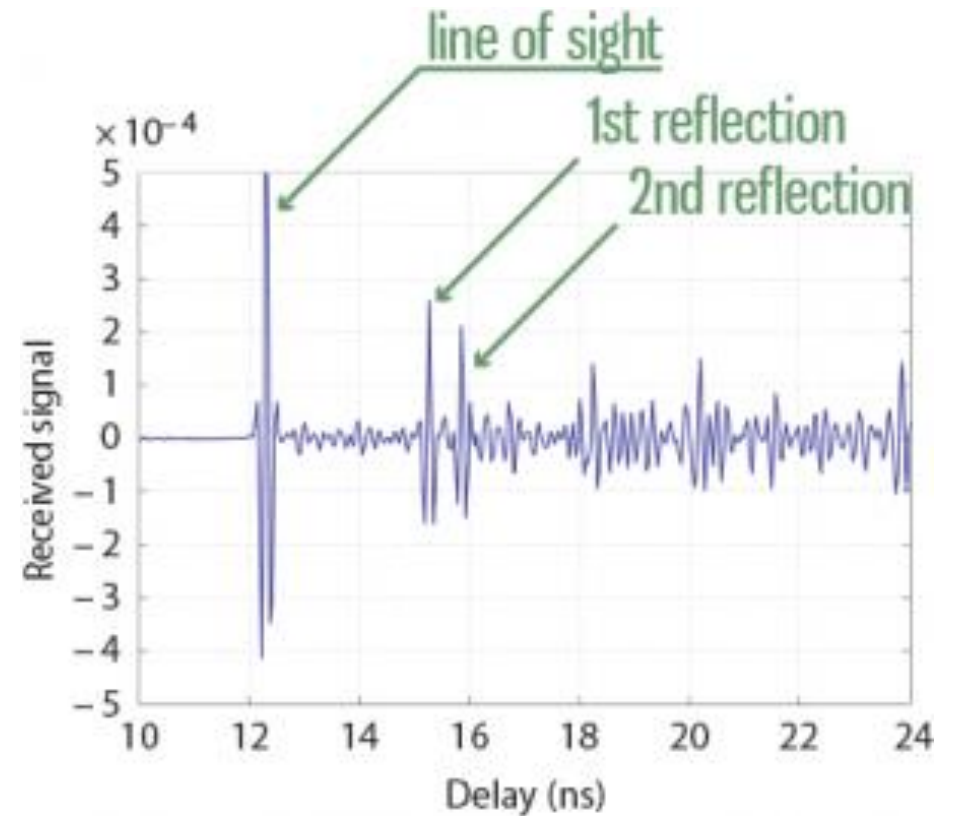


Figure 4: First Path pulse and Reflections
Source: [3]

Why UWB?

- Wide bandwidth allows for sharper pulses
- More accurate timestamps allow for TDoA distancing
- TDoA less affected by multipath interference than RSSI

Time Based Distancing

- Distance = time*speed
- Radio waves travel at light speed

Time Difference of Arrival(TDoA)

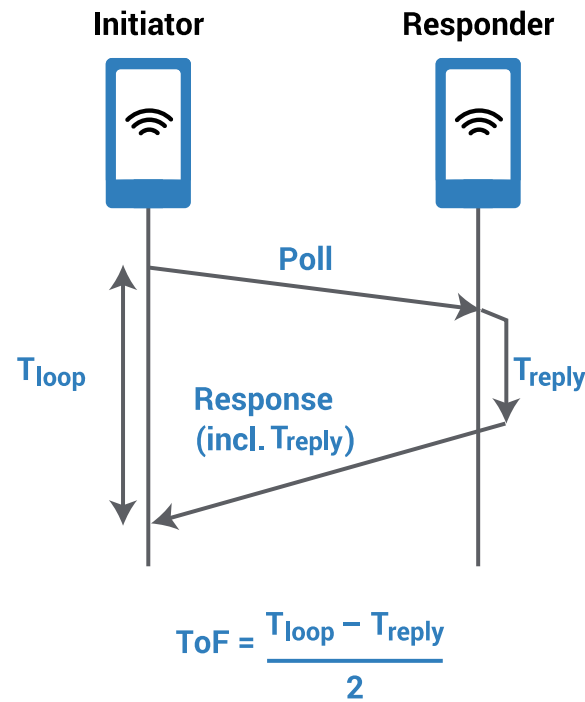


Figure 5: Example of TDoA Ranging
Source: [7]

Timestamps

- Four timestamps are needed
- Timestamps need to be distinguished from each other
- Accuracy and precision are necessary
- Errors and delays must be accounted for

The Problem

- What happens if the signal does not fall exactly on the rising edge?
- Clock speed of the DW3000 is 38.4 MHz
- Period of 26.04 ns
- Speed of light is 299,792,458 m/s
- Assuming perfect conditions max error is 7.807 m

The Solution

- Synchronize clocks
- Account for antenna delay
- Estimate ToA with an algorithm
- Get a faster clock

Phase Locked Loop(PLL)

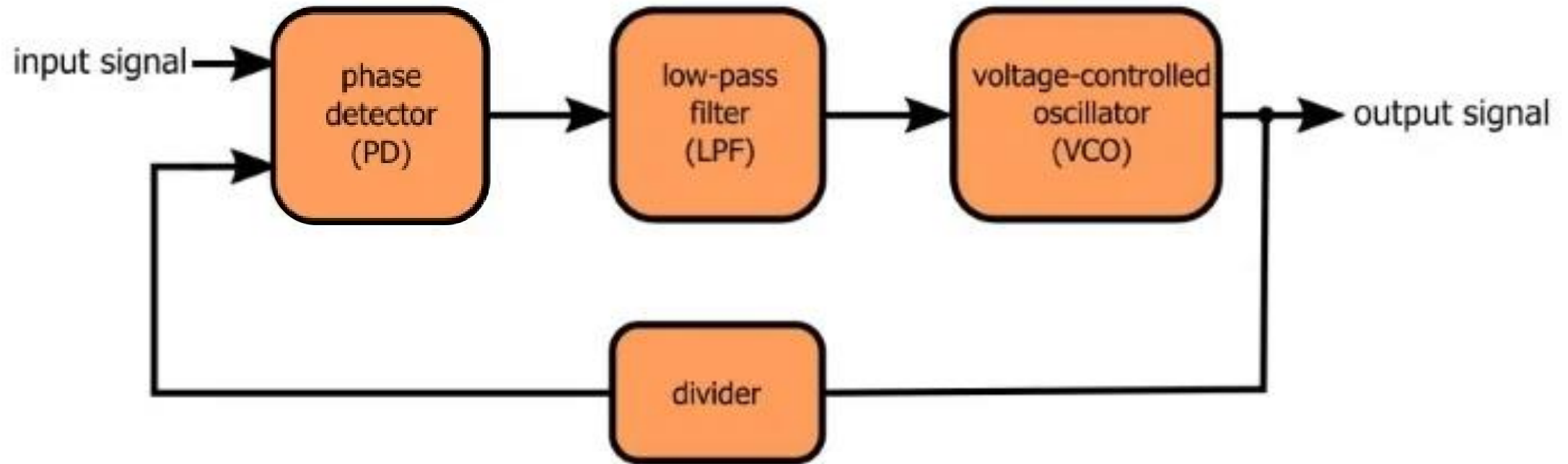


Figure 6: PLL Block Diagram
Source: [5]

Phase Locked Loop(PLL)

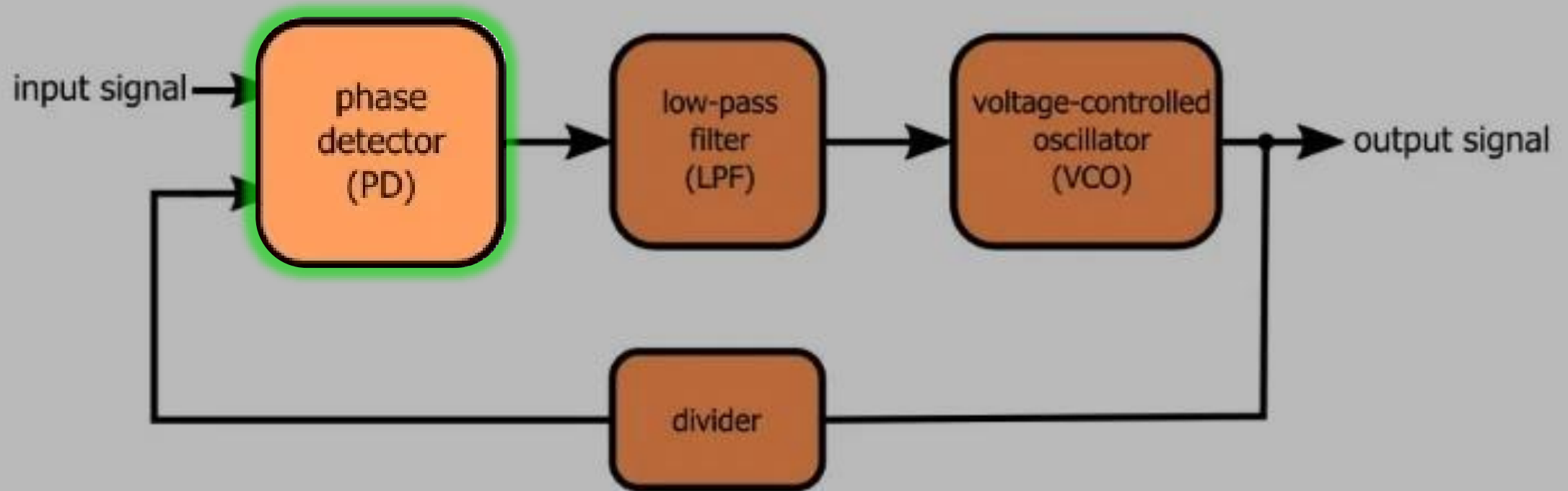


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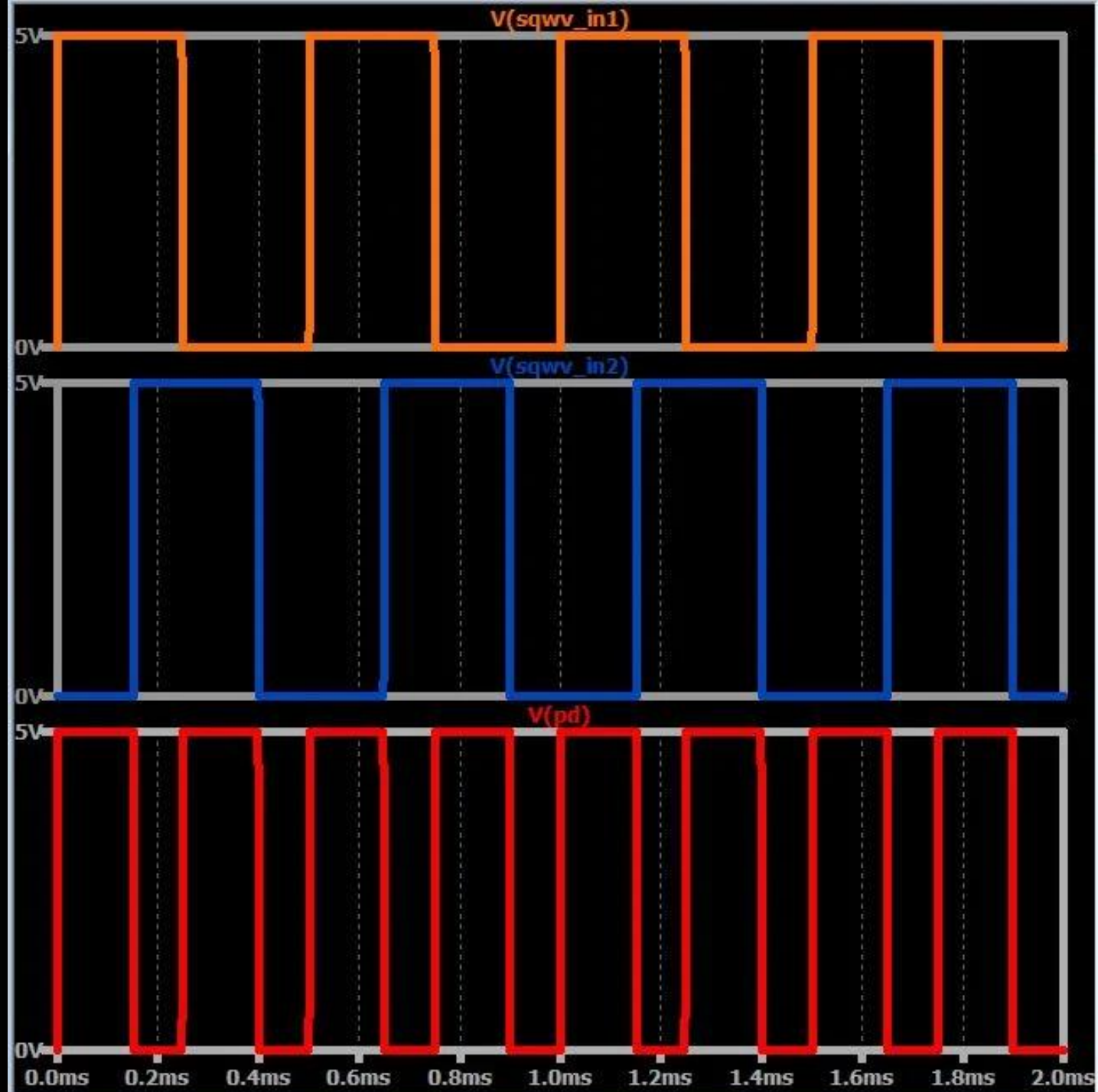


Figure 7: Voltage After
XOR Detection
Source: [6]

Phase Locked Loop(PLL)

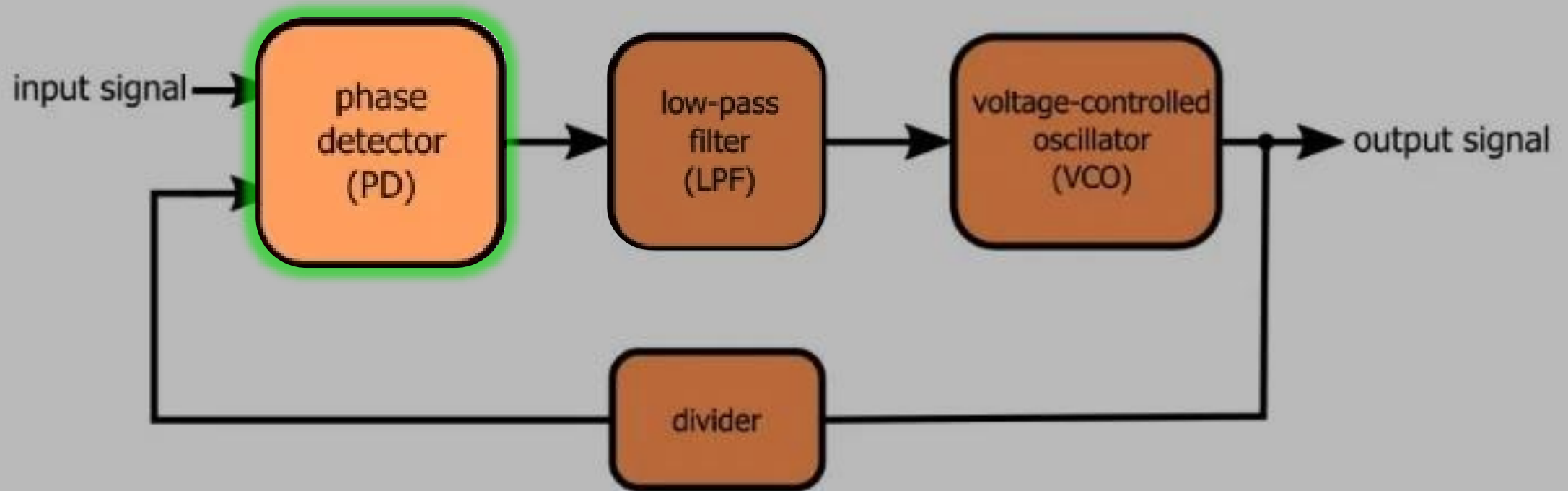


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Phase Locked Loop(PLL)

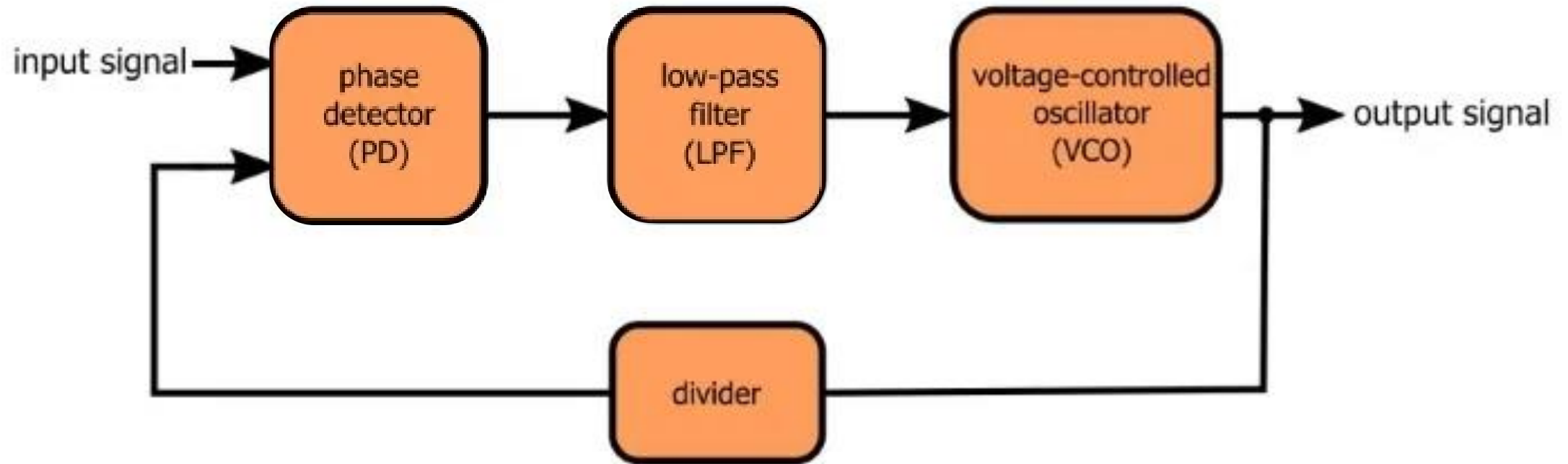


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Phase Locked Loop(PLL)

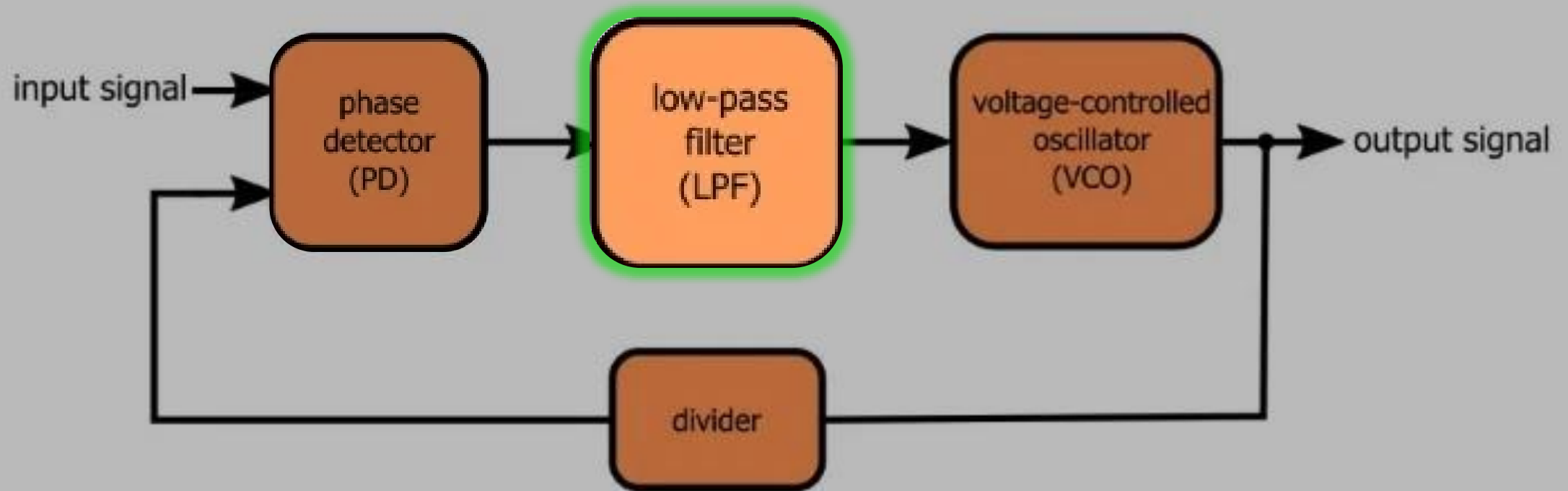


Figure 6: PLL Block Diagram
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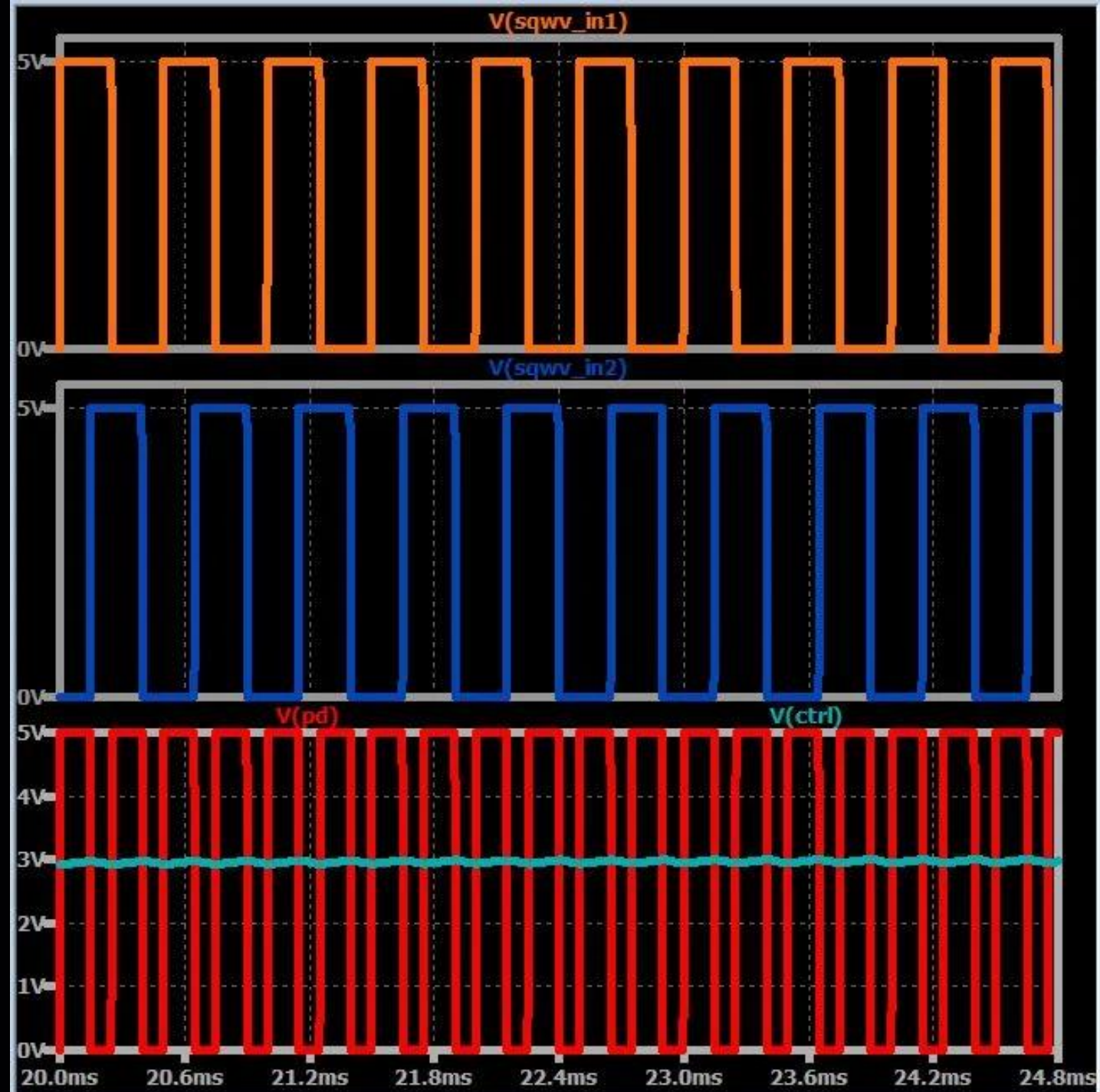


Figure 8: Voltage After
Filtering
Source: [6]

Phase Locked Loop(PLL)

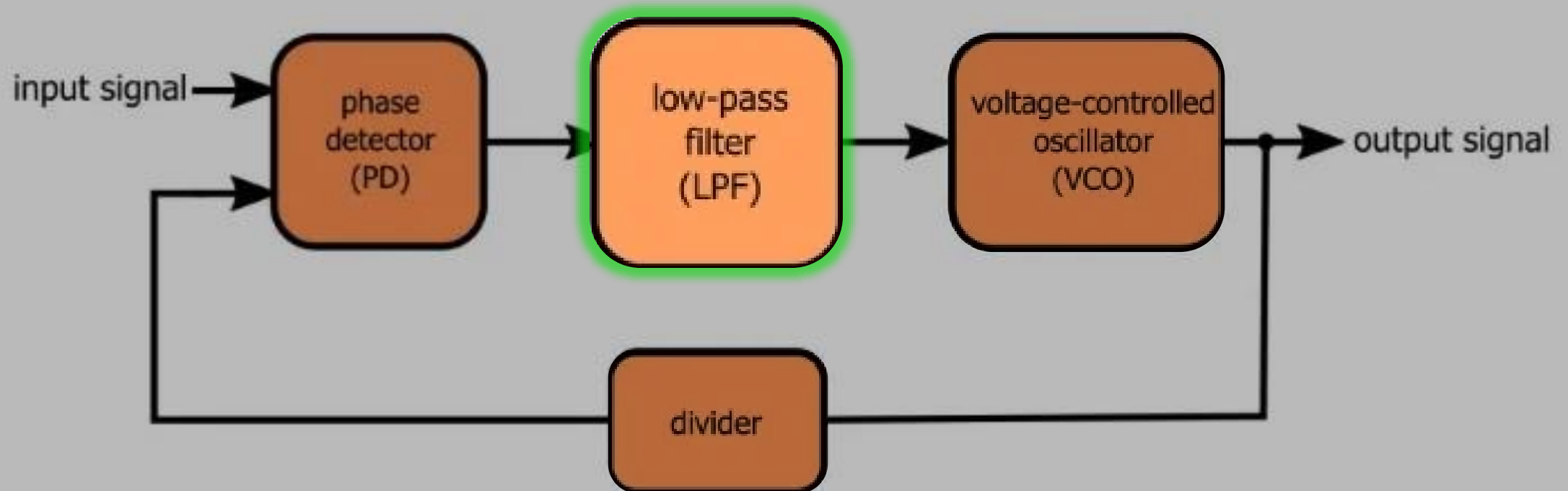


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Phase Locked Loop(PLL)

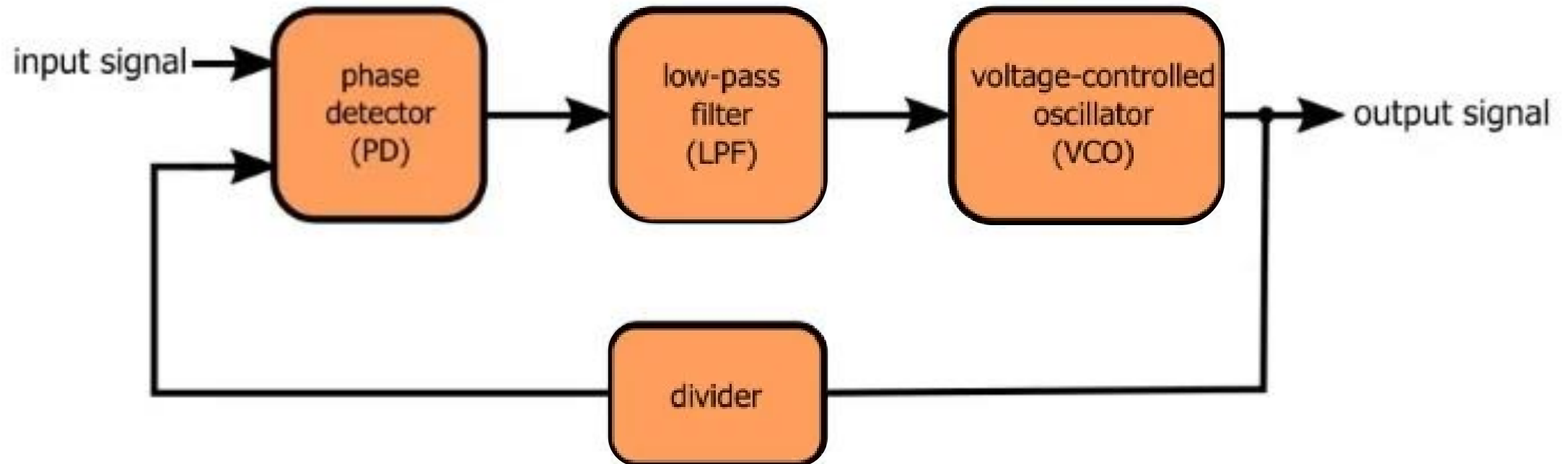


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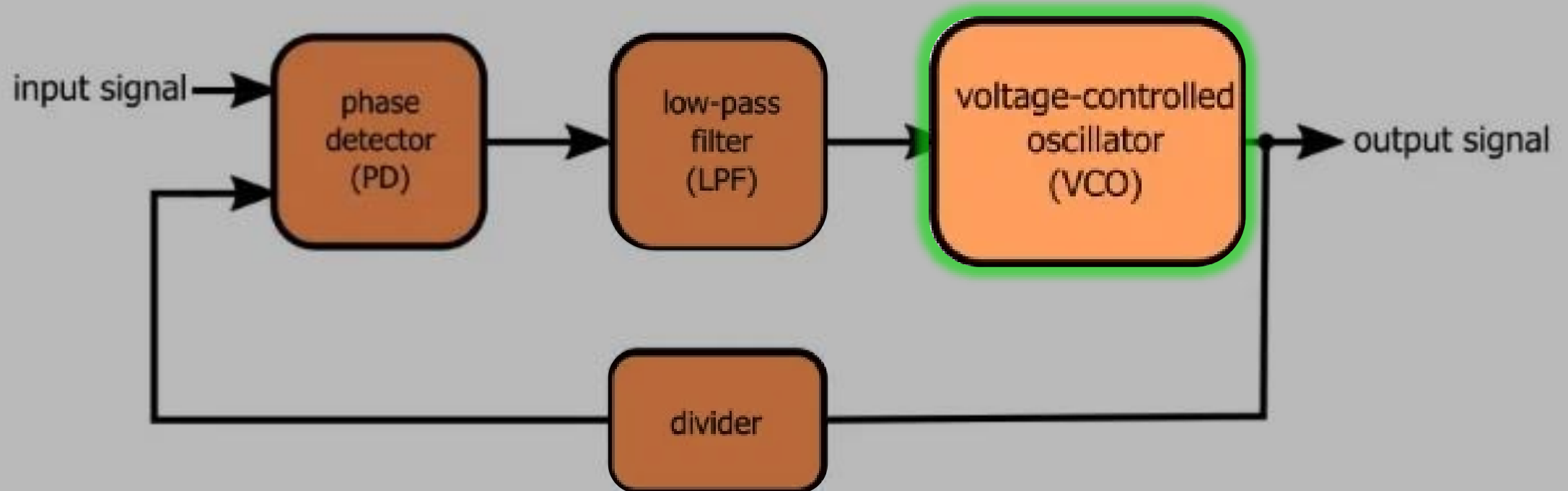


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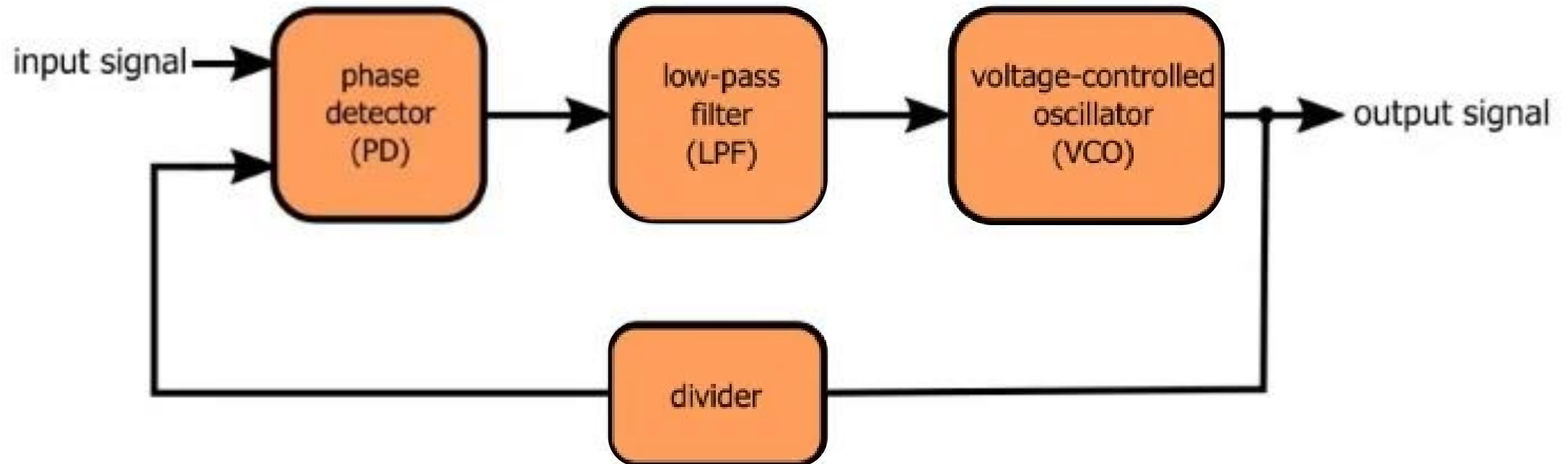


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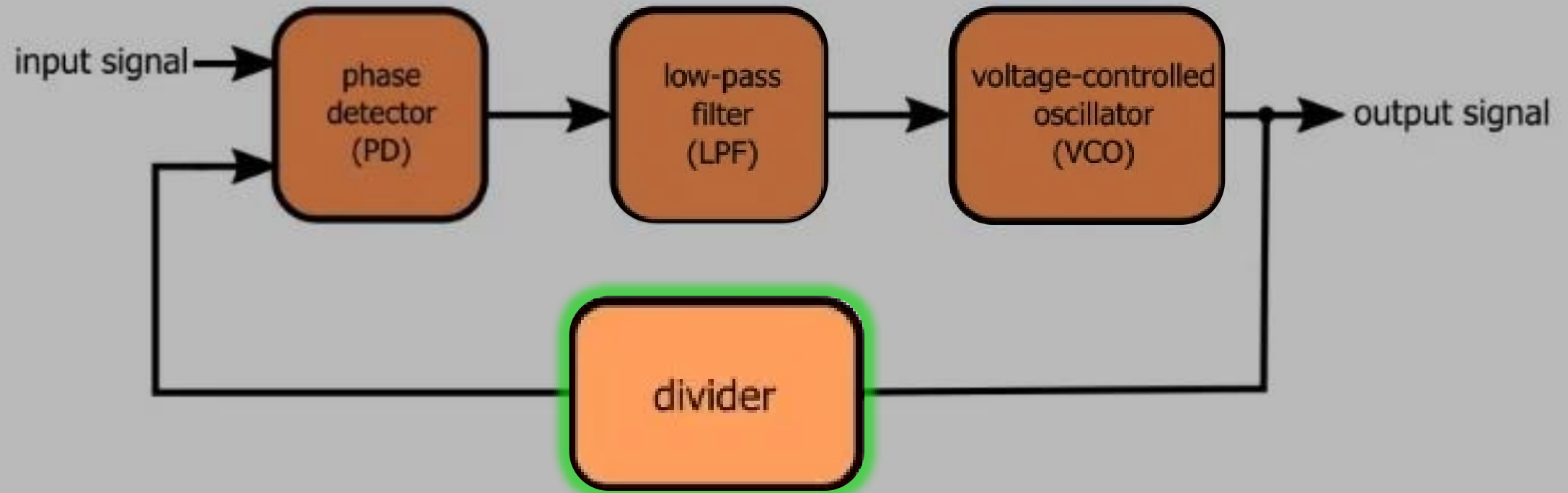


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Voltage Divider

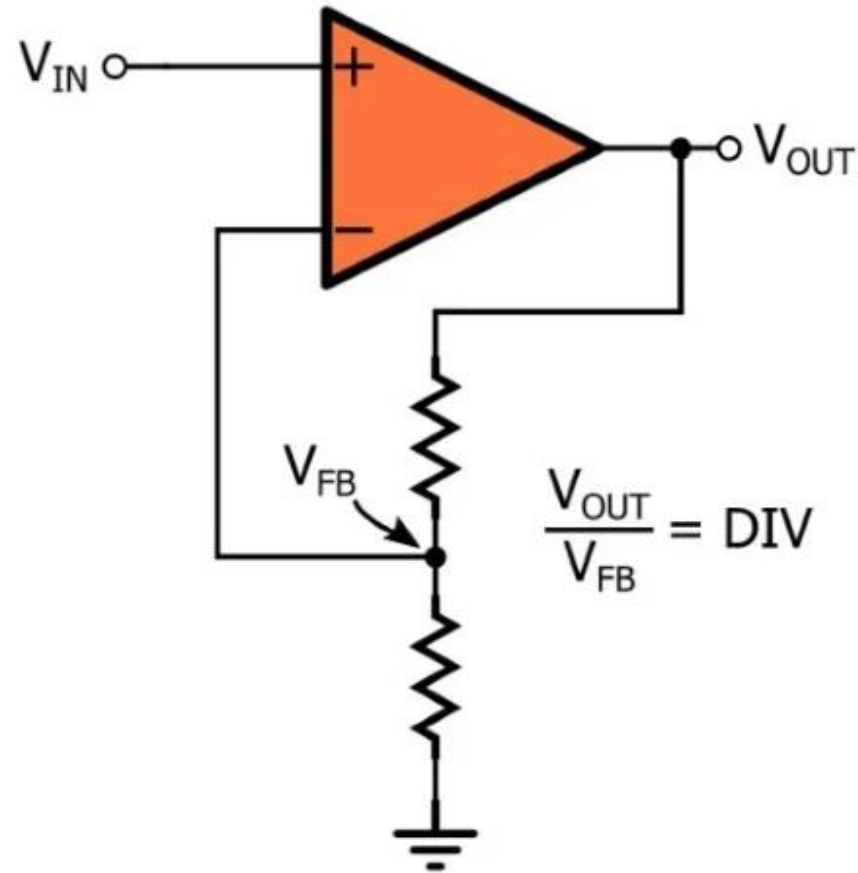


Figure 9: Voltage Divider Circuit
Source: [5]

Voltage Divider

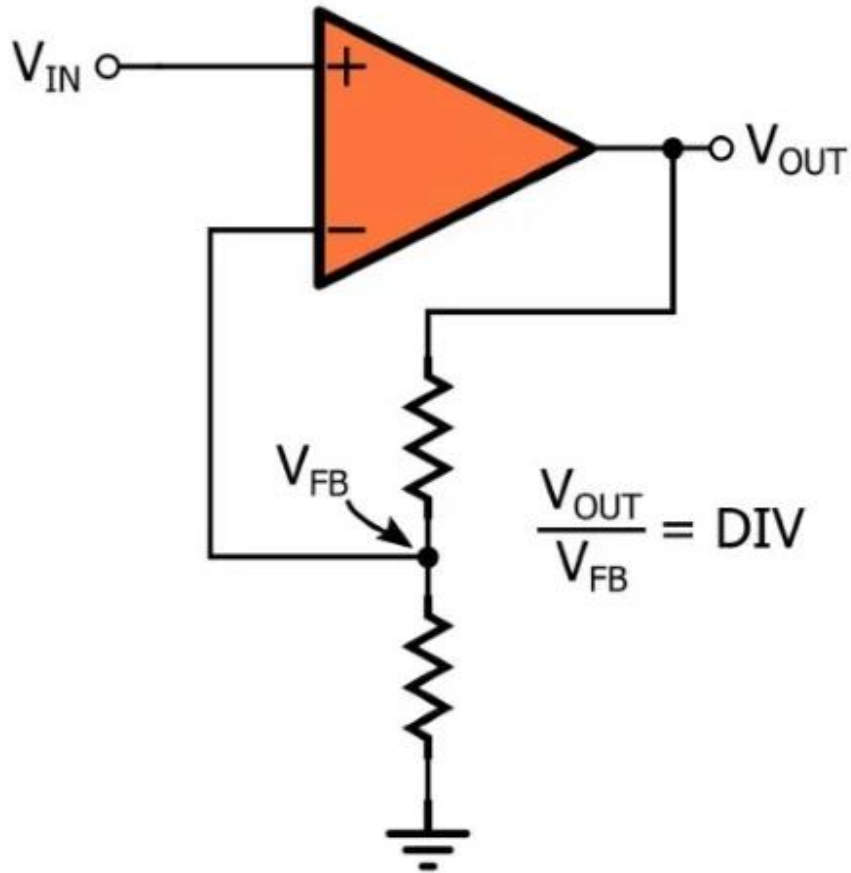


Figure 9: Voltage Divider Circuit
Source: [5]

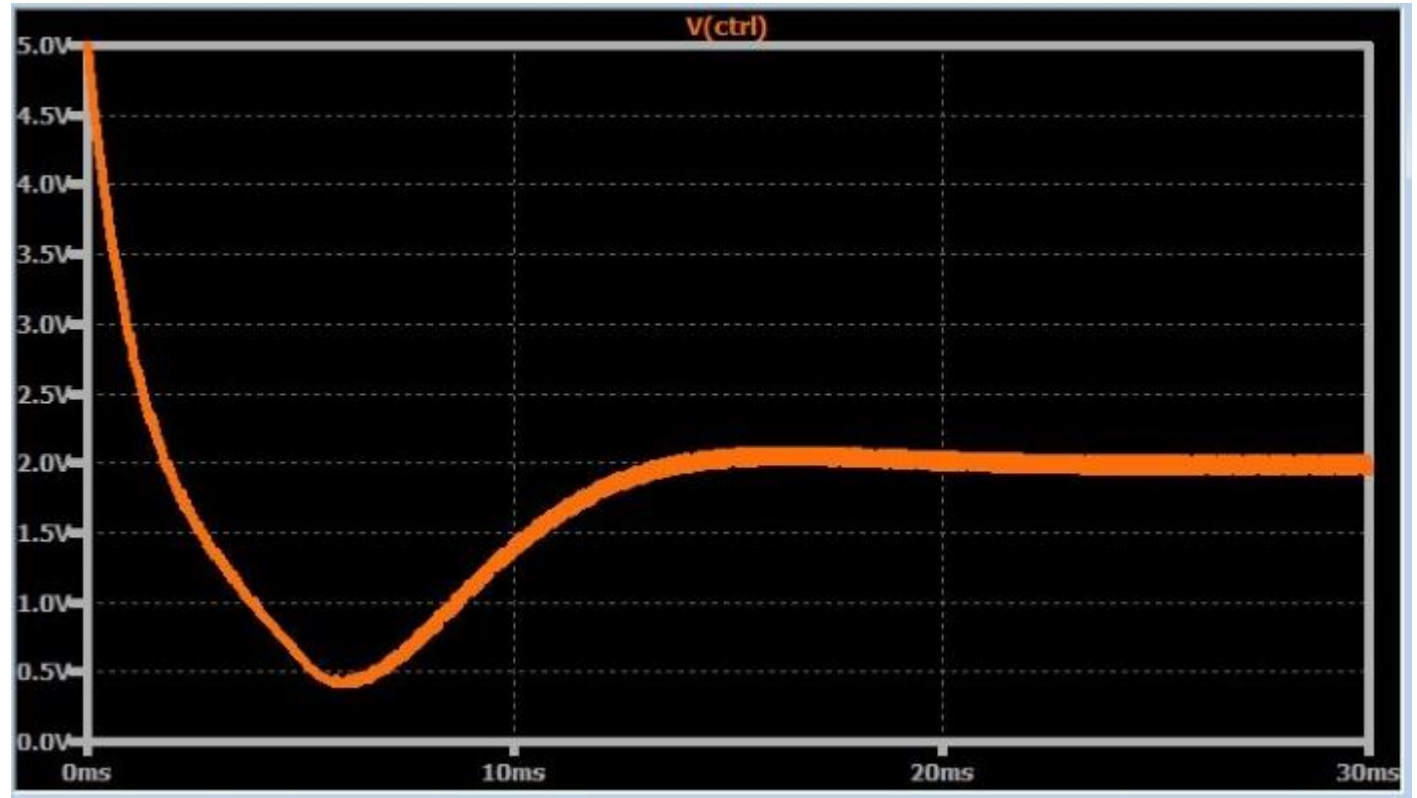


Figure 10: Transient Response Before Division
Source: [8]

Voltage Divider

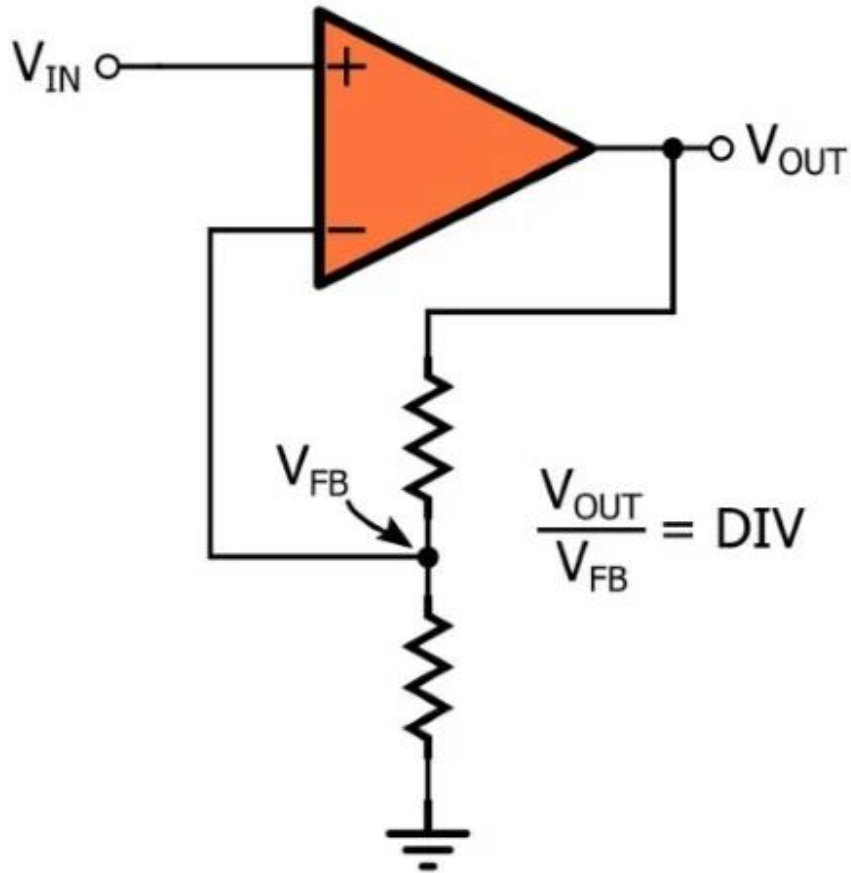


Figure 9: Voltage Divider Circuit
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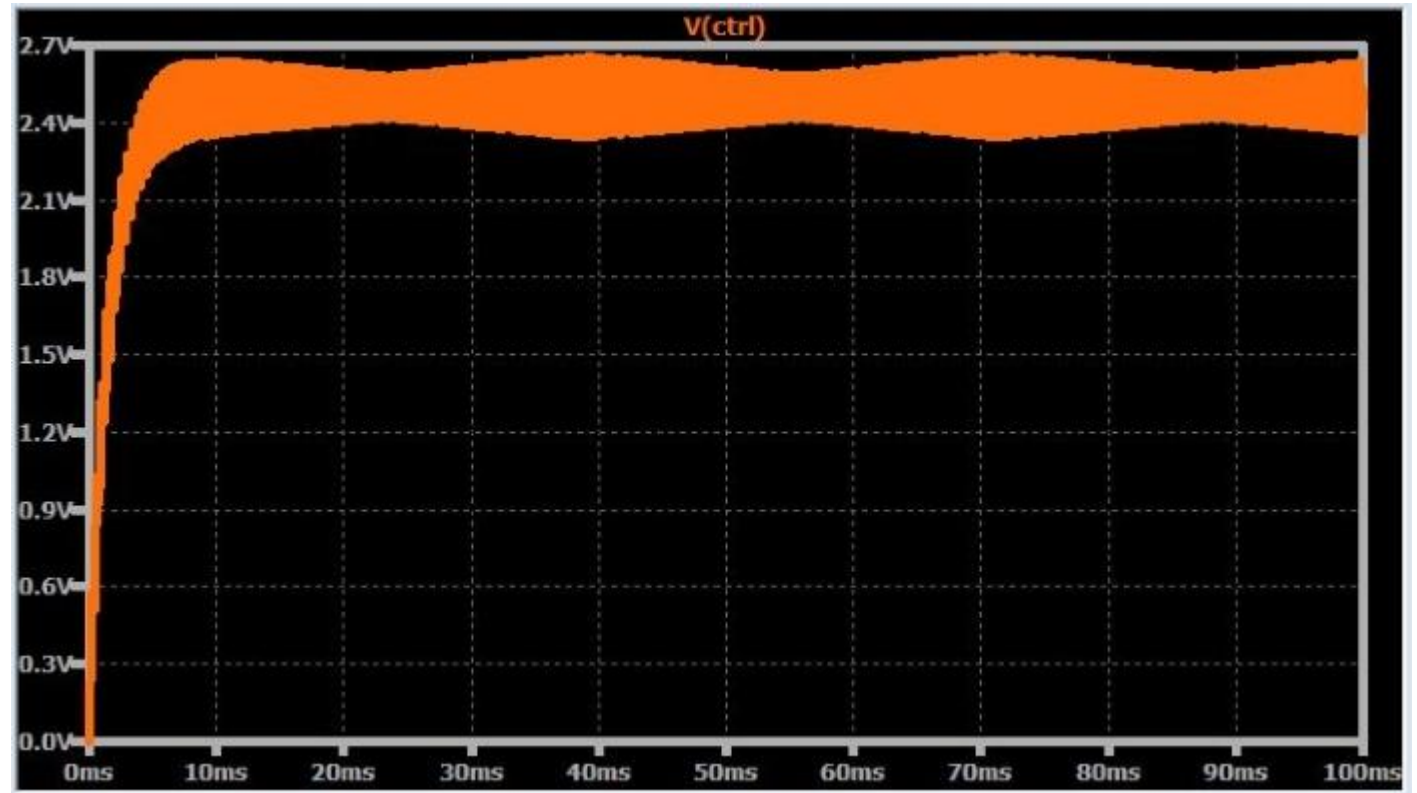


Figure 11: Transient Response After Division
Source: [8]

Did it Help?

- DW3000 collects timestamps at a rate of 125 MHz
- Or every 8 ns
- Error of up to 2.398 m
- Still too much

First Path Estimation

- DW3000 sampling frequency provided by the internal PLL is ≈ 64 GHz

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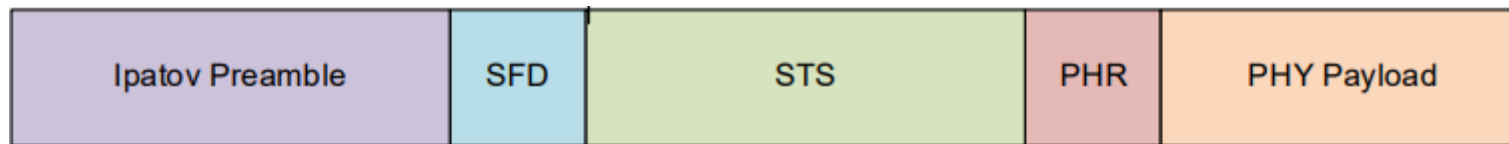


Figure 12: Data Format
Source: [11]

First Path Estimation

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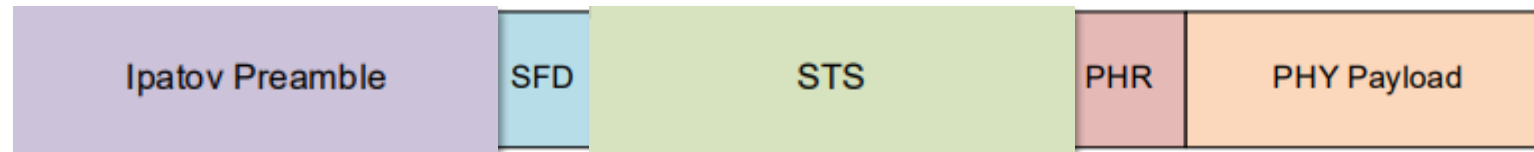


Figure 12: Data Format
Source: [11]

- Preamble and STS are known sequences
- Data points are accumulated at 64 GHz
- Two Channel impulse responses(CIR) are calculated
- The CIR of both the preamble and STS are run through a channel impulse analyzer(CIA) algorithm to find the first path

Final procedure

- Clocks are synchronized
- Robot sends message and logs timestamp
- Beacon receives message gathers rough timestamp and two CIRs
- First path estimation occurs
- Beacon sends a message with the timestamp information
- Robot receives message gathers rough timestamp and two CIRs
- First path estimation occurs
- Antenna delay is subtracted from total time
- Processing time of the beacon is subtracted from total time
- Total time is divided by two
- Final time is multiplied by the speed of light

Sources

- [1] GISGeography, “Trilateration vs Triangulation - How GPS Receivers Work - GIS Geography,” *GIS Geography*, Mar. 04, 2019. [Online]. Available: <https://gisgeography.com/trilateration-triangulation-gps/>
- [2] “Trilateration - GIS Wiki | The GIS Encyclopedia,” *wiki.gis.com*. [Online]. Available: <https://wiki.gis.com/wiki/index.php/Trilateration#:~:text=Trilateration%20is%20a%20method%20for>. [Accessed: Mar. 14, 2023]
- [3] “Pozyx Academy | How ultra-wideband works,” *www.pozyx.io*. [Online]. Available: <https://www.pozyx.io/pozyx-academy/how-does-ultra-wideband-work>. [Accessed: Mar. 14, 2023]
- [4] EETimes, “Why Such Uproar Over Ultrawideband?,” *EE Times*, Mar. 01, 2002. [Online]. Available: <https://www.eetimes.com/why-such-uproar-over-ultrawideband/#:~:text=Carefully%20implemented%2C%20UWB%20is%20also>. [Accessed: Mar. 16, 2023]
- [5] R. Keim, “Understanding PLL Applications: Frequency Multiplication,” *AllAboutCircuits.com*, Mar. 26, 2018. [Online]. Available: <https://www.allaboutcircuits.com/technical-articles/understanding-pll-applications-frequency-multiplication/#:~:text=With%20a%20PLL%20the%20multiplication,generated%20from%20one%20oscillator%20circuit..> [Accessed: Mar. 16, 2023]
- [6] R. Keim, “What Exactly Is a Phase-Locked Loop, Anyways?,” *AllAboutCircuits.com*, Mar. 09, 2018. [Online]. Available: <https://www.allaboutcircuits.com/technical-articles/what-exactly-is-a-phase-locked-loop-anyways/#:~:text=Hence%20the%20low%20pass%20filter,oscillator%20controlled%20by%20a%20voltage..> [Accessed: Mar. 16, 2023]
- [7] “How UWB Works | FiRa Consortium,” *www.firaconsortium.org*. [Online]. Available: <https://www.firaconsortium.org/discover/how-uwb-works>. [Accessed: Mar. 17, 2023]
- [8] R. Keim, “PLL Frequency Multiplication: Transient Response and Frequency Synthesis,” *AllAboutCircuits.com*, Mar. 29, 2018. [Online]. Available: <https://www.allaboutcircuits.com/technical-articles/pll-frequency-multiplication-transient-response-frequency-synthesis/>. [Accessed: Mar. 18, 2023]
- [9] “IEEE Standard for Low-Rate Wireless Networks--Amendment 1: Enhanced Ultra Wideband (UWB) Physical Layers (PHYs) and Associated Ranging Techniques,” doi: <https://doi.org/10.1109/ieeestd.2020.9179124>.
- [10] “DW3000 Datasheet,” *Qorvo.com*. [Online]. Available: <https://www.qorvo.com/products/d/da008142>. [Accessed: Mar. 18, 2023]
- [11] “DW3000 User Manual,” *Qorvo.com*. [Online]. Available: <https://www.qorvo.com/products/d/da008154>. [Accessed: Mar. 18, 2023]