# Hobby-Project-CWDL-2024- IIIT-Bangalore

Github Repo:
https://github.com/Haxous742/Verilog-Projects/tree/main/Square_wave_assignment

Roll Number: BT2024268

Memo Title: Project#2: Verilog Block

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## Overview-

This project implements a Verilog module "square_wave_gen" that generates two square waves with a 90-degree phase difference, along with a testbench "tb_square_wave_gen" to simulate and verify its behavior. The square waves are generated using a 2-bit counter driven by a clock signal, and an active-high reset signal ensures initialization. The output frequency of the square waves is 1 MHz when driven by a 4 MHz clock.

## Files-

- square_wave_gen.v: The main module that generates two square waves.
- tb_square_wave_gen.v: The testbench module to simulate and verify the functionality of square_wave_gen.

## Functionality of (square_wave_gen.v)-

The square_wave_gen module generates two square wave signals (out1 and out2) with a 90-degree phase difference. It operates as follows:

**Inputs and Outputs**

- **Inputs**:
  - clk: The input clock signal (4 MHz in the testbench).
  - reset: Active-high reset signal to initialize the counter and outputs to 0.
- **Outputs**:
  - out1: The first square wave, high for the first half of the period.
  - out2: The second square wave, high for the second and third quarters of the period (90-degree phase shift relative to out1).

**Internal Logic**

- A 2-bit counter (counter) increments from 0 to 3 on each positive clock edge when reset = 0.
- When reset = 1, the counter resets to 0, and both outputs are set to 0.
- The outputs are defined using combinational logic in an always @(*) block:
  - out1 is high when counter < 2 (i.e., counter = 0 or 1).
  - out2 is high when counter == 1 || counter == 2.
- The counter creates a 4-cycle period (since it counts from 0 to 3), and the outputs have a 50% duty cycle (high for 2 cycles, low for 2 cycles).

**Why the Output Frequency is 1 MHz**

- The testbench provides a 4 MHz clock (period = 250 ns, as defined by forever #125 clk = ~clk).
- The 2-bit counter completes one full cycle (0 to 3) in 4 clock cycles:

- Total period = 4×250ns=1000 ns=1µs.

- The frequency of the square waves is the inverse of the period:
  - Frequency = 1/1µs=1MHz.
- Thus, both out1 and out2 have a frequency of 1 MHz, with out2 lagging out1 by one clock cycle (250 ns), which is a 90-degree phase shift (14×360∘=90∘).

## ***Functionality of (tb_square_wave_gen.v)-***

The testbench tb_square_wave_gen simulates the square_wave_gen moduleby providing clock and reset stimuli and generating a waveform file for verification.

**Key Features**

- **Clock Generation**:
  - Generates a 4 MHz clock (250 ns period) by toggling clk every 125 ns (forever #125 clk = ~clk).
- **Reset Sequence**:
  - 0–500 ns: reset = 1 (initial reset).
  - 500–4500 ns: reset = 0 (observe 4 periods of square waves).
  - 4500–5500 ns: reset = 1 (second reset).
  - 5500–9500 ns: reset = 0 (observe another 4 periods).
  - 9500 ns: Simulation ends ($finish).
- **Waveform Dumping**:
  - Dumps all signals to square_wave.vcd using $dumpfile and $dumpvars fo r visualization in GTKWave.

## ***Simulation_Instructions-***

1. Compile the Verilog files:
   iverilog -o testbench tb_square_wave_gen.v square_wave_gen.v
2. Run the simulation:

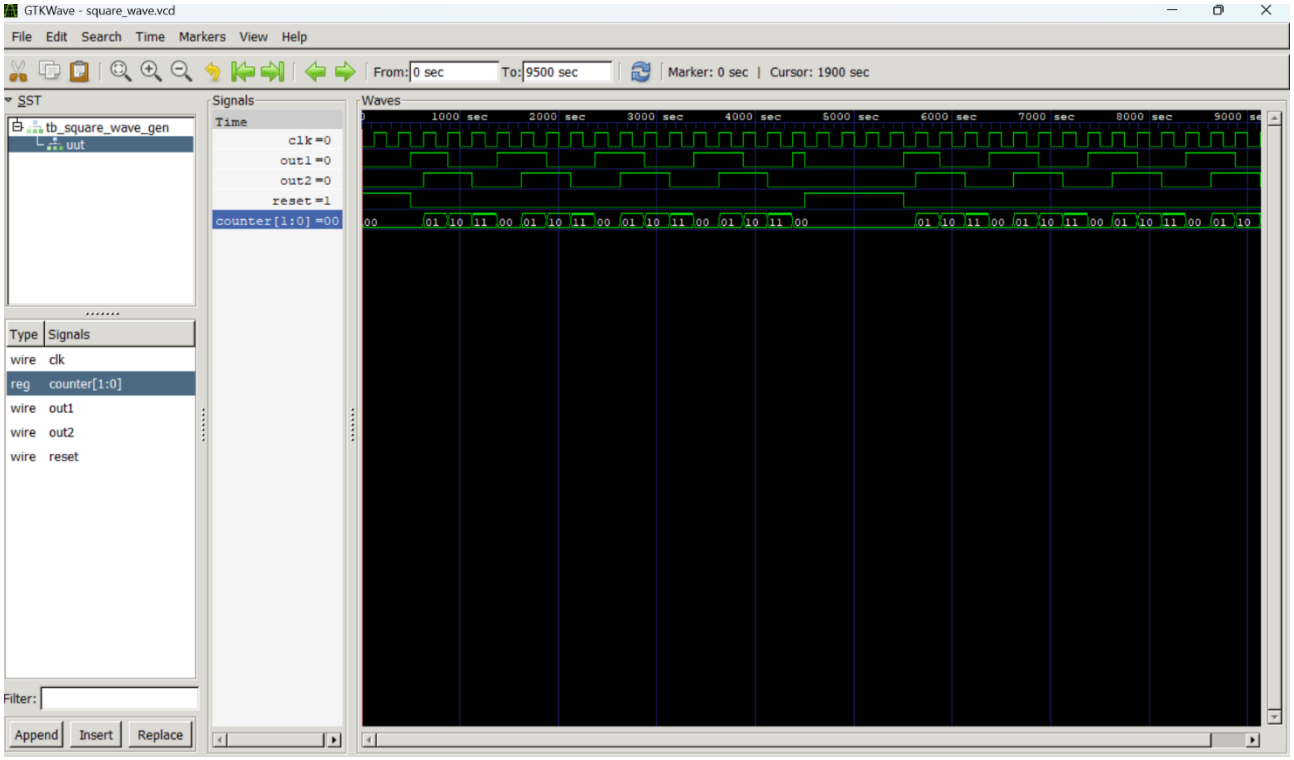
   vvp testbench
3. View the waveforms:

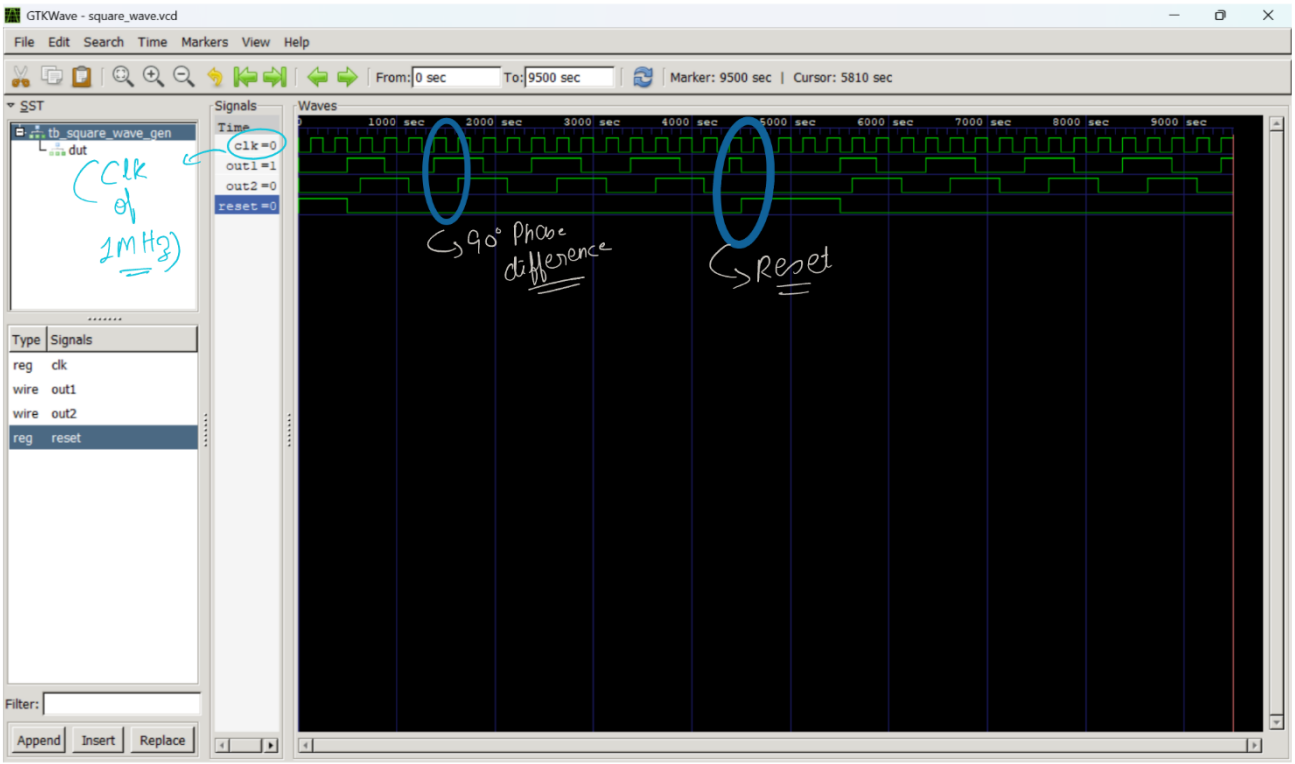
   gtkwave square_wave.vcd

## ***Waveform Analysis-***

In GTKWave, you'll observe:

- **Clock (clk)**: 4 MHz (250 ns period).
- **Counter**: Increments from 0 to 3 every 4 clock cycles (1000 ns period).
- **out1**: High for counter = 0, 1 (500 ns), low for counter = 2, 3 (500 ns), frequency = 1 MHz.
- **out2**: High for counter = 1, 2 (500 ns, shifted by 250 ns), low for counter = 0, 3, frequency = 1 MHz.
- **Reset Behavior**: Outputs are 0 and counter resets to 0 when reset = 1.


GTKWave - square_wave.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 9500 sec
Marker: 0 sec | Cursor: 1900 sec
SST
tb_square_wave_gen
uut
Signals
Time
clk =0
out1 =0
out2 =0
reset =1
counter[1:0] =00
Waves
1000 sec
2000 sec
3000 sec
4000 sec
5000 sec
6000 sec
7000 sec
8000 sec
9000 sec
Type Signals
wire clk
reg counter[1:0]
wire out1
wire out2
wire reset
Filter:
Append
Insert
Replace


GTKWave - square_wave.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 9500 sec
Marker: 9500 sec | Cursor: 5810 sec
SST
tb_square_wave_gen
dut
Clk of 1MHz
Signals
Time
clk =0
out1 =1
out2 =0
reset =0
Waves
1000 sec
2000 sec
3000 sec
4000 sec
5000 sec
6000 sec
7000 sec
8000 sec
9000 sec
90° Phase difference
Reset
Type Signals
reg clk
wire out1
wire out2
reg reset
Filter:
Append
Insert
Replace