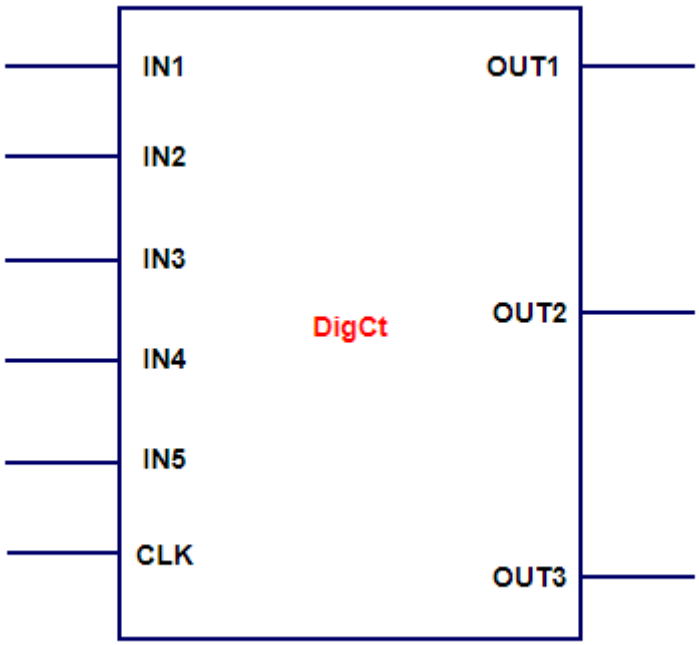
Assignment 2.1

introduction: -

The target of this assignment is to modify in your assignment 1 code based on blocking and Non-blocking concept we are discussed in session 2 to describe all the flops using only 1 always block and capture every combinational cloud drive a flop with only 1 always block. So finally, your code has to optimized to contain only 4 always blocks.

Block Interface

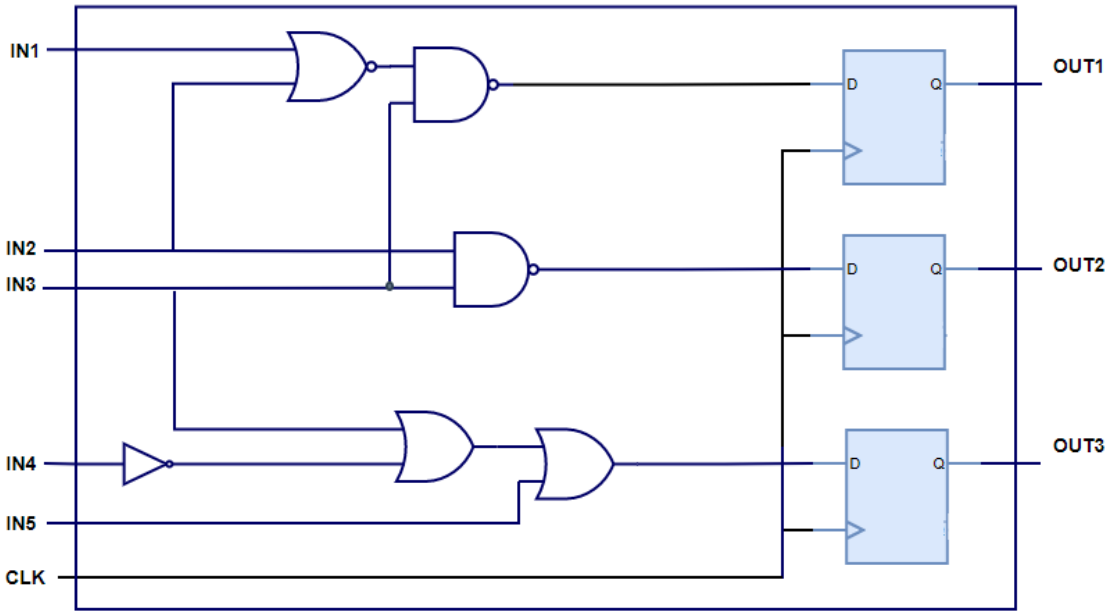


Block(Module) Name: DigCt

Inputs: IN1, IN2, IN3, IN4, CLK (all inputs of 1-bit width)

Outputs: OUT1, OUT2, OUT3 (output of 1-bit width)

Circuit Implementation: -



Requirements: -

- Design the above circuit using Verilog language.