Notes:

1. In the lab writeup you are given the following table:

Table 1: Register contents and control signals for computing $A^2 + C$

	Reset	1	2	3	4	5	6	7	
data_in		5	4	3	2	2	2	2	
RA		0	5	5	5	5	25	25	
RB		0	0	4	4	4	4	4	
RC		0	0	0	3	3	3	3	
Rx		0	0	0	0	2	2	2	
RR		0	0	0	0	0	0	28	
ld_a		1	0	0	0	1	0	1	
ld_b		0	1	0	0	0	0	0	
ld_c		0	0	1	0	0	0	0	
ld_x		0	0	0	1	0	0	0	
ld_alu_out		0	0	0	0	1	0	0	1 = select alu output
alu_select_a		0	0	0	0	0	0	0	0 = select A
alu_select_b		0	0	0	0	0	2	0	2 = select C
alu_op		0	0	0	0	1	0	0	0 = add, 1 = multiply
ld_r		0	0	0	0	0	1	0	

This table shows you the steps taken in the circuit. The top line is the step (clock) number.
The next section has the various registers and their contents for 5*5+3. So when the data in is 5, RA will get a 5 at the second step. RR gets the value of 28=A*A+C at step 7. Often we call this the data path.
The next section, below the double line, shows the control signals involved and their values at each step. For example, at step 1 ld_a=1 and ld_alu_out=0 to cause the load of data_in into RA. You will need to look at the diagram of the circuit on page 7 of the lab to see this. This is called the control path, since it controls the flow of the data. The control signals are set up before the clock edge where they take effect on the data.

So for each step here is what is happening in this example:

Step	Data changes	Control changes to set up for next clock
1		Select data_in (currently 5) to RA input
2	RA gets data_in.	data_in is changed to 4. Select data_in to RB
3	RB gets data_in.	data_in is changed to 3. Select data_in to RC
4	RC gets data_in	data_in is changed to 2. Select data_in to Rx
5	Rx gets data_in.	Select A goes to both sides of ALU. control ALU to multiply the two inputs (calculating A*A in this case) Select ALU result to A (to overwrite what is currently in A)
6	RA gets A*A from ALU	Select RA and RC to ALU control ALU to do an add Select to load result into RR
7	RR gets result	