```
module ALU (SW, KEY, LEDR, HEXO, HEX1, HEX2, HEX3, HEX4, HEX5);
          input [7:0] SW;
         input [2:0] KEY;
output [7:0] LEDR;
output [6:0] HEXO, HEX1, HEX2, HEX3, HEX4, HEX5;
 3
 4
 5
6
7
          // For ease of readability
         wire [3:0] A, B;
 8
         wire [2:0] K;
 9
         wire [4:0] addOut;
10
         assign A = SW[7:4];
assign B = SW[3:0];
11
12
13
         assign K = \sim KEY;
14
          // Calculates sum for the ALU
         FARip4b a1(SW[7:0],
addOut[4:0]);
15
16
17
          // Stores our ouput value
18
          reg [7:0] ALUout;
19
20
          always @(*)
21
         begin
22
             case (K)
23
                 // Case 0
3'b000: ALUout = addOut;
24
25
                 // Case 1
                  b001: ALUout = A + B;
26
27
                 // Case 2
                 3'b010: begin
28
                    ALUout[7:4] = \sim (A \& B);
ALUout[3:0] = \sim (A \land B);
29
30
31
                    end
32
                 // Case 3
                 3'b011: begin
33
                    if (|{A, B})
34
35
                        ALUout = 8'b00001111;
36
37
                        ALUout = 8'b0;
38
                    end
39
                 // Case 4
                 3'b100: begin
40
41
                     42
                        ALUout = 8'b1110000;
43
                        ALUout = 8'b0;
44
45
                    end
46
                 // Case 5
                 3'b101: ALUout = {A, ~B};
47
48
                 // Default case
                 default: ALUout = 8'b00000000;
49
50
             endcase
51
         end
52
          // Assign results to appropraite displays/LEDs
53
          assign LEDR[7:0] = ALUout;
54
         HexDecoder \bar{h}0 (\bar{S}W[3:0], HEXO);
         HexDecoder h1 (SW[7:4], HEX2);
55
56
                           (4'b0000, HEX1);
         HexDecoder h2
         HexDecoder h3 (4'b0000, HEX3);
HexDecoder h4 (ALUout[3:0], HEX4);
57
58
59
         HexDecoder h5 (ALUout[7:4], HEX5);
60
      endmodule
61
62
      module FARip4b (In, Out);
63
64
          input [7:0] In;
65
         output [4:0] Out;
66
         wire w1, w2, w3;
67
68
         FA u0 (.in1(In[4]), .in2(In[0]), .cin(1'b0),
         .s(Out[0]), .cout(w1));

FA u1 (.in1(In[5]), .in2(In[1]), .cin(w1), .s(Out[1]), .cout(w2));

FA u2 (.in1(In[6]), .in2(In[2]), .cin(w2),
69
70
71
73
                   s(Out[2]), .cout(w3))
74
          FA u3 (.in1(In[7]), .in2(In[3]),
                                                  .cin(w3),
75
                  .s(Out[3]), .cout(Out[4]) );
76
      endmodule
```

```
78
        module FA (input in1, in2, cin,
             output s, cout);
assign s = in1 \( \) in2 \( \) cin;
 79
 80
             assign cout = (in1 & in2) | (in1 & cin) | (in2 & cin);
 81
         endmodule
 82
 83
 84
        module HexDecoder (In, HEX);
 85
             input [3:0]_In;
             output [6:0] HEX;
// For ease of readability
 86
 87
             assign c0 = In[0];
 88
 89
             assign c1 = In[1];
 90
             assign c2 = In[2];
 91
             assign c3 = In[3];
 92
 93
             assign HEX[0] = (-c3 \& -c2 \& -c1 \& c0) + (-c3 \& c2 \& -c1 \& -c0) + (c3 \& -c2 \& c1 \& c0) +
         (c3 \& c2 \& \sim c1 \& c0);
         assign HEX[1] = (~c3 & c2 & ~c1 & c0) + (~c3 & c2 & c1 & ~c0) + (c3 & ~c2 & c1 & c0) + (c3 & c2 & c1 & c0);
 94
             assign HEX[2] = (-c3 \& -c2 \& c1 \& -c0) + (c3 \& c2 \& -c1 \& -c0) + (c3 \& c2 \& c1 \& -c0) + (
 95
        c3 & c2 & c1 & c0);
    assign HEX[3] = (~c3 & ~c2 & ~c1 & c0) + (~c3 & c2 & ~c1 & ~c0) + (~c3 & c2 & c1 & c0) +
(c3 & ~c2 & ~c1 & c0) + (c3 & ~c2 & c1 & ~c0) + (c3 & c2 & c1 & c0);
    assign HEX[4] = (~c3 & ~c2 & ~c1 & c0) + (~c3 & ~c2 & c1 & c0) +
(~c3 & c2 & ~c1 & c0) + (~c3 & c2 & c1 & c0) +
(~c3 & c2 & ~c1 & c0) + (~c3 & ~c2 & c1 & c0);
 96
 97
             assign HEX[5] = (\sim c3 \& \sim c2 \& \sim c1 \& c0) + (\sim c3 \& \sim c2 \& c1 \& \sim c0) + (\sim c3 \& \sim c2 \& c1 \& c0) +
 98
          (~c3 & c2 & c1 & c0) + (c3 & c2 & ~c1 & c0);

assign HEX[6] = (~c3 & ~c2 & ~c1 & ~c0) + (~c3 & ~c2 & ~c1 & c0) + (~c3 & c2 & c1 & c0) +
 99
          (c3 \& c2 \& \sim c1 \& \sim c0);
100
         endmodule
```

101 102

Page 2 of 2 Revision: ALU