```
1   // Data written to registers R0 to R5 are sent to the H digits
2   module seg7 (Data, Addr, Sel, Resetn, Clock, H5, H4, H3, H2, H1, H0);
3       input [6:0] Data;
4       input [2:0] Addr;
5       input Sel, Resetn, Clock;
6       output [6:0] H5, H4, H3, H2, H1, H0;
7
8       wire [6:0] nData;
9       assign nData = ~Data;
10
11      regne reg_R0 (nData, Clock, Resetn, Sel & (Addr == 3'b000), H0);
12      regne reg_R1 (nData, Clock, Resetn, Sel & (Addr == 3'b001), H1);
13      regne reg_R2 (nData, Clock, Resetn, Sel & (Addr == 3'b010), H2);
14      regne reg_R3 (nData, Clock, Resetn, Sel & (Addr == 3'b011), H3);
15      regne reg_R4 (nData, Clock, Resetn, Sel & (Addr == 3'b100), H4);
16      regne reg_R5 (nData, Clock, Resetn, Sel & (Addr == 3'b101), H5);
17  endmodule
18
19  module regne (R, Clock, Resetn, E, Q);
20      parameter n = 7;
21      input [n-1:0] R;
22      input Clock, Resetn, E;
23      output [n-1:0] Q;
24      reg [n-1:0] Q;
25
26      always @(posedge Clock)
27          if (Resetn == 0)
28              Q <= {n{1'b1}};  // turn OFF all segments on reset
29          else if (E)
30              Q <= R;
31  endmodule
32
```