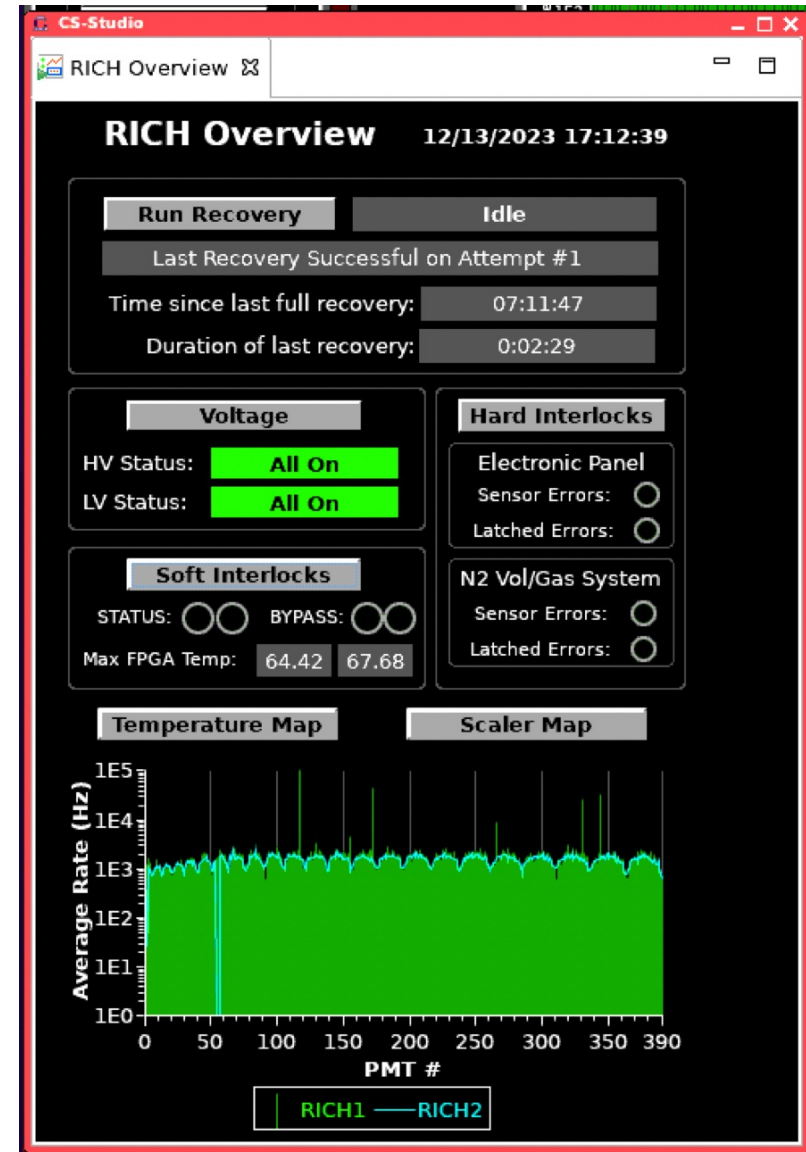


RICH Control Manual

Valery Kubarovsky

January 23, 2024

- RICH front-end is sitting in the beam of the secondary particles. The radiation damage causes the malfunction of FE . Dead tiles appear. The damage is not permanent. It can be recovered by switching LV OFF/ON or reloading the RICH front-end FPGA
- We don't need to perform the RICH full recovery daily any more. DAQ is reloading FPGA memory during prestart automatically
- In case you got RICH alarm do the following:
 1. Continue data taking if DAQ is working.
 2. Start new run with CANCEL-RESET
 3. With high probability the problem will be fixed automatically
 4. If the problem is not solved do RICH full recovery.
 5. If it does not not help call RICH expert

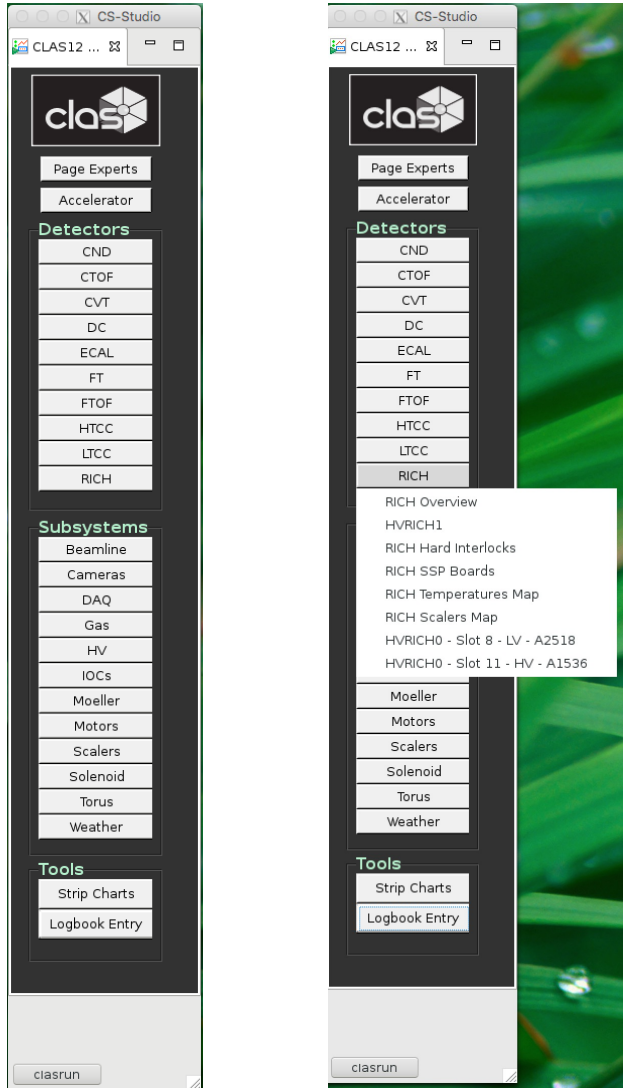


RICH mainframe remote reboot

In case of communication lost with the RICH mainframe try to reboot it remotely

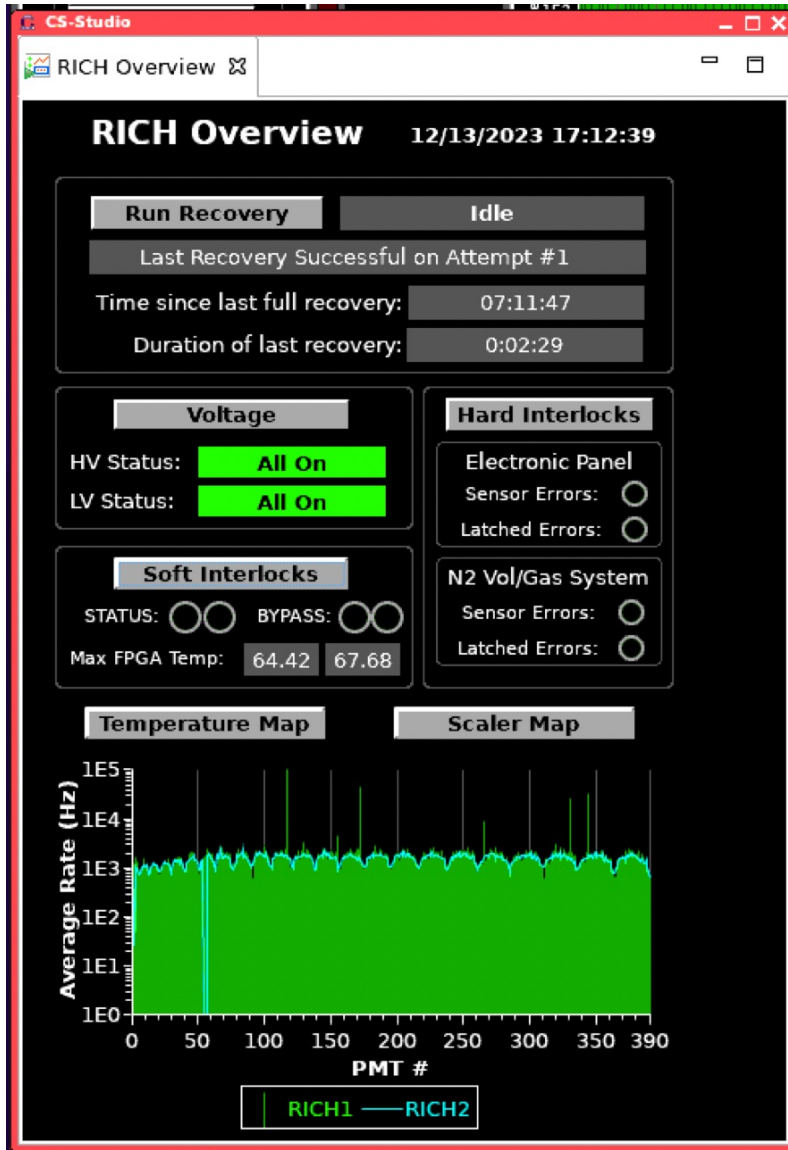
- To reboot only the CPU:
caenhvReset.py --soft hvrich1 (sector 4)
caenhvReset.py --soft hvrich2 (sector 1)
- To power cycle the whole thing, causing all voltages to go to zero:
caenhvReset.py --hard hvrich1 (sector 4)
caenhvReset.py --hard hvrich2 (sector 1)

RICH GUI overview



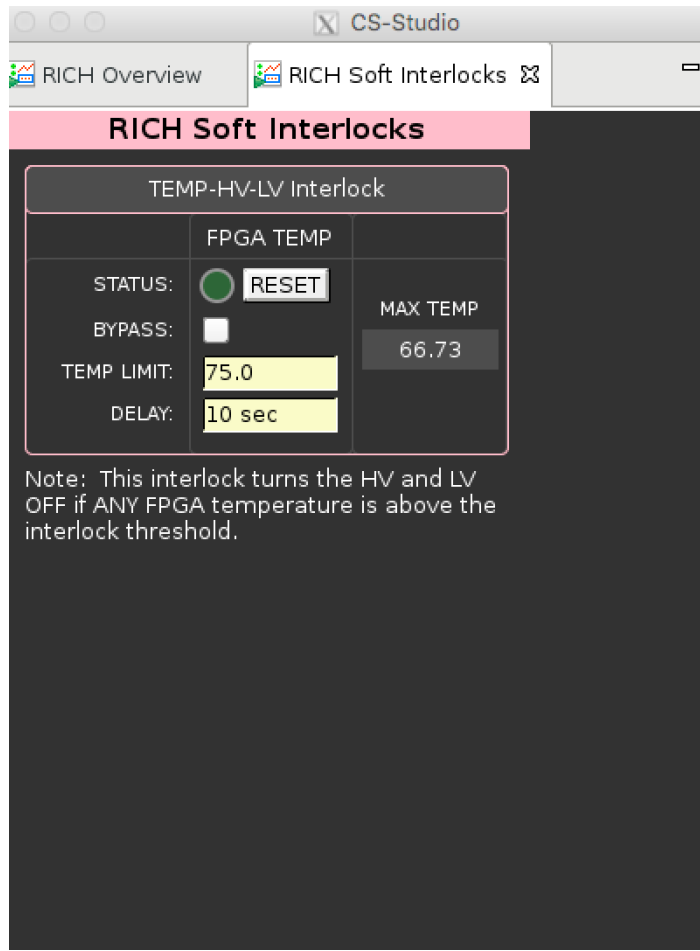
- Press RICH on clascss menu
- Chose RICH Overview

RICH GUI



- **Voltage**
Control RICH HV and LV
- **Temperature Map**
Shows the temperature of the RICH electronic boards
- **Scaler Map**
Presents the rate of the MAPMT pixels
- **Hard Interlock**
Control the RICH interlock
- **Soft Interlock**
Control the max temperature of the FPGA chips

Soft Interlock



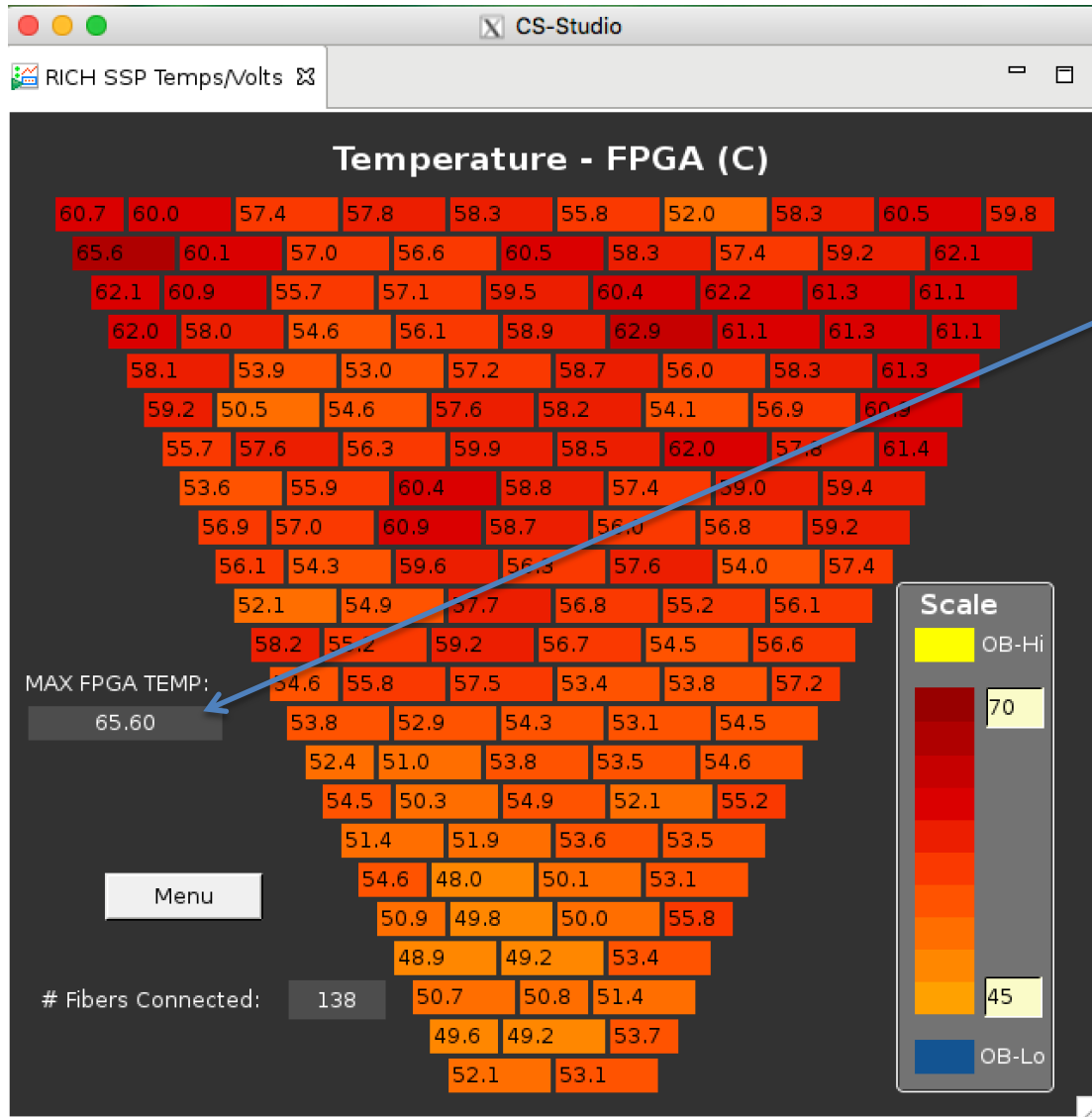
The screenshot shows the CS-Studio interface with the 'RICH Soft Interlocks' window open. The window has a pink header 'RICH Soft Interlocks'. Inside, there is a section titled 'TEMP-HV-LV Interlock'. This section contains a table with the following data:

	FPGA TEMP	
STATUS:	<input checked="" type="radio"/> <input type="radio"/> RESET	
BYPASS:	<input type="checkbox"/>	MAX TEMP
TEMP LIMIT:	75.0	66.73
DELAY:	10 sec	

Below the table, a note states: 'Note: This interlock turns the HV and LV OFF if ANY FPGA temperature is above the interlock threshold.'

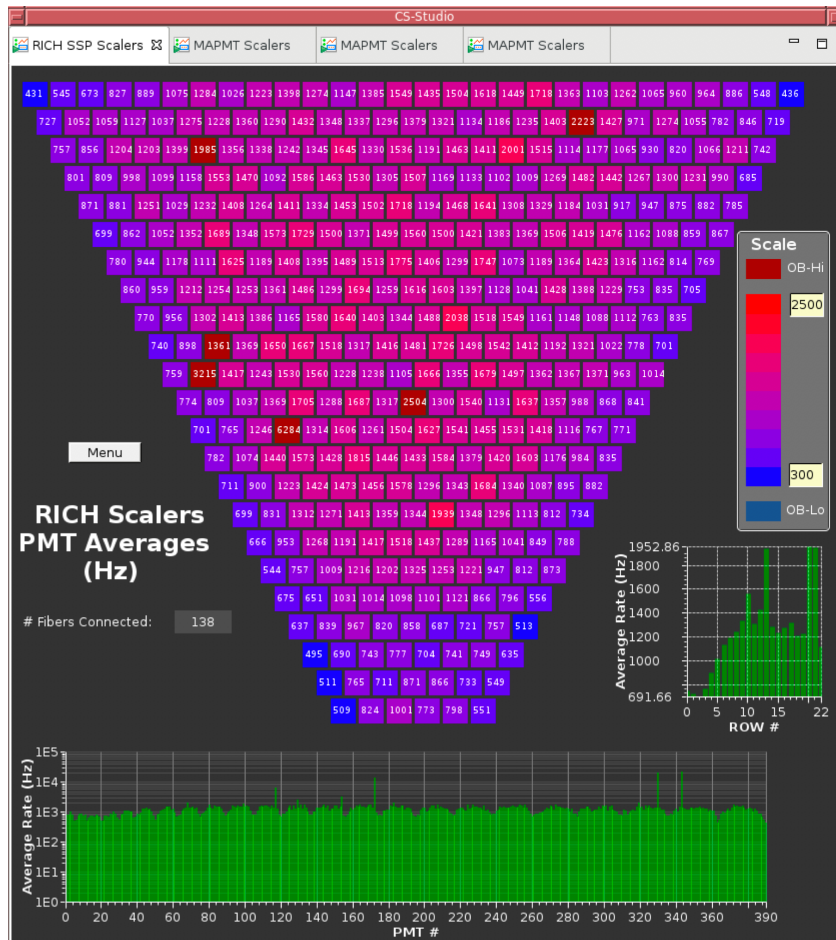
- Max temperature has to be less than 75 C
- Reset the interlock if necessary

Temperature Map

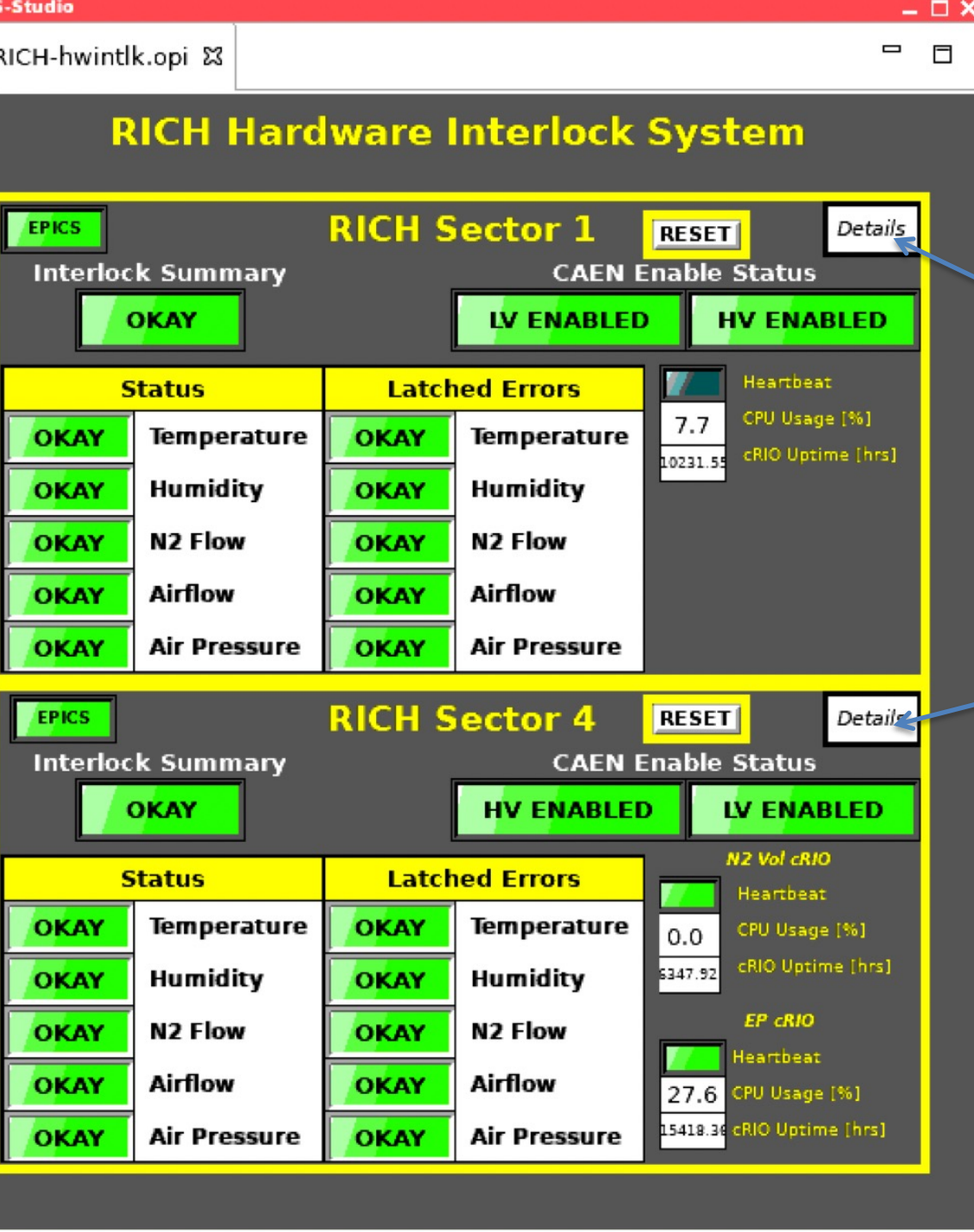


- Max temperature has to be less than 75 C
- Soft interlock switches off The RICH HV and LV if $t > 75^{\circ}\text{C}$
- All tiles have to be present except Tile 21 in sector 1

RICH scalers



- The plot presents the average rate of the MAPMT pixels
- ALL MAPMTs have to be present except Tile 21 in sector 1



- Hard Interlock controls the temperature and humidity inside the RICH detector
- Press this button to view the sector 1 panel
- Press this button to view the sector 4 panel

Electronic Volume Interlock

CS-Studio

RICH_S1_EP.opi

RICH Sector 1 Electronic Panel Interlocks

Detector Interlock Status

Any Interlock Over Limit? **OK**

RICH CAEN HV Enable Status **HV ENABLED**

RICH CAEN LV Enable Status **LV ENABLED**

Air Compressor Status **ON**

Heartbeat

EPICS Control **ENABLED**

Signal Monitoring and Limit Control | Sensor Locations in RICH

Sector 1 Electronic Panel Temperature Interlocks

	Value	Status	Limit Control		Unit	Interlock Status		Latched Errors	
			High	Low		High	Low	High	Low
Temperature 1	32.94	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 2	33.03	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 3	31.90	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 4	34.17	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 5	40.04	ENABLED	46	10	°C	OK	OK	OK	OK
Temperature 6	39.94	ENABLED	46	10	°C	OK	OK	OK	OK
Temperature 7	35.58	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 8	35.52	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 9	39.02	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 10	38.93	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 11	40.27	ENABLED	47	10	°C	OK	OK	OK	OK
Temperature 12	40.16	ENABLED	47	10	°C	OK	OK	OK	OK
Temperature 13	38.15	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 14	38.24	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 15	25.34	ENABLED	45	10	°C	OK	OK	OK	OK
Temperature 16	25.54	ENABLED	45	10	°C	OK	OK	OK	OK

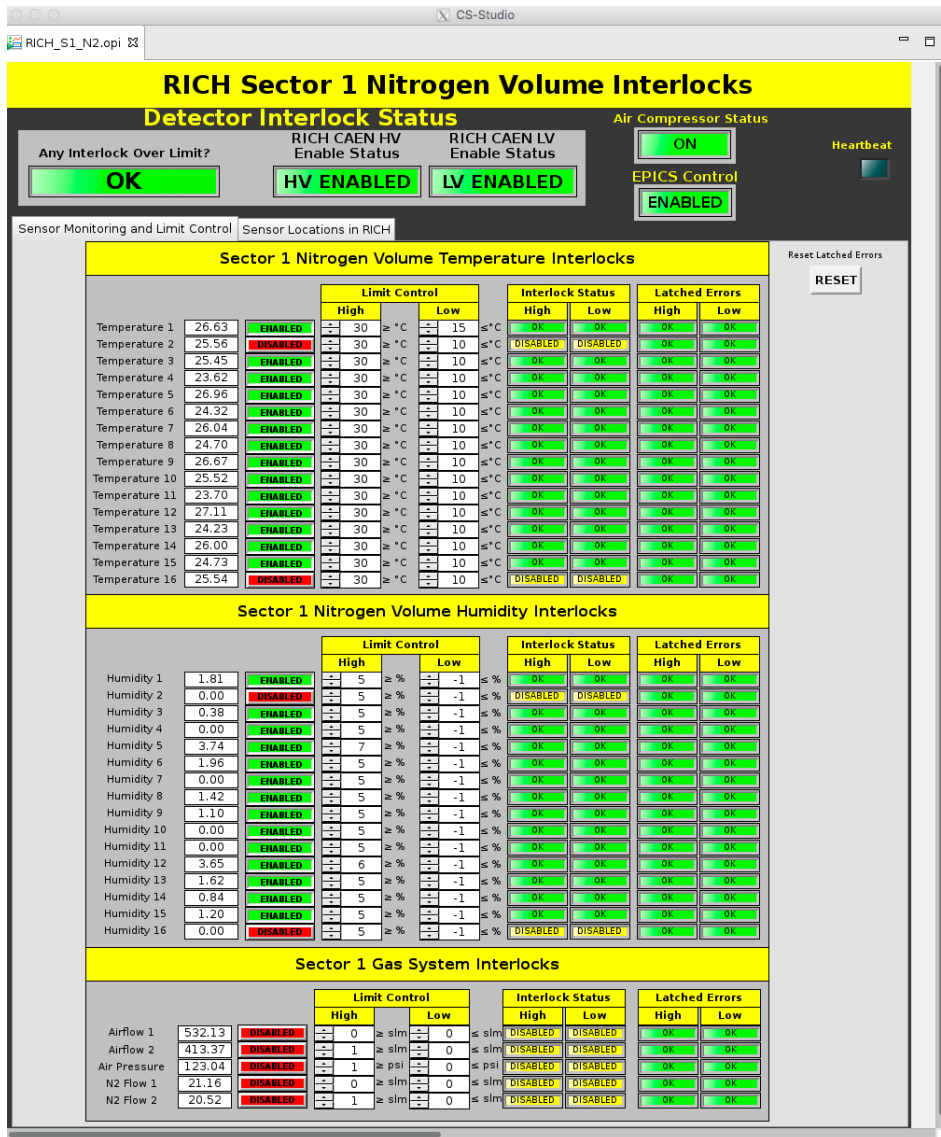
Sector 1 Electronic Panel Humidity Interlocks

	Value	Status	Limit Control		Unit	Interlock Status		Latched Errors	
			High	Low		High	Low	High	Low
Humidity 1	20.92	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 2	21.00	DISABLED	50	0	%	DISABLED	DISABLED	OK	OK
Humidity 3	19.54	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 4	0.00	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 5	0.03	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 6	0.10	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 7	0.44	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 8	0.41	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 9	0.30	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 10	0.22	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 11	0.31	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 12	0.36	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 13	0.11	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 14	0.09	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 15	0.00	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK
Humidity 16	32.69	DISABLED	0	0	%	DISABLED	DISABLED	OK	OK

Reset Latched Errors **RESET**

Check the temperature and humidity

Nitrogen Volume Interlock



Check the temperature and humidity