CLAS 12

Silicon Vertex Tracker Technical Design Report

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Contents

1 Introduction

The electron beam energy of the Continuous Electron Beam Accelerator Facility (CEBAF) is being upgraded to 12 GeV; hence, the CEBAF's Large Acceptance Spectrometer (CLAS) is being upgraded to conduct, at this energy regime, spectroscopic studies of excited baryons and of polarized and unpolarized quark distributions, investigations of the influence of nuclear matter on propagating quarks, and measurements of generalized parton distributions [1]. Figure 1.1 shows a view of the CLAS12 detector. Details of the detector are given in the conceptual design report [1]. This technical design report presents the design details of the Silicon Vertex Tracker (SVT), which is part of the central detector.

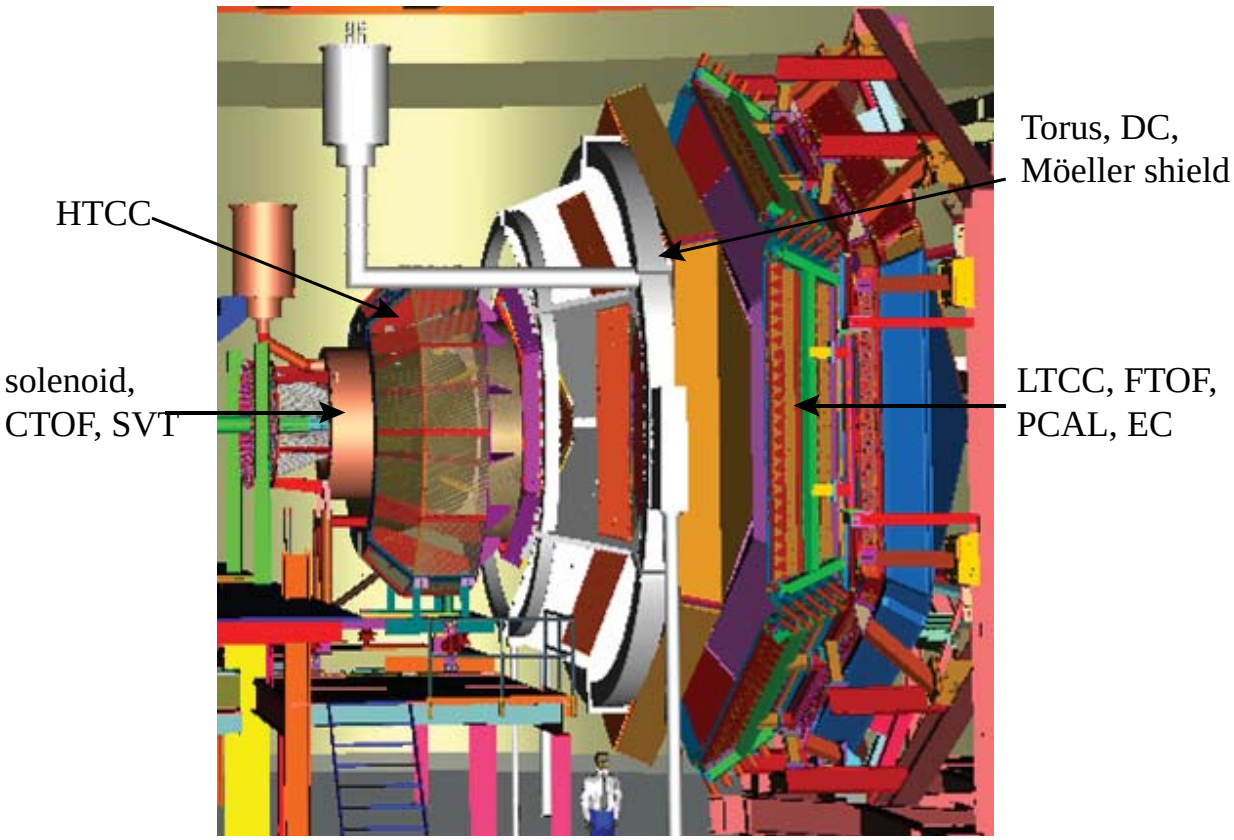


FIG. 1.1. A three-dimensional view of the proposed CLAS12 detector, showing the subsystems.

2 Central Detector

The central detector consists of a solenoid, central time-of-flight system (CTOF), and the SVT, FIG 2.1. The solenoid has outer and inner diameters of 2040 mm and 780 mm and a length of 1800 mm. The maximum central field value of the solenoid is 5 T. Besides curling Möller electrons into the absorber, the magnetic field of the solenoid is essential to determine the momentum of charged particles. The CTOF is located against the inside surface of the solenoid. The time resolution of the CTOF, ~60 ps, enables charged particle identification, as well as rejection of out-of-time hits. Between the target and the CTOF, there is ~240 mm of radial distance, available for the SVT.

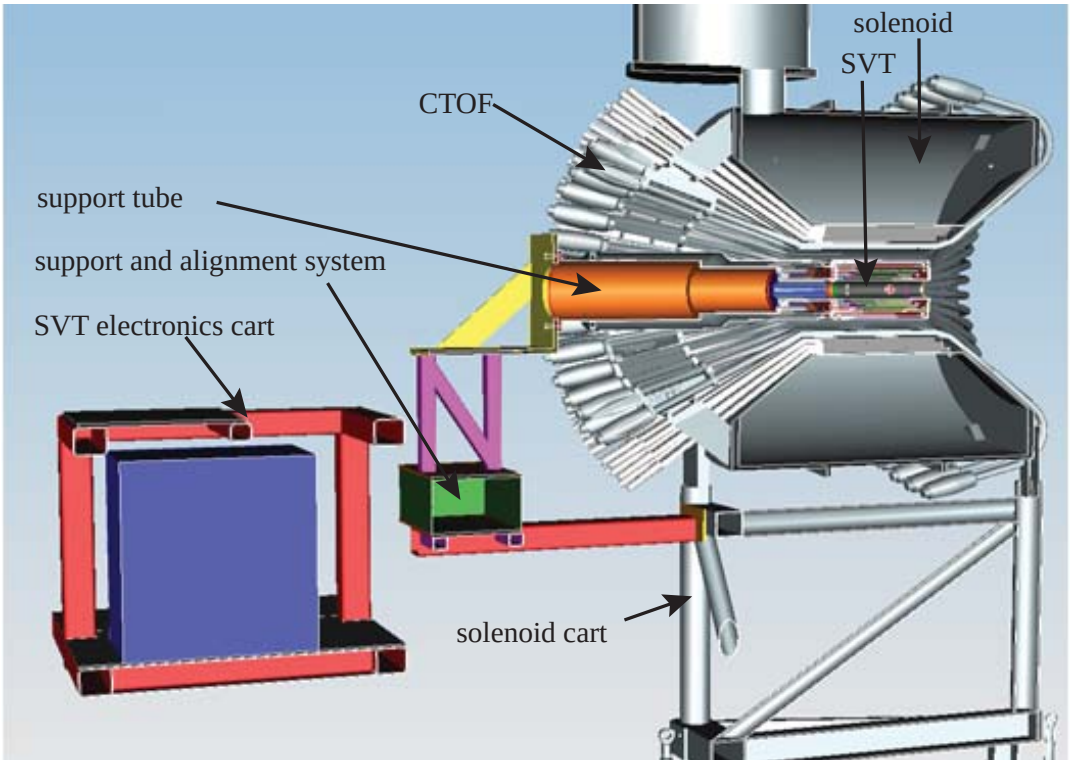


FIG. 2.1. Central detector with SVT.

3 Silicon Vertex Tracker

3.1 Introduction

Deep exclusive reactions set stringent requirements for the CLAS12 tracking system [1]. The design of the SVT is based on these requirements. The SVT, which has a coverage in θ is from 35°–125° and a coverage of ~2π in φ, has four polygonal regions, R1–R4, that have 10, 14, 18, and 24 sectors respectively.

Each sector is realized by a module, whose top and bottom sides each, have three (Hybrid, Intermediate, and Far), 320-μm thick, silicon sensors, a pitch adapter, and a readout hybrid—part of the readout electronics located on the hybrid flex circuit board (HFCB), which are wire bonded together. Studies indicate that as long as the cracks between adjacent sectors are less than 2 mm, track loss due to the cracks is less than 5% for a half-field setting, 2.5 T, of the solenoid. The bottom side of the module, closer to the beam, is referred to as the *U* layer, or the #*A* layer, the top side of the module is referred to as the *V* layer, or the #*B* layer; the hash sign is a placeholder for the region number. Each side of the module has 256 readout strips.

Having four regions for track reconstruction, rather than the minimum of three, not only provides a redundant tracking region, but mitigates tracking inefficiencies caused by malfunctioning strips and electronics, and electronic noise of a layer, and reduces the number of accidental tracks—tracks reconstructed wholly with or with a subset of background hits. Tracking simulations indicate that with four regions, instead of three, the probability of reconstructing accidental tracks for a given number of correlated background hits per region, randomly distributed over the four regions, is reduced by about a factor of three. Further, the tracking simulations indicate that with four regions, the track reconstruction program can handle ~40 hits in an acquisition time window of 132 ns.

R1–R4 have inner radii of ~65 mm, ~92 mm, ~119 mm, and ~160 mm, respectively, Fig 3.1.1. The radial distance Δr between R1 and R4 has been maximized because the momentum resolution goes as Δr^{-2}. To match the absolute momentum resolution of the forward tracking system, the central tracking system's fractional momentum resolution requirement for particles with a momentum of 1 GeV is required to be ~5%—needed to identify a missing pion in exclusive reactions [1]. To measure the momentum with a resolution better than 5%, for tracks with p_T up to 1 GeV,

for the given spacing of Δr of 9.5 cm between R1 and R4, a spatial resolution better than 70 μm in the bending plane is needed.

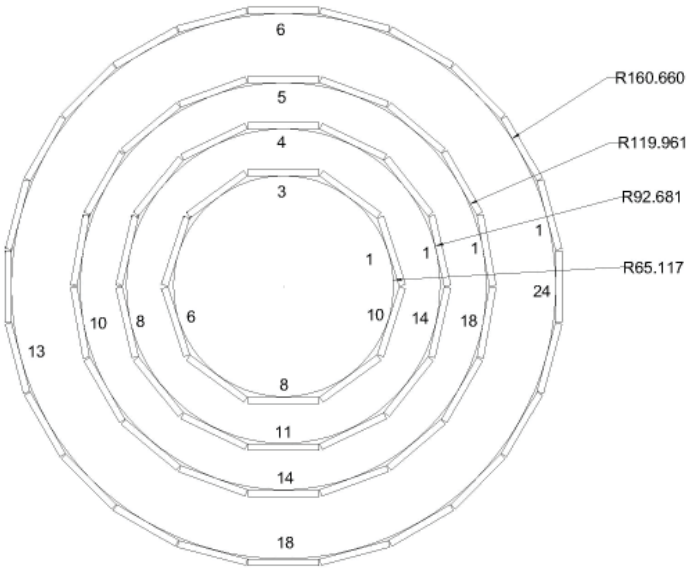


FIG. 3.1.1. Rear view of the SVT showing the module partitioning in each region.

The readout strips have a constant φ pitch of 1/85°. Such a layout reduces the dead area along the edge of the sensors, particularly important, because the modules, to reduce the radiation length seen by a particle's trajectory, do not overlap. As a consequence of the constant φ pitch, the layout of the strips is such that the strip pitch P (z,n,n+1) between the n^{th} and the $(n+1)^{th}$ strip is a function of the z location and of the strip numbers n and n+1. The readout pitch of a module ranges from 156 μm at the Hybrid sensor end to 202 μm at the Far sensor end of the module. Because of the change in the pitch, the spatial resolution ranges from 50 μm at the Hybrid sensor end to 65 μm at the Far sensor end of the module. The r-z position of tracks is determined by the stereo angle, which is 3° at the Hybrid sensor end and ~2° at the Far sensor end.

To reduce the degradation of the performance of the pattern recognition algorithm, which degrades as hit occupancy and the number of multiple hits (more than one hit within an acquisition time bin on the same strip) increases, the hit occupancy and multiple hits are kept as low as possible by minimizing the readout pitch, increasing the number of readout channels, which on the other hand for cost reasons have to be kept at a reasonable number. Fulfilling these requirements leads to a readout strip pitch around 150 μm, as well.

Figure 3.1.2 shows a 3-D rendering of the complete SVT.

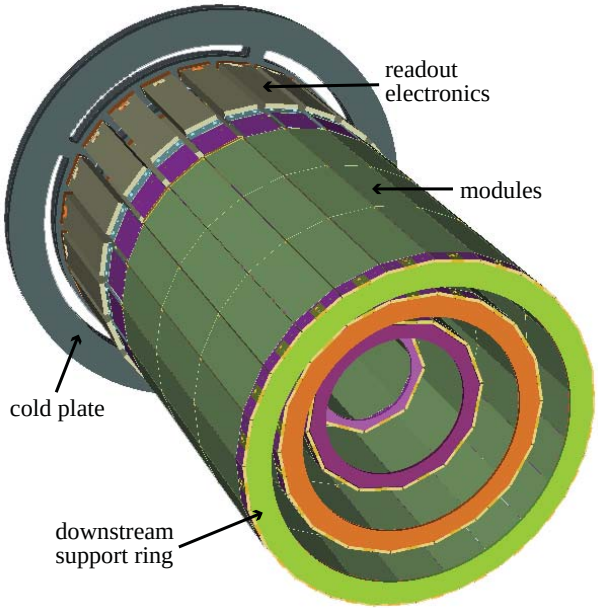


FIG. 3.1.2. Conceptual rendering of the SVT.

Hits on the *U* and *V* strips of a region are combined to form a 3D space-point. The space-point has a resolution $\sigma_{\perp}$ perpendicular to the strip and $\sigma_{||}$ along the strip. Because of the small stereo angle, $\sigma_{\perp} \approx \sigma_{strip}$ and $\sigma_{||} \approx 862$–1600 mm. Using pulse height information from the 3-bit flash ADC of the FSSR2 ASIC, the spatial resolution can be improved by the weighting algorithm in the cluster finding routine.

Multiple scattering leads to the deviation of charge particle trajectories and, in the case of electrons, fluctuating energy losses due to Bremsstrahlung. To optimize the tracking performance and to prevent the degradation of tracking resolution due to multiple scattering, the total number of radiation lengths X_0 seen by particles traversing the detector is minimized. The X_0 of a module is ~1%.

Table I summarizes the specifications of the central tracker.

Specification	Measurement
angular coverage	35°–125°
momentum resolution	$dp/p < 5\%$
θ resolution	10–20 mrad
φ resolution	~5 mrad
luminosity	10^{35} cm^{-2}s^{-1}

TABLE I. Specifications of the CLAS12 central tracker.

3.2 Simulation

Event and background rates have been estimated with the Geant4 Monte-Carlo simulation package (GEMC) [2,3]. The sensitive volume of each module includes active area materials: silicon, epoxy, bus cable, carbon fiber, wire bonds, copper support, Noryl support ring, and Rohacell, as well as the hybrid portion of the hybrid flex circuit board (HFCB) instrumented with FSSR2 ASICs. For the simulation, the sensitive volume can be selected to be either three or four regions. Figure 3.2.1(a) shows the engineering drawing, and Fig. 3.2.1(b) shows the GEMC implementation; it can be seen that the Geant4 implementation is a true representation of the SVT.

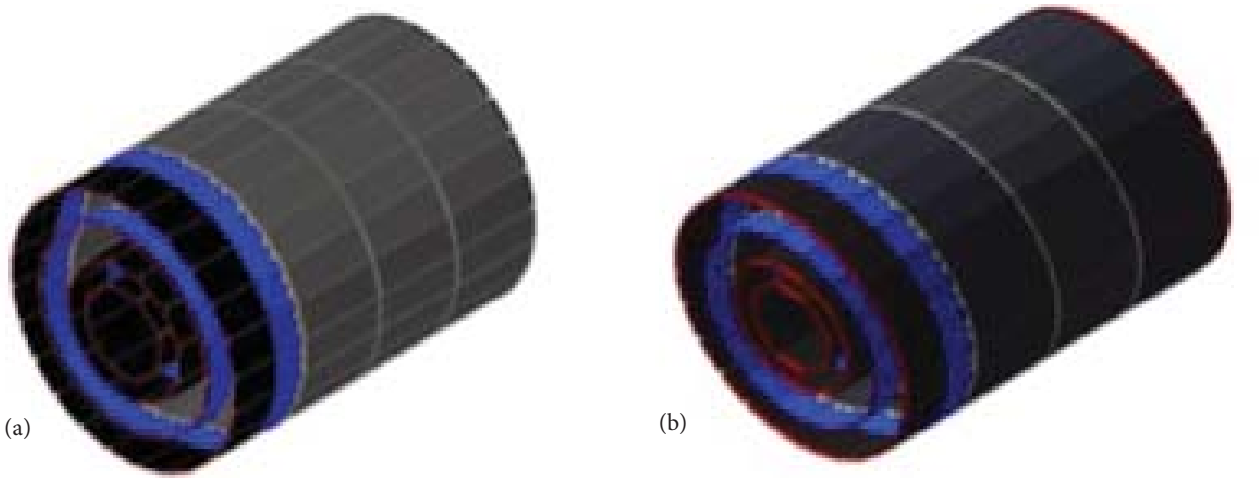


FIG. 3.2.1. (a) The engineering design of the SVT. (b) The GEMC implementation. All dimensions, materials, and placements match the design.

The simulation takes into account charge-sharing between the strips as well as the capacitive coupling of the strips to each other and to the bias plane. For each Geant4 step, the charge-sharing algorithm, illustrated in Fig. 3.2.2, was applied. If ionization occurs near the readout strip center, all the electrons generated by the ionization drift to that readout strip. If the ionization takes place exactly between two strips, at the location of the intermediate strip, 90% of the electrons will be divided between the adjacent readout strips and 10% of the electrons will be lost due to the intermediate strip's capacitive coupling to the aluminum bias voltage plane of the sensor.

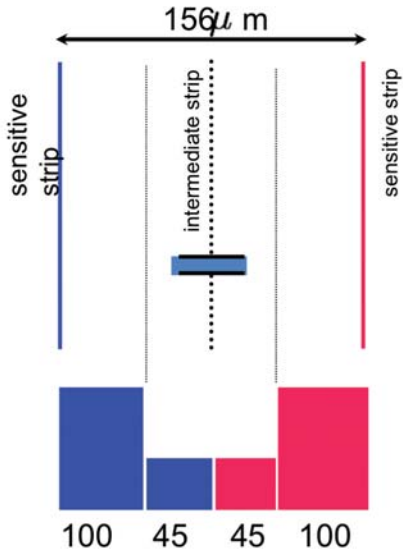


FIG. 3.2.2. Charge-sharing in the SVT hit process routine.

The most probable number of electrons, the signal Q_s, generated by a minimum ionizing particle in a 320-μm-thick silicon sensor is ~24,000 electrons (~3.8 fC). The electronic noise charge Q_n is given by dividing the signal Q_s by the signal-to-noise ratio, S/N. Simulations were performed for several values of S/N; results for S/N of 10 are presented here.

At a luminosity of $10^{35}cm^{-2}s^{-1}$, the beam current for a 5 cm liquid hydrogen target is 80 nA, which for a data acquisition time window of 130 ns corresponds to ~65,000 electrons. These electrons interact with the target and produce photons, electron-positron pairs, and hadrons. Background hit rates for different targets were extracted. The hit information includes raw Geant4 information: energy deposited, position, location, and timing, and digitized information, such as strip number, layer, sector, ADC, and TDC.

Figure 3.2.3 shows energy deposition for kaons and protons in layer 1*A* as a function of the particles' momentum. As expected, the minimum ionizing region starts at ~600 MeV/c for kaons and at 1 GeV/c for protons.

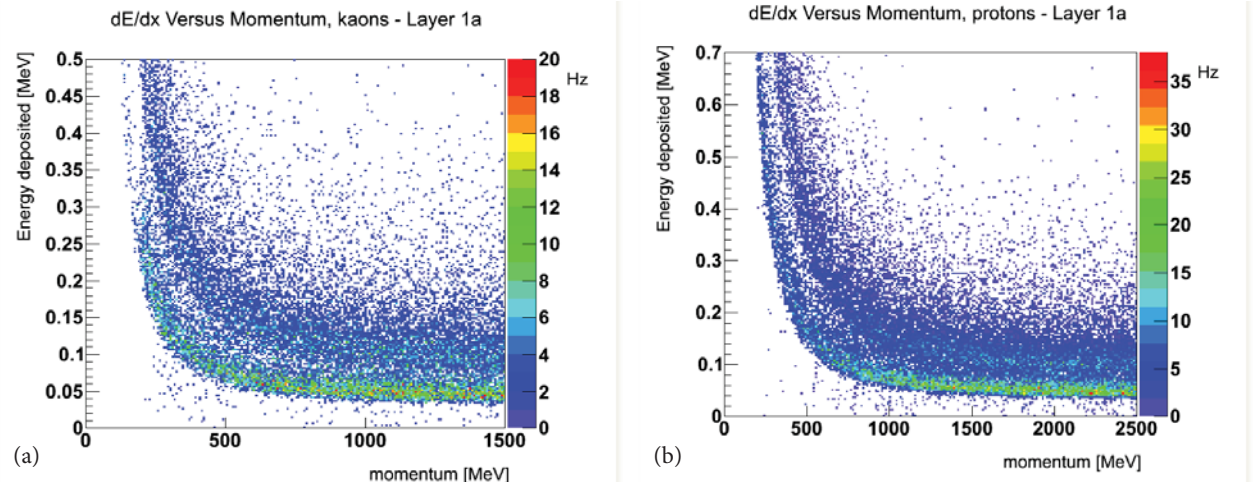


FIG. 3.2.3. Energy deposited versus momentum for kaons (a) and protons (b).

The energy deposited E_{dep} for pion, proton, and kaon tracks, and electromagnetic and hadronic backgrounds, is shown in Fig. 3.2.4. This plot is used to determine the energy threshold E_{Th} needed to reject the background. To determine how many events are rejected at a certain E_{Th}, the number of events with E_{dep} between 0 and E_{Th} is calculated and divided by the total number of events $N(E)$; this ratio is the rejection factor $R_{E_{Th}}$:

$$R_{E_{Th}} = \frac{\int_0^{E_{Th}} N(E)dE}{\int_0^{\infty} N(E)dE}$$

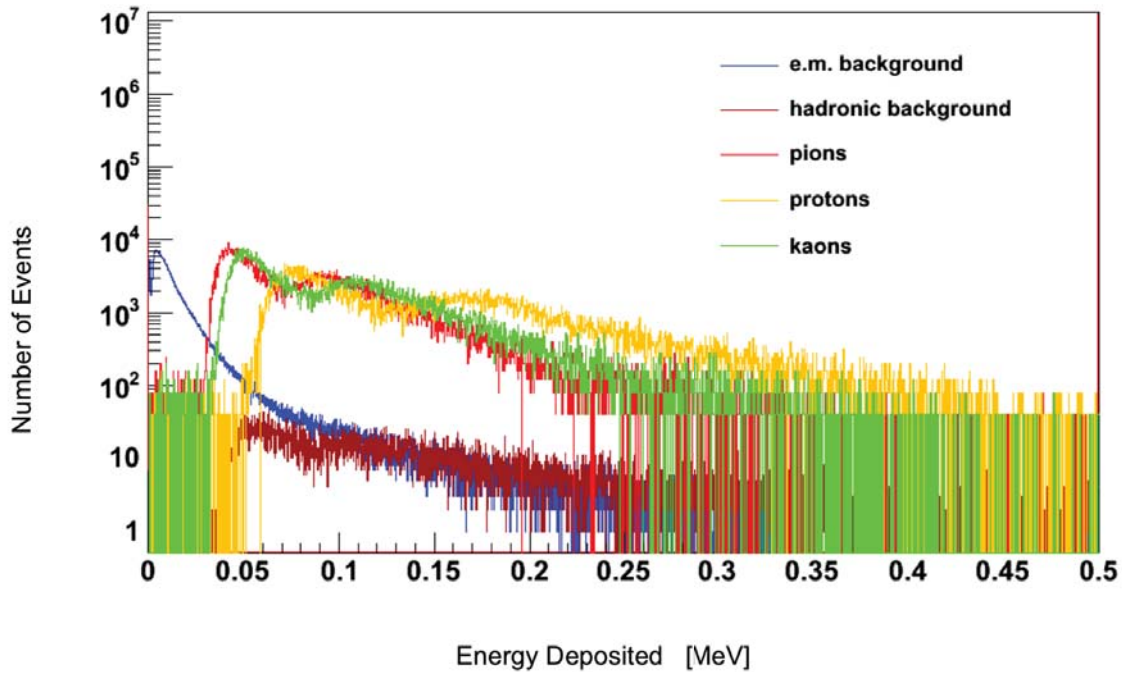


FIG. 3.2.4. The energy deposited for pion, proton, and kaon tracks, plus electromagnetic and hadronic backgrounds; signal $800 < p < 1000$ MeV.

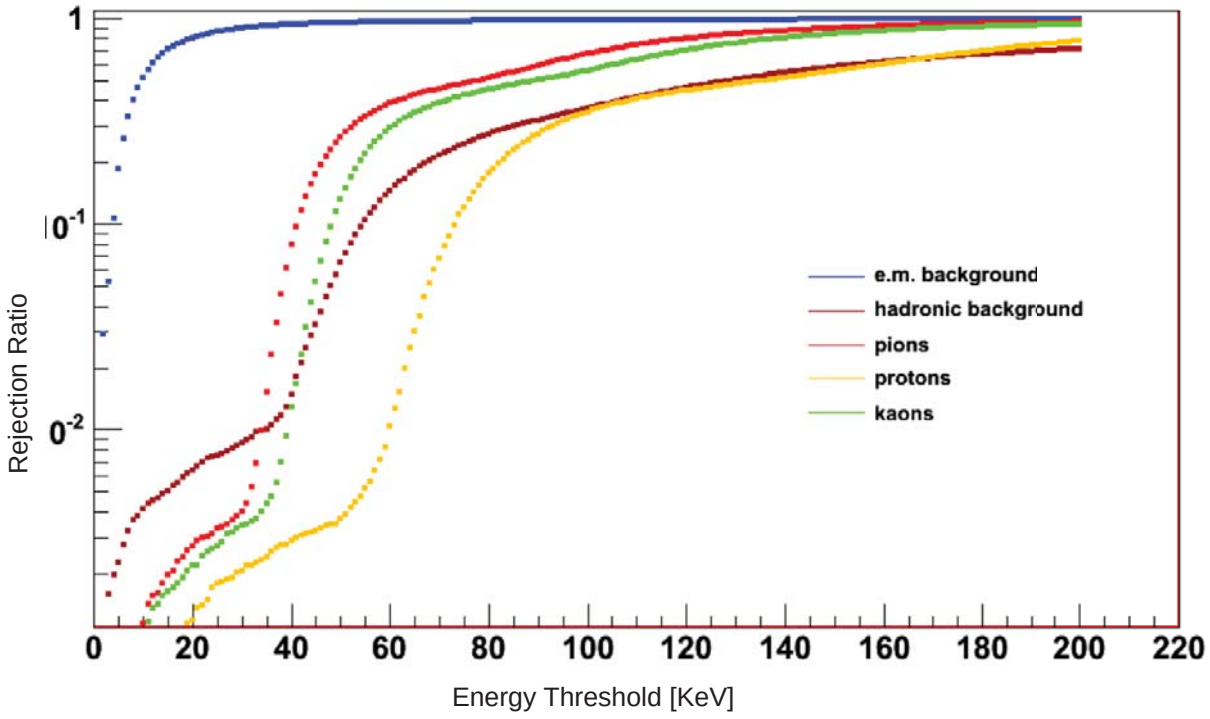
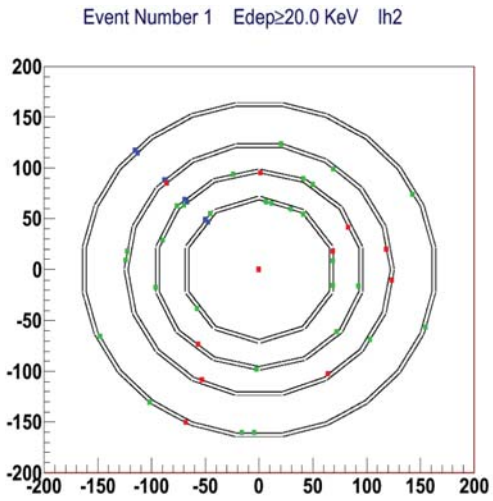


FIG. 3.2.5. The rejection factor for pions, protons, kaons and electromagnetic and hadronic backgrounds; signal $800 < p < 1000$ MeV.

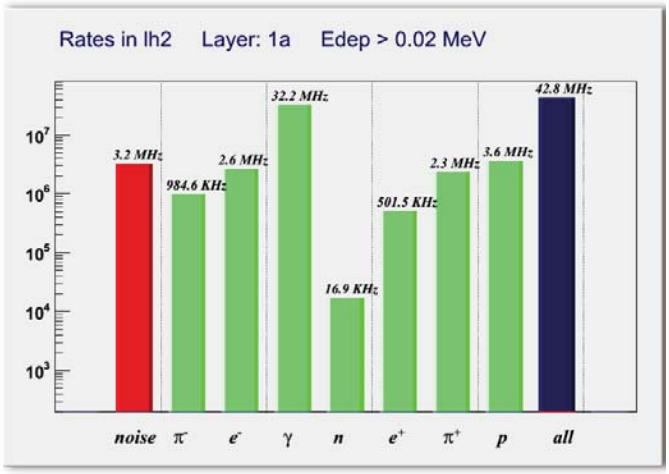
Fig. 3.2.5 shows that at a threshold of 30 KeV, 92% of the electromagnetic background and 0.5% of the signals coming from pions, kaons, and protons are rejected.

Figure 3.2.6 shows the generated background rates from an LH_2 target for E_{Th} of 20, 30, and 40 KeV in layer 1*A*, the layer closest to the target, for 5 T setting of the solenoid. The left hand column shows the hits (background hits are in green; electronic noise hits are in red; hits from the true track are in blue) on the four regions of the SVT. As the threshold increases the background and electronic noise hits are reduced, and at 40 KeV only the hits from the background and true tracks remain. Figure 3.2.7 shows in detail the difference for energy thresholds of 20 KeV and 30 KeV.

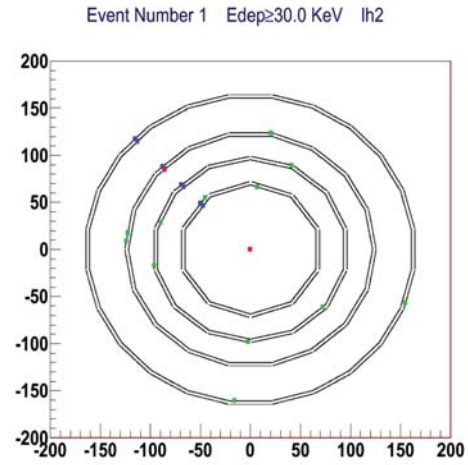
The right hand column of Fig. 3.2.6 shows the individual rates from different particles and in purple, the rightmost bar, the total rate. At a threshold of 20 KeV, the photon rate is ~75% of the total rate and decreases to ~35% of the total rate at 40 KeV. To be noted is that the hadronic rate is not reduced by increasing the threshold to 40 KeV; the ratio of the hadrons to photons, which is ~0.2 at 20 KeV increases to ~1.2 at 40 KeV. The electronic noise, shown in red, disappears at 40 KeV. Based on these observations the threshold setting is expected to be between 30–40 KeV.



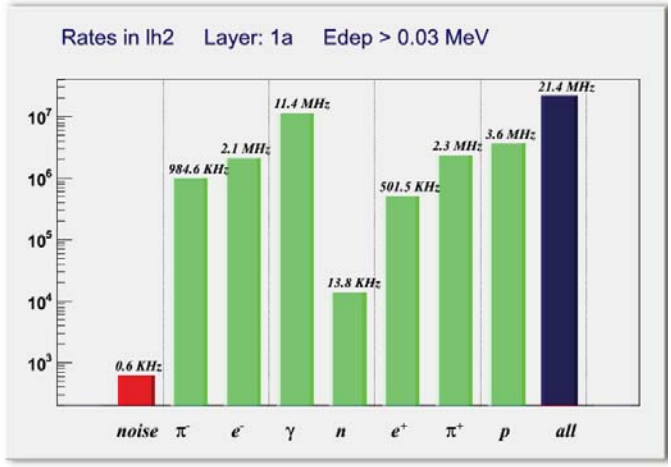
(a)



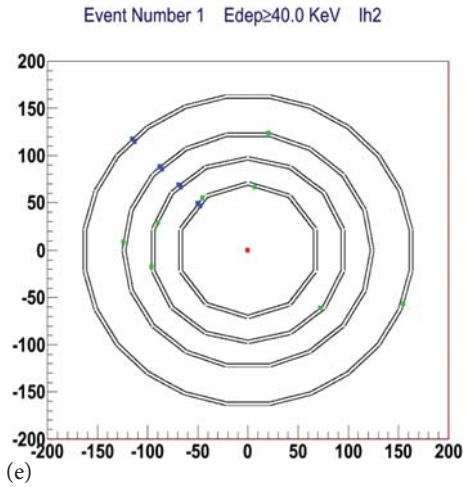
(b)



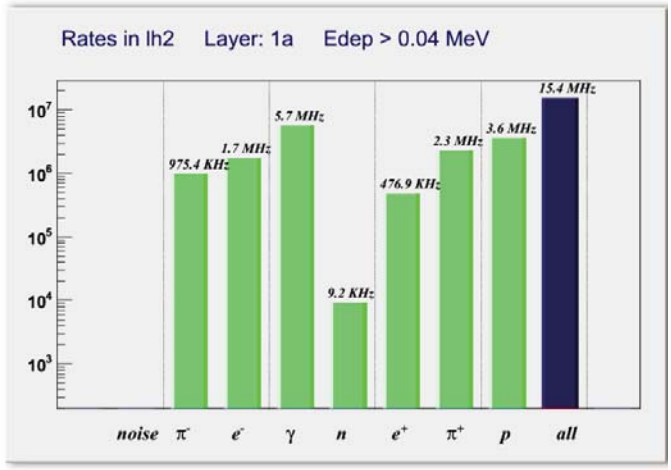
(c)



(d)



(e)



(f)

FIG. 3.2.6. One proton plus background event at an energy threshold cut of 20 KeV (a), 30 KeV (c), and 40 KeV (e). Background and noise rates (b), (d), and (f).

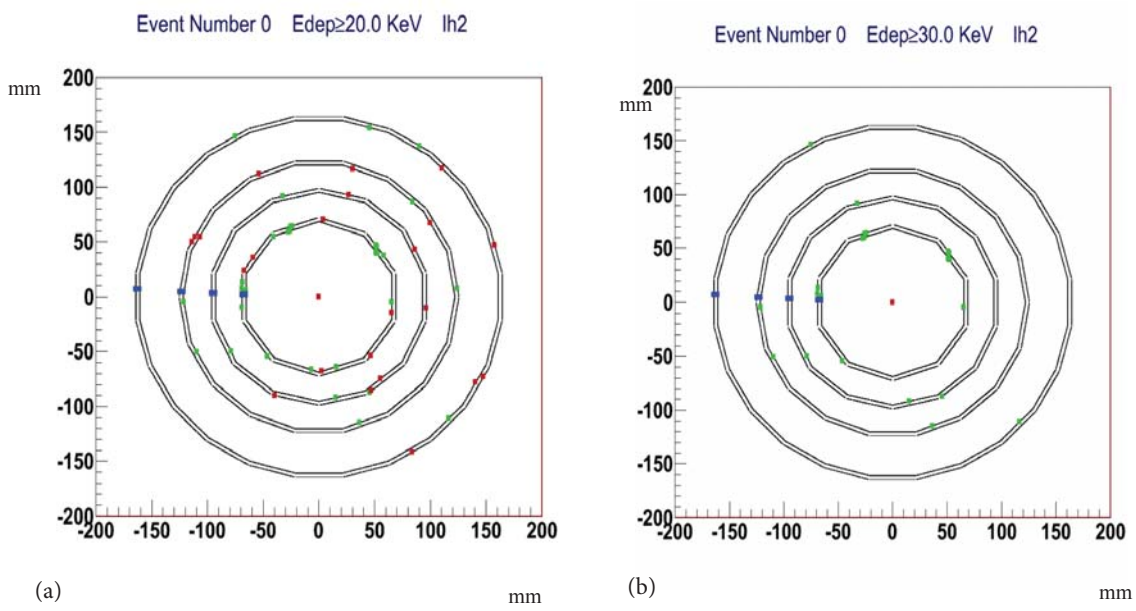


FIG. 3.2.7. (a) A proton track at full luminosity, shown by the blue rectangles. Background hits are shown in green. Electronic noise is shown in red. At 20 KeV of electronic threshold, the electronic noise is comparable to the physics background. However, at 30 KeV (b), electronic noise disappear.

Table II shows the rates of an FSSR2 ASIC on layer 1*A* and its occupancy for an acquisition time of 130 ns.

E_{th} [KeV]	Rate [Mhz]	Occupancy [%]
20	2.14	0.22
30	1.07	0.11
40	0.77	0.08

TABLE II. Rate and occupancy as a function of energy threshold for FSSR2 ASICs on layer 1*A*.

The radiation dose was calculated for LH_2, LD_2, C, Fe, and Pb targets. Table III shows the radiation dose for C and Fe. For the C target, the simulation yields, for layer 1*A,* 301 Krad per year of continuous running (one year of continuous running is equivalent to two years on the floor because of beam availability and planned shutdowns.). The radiation dose of 301 Krad/year corresponds to 3 Mrad for 20 years on the floor, well within the acceptable limit of 5 Mrad [4,5]. In the calculation, it was assumed that all radiation in one sector will be absorbed by the Far sensor of the layer. Much as this is a reasonable assumption, Fig. 3.2.8, it leads to an overestimate of the dose. With regards to the radiation dose, it should be noted that the FSSR2 ASICs are radiation hardened to handle a dose of 5 Mrad. The silicon sensors are affected by radiation. However, up to a dose of 2 Mrad, the modules can be operated at ~21°C. The 1 MeV equivalent neutron fluence for the LH_2 target over a year of continuous running in layer 1*A* is estimated to be ~ 5 x 10^{11} cm^{-2}.

		C			Fe	
Particles	GeV/s	Mrad/s	Rad/year	GeV/s	Mrad/s	Rad/year
pi-	229	0.112763	3556	363	0.178654	5634
e-	209	0.102942	3246	554	0.272492	8593
gamma	5236	2.57438	81185	5585	2.74589	86594
n	47	0.0232453	733	108	0.0531899	1677
e+	58	0.0286764	904	145	0.071363	2250
pi+	365	0.1798	5670	650	0.31982	10085
p	9967	4.89975	154518	13452	6.61283	208542
all	19468	9.57049	301814	23496	11.5503	364249

TABLE III. Layer 1*A* fluences.

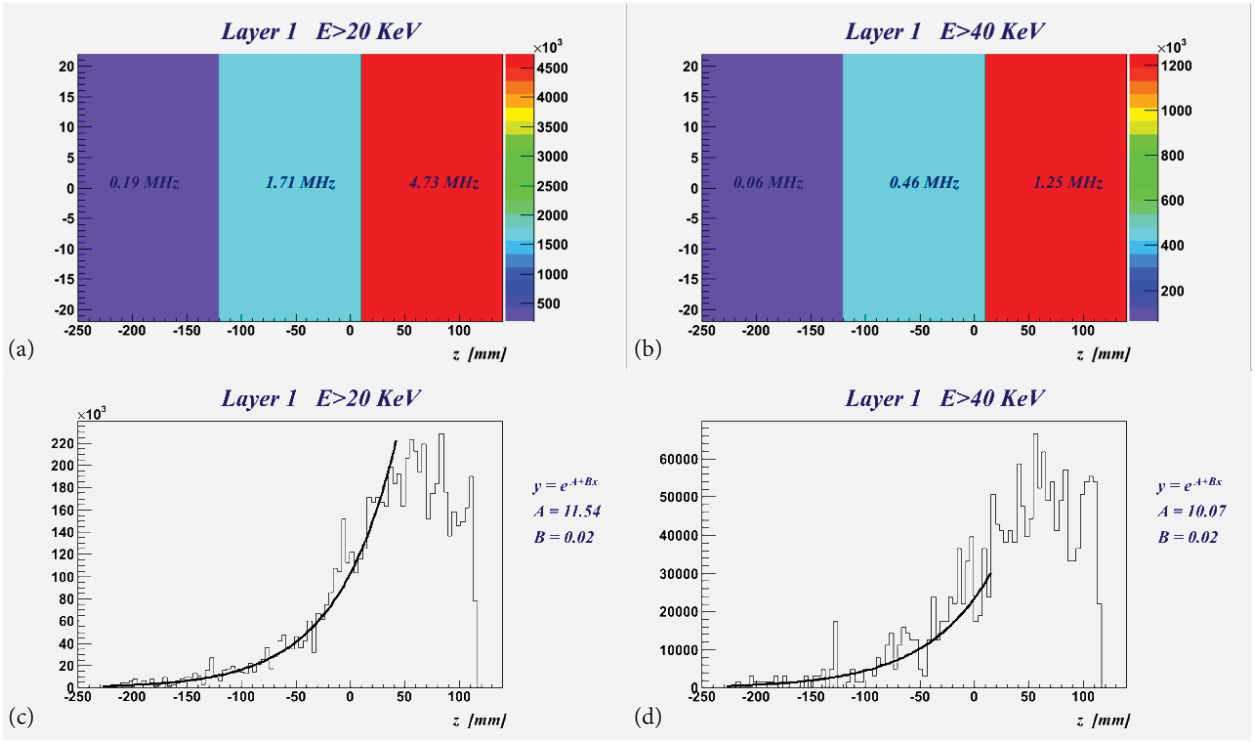


FIG. 3.2.8.

For 5 T and 2.5 T settings of the solenoid, the green and red lines along the beam axis, Fig. 3.2.9, is the Möller electron envelope, on the surface of which the rate is ~1 MHz. The Möller electron rate drops rapidly with increasing θ scattering angle [3].

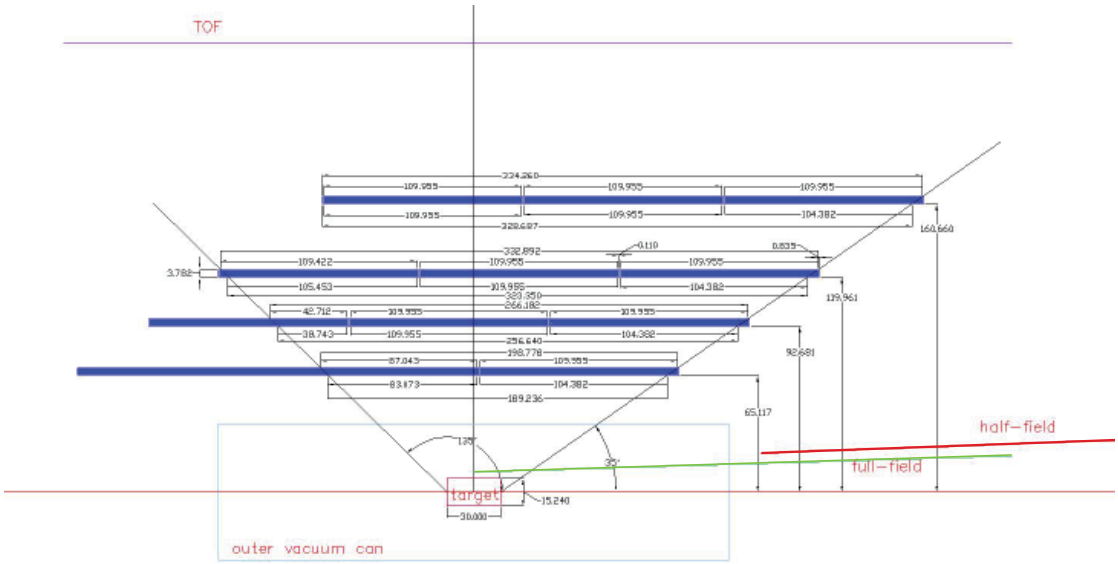


FIG. 3.2.9. Side view of the SVT showing the layout of the regions (all dimensions in mm.)

Though most of the photons are absorbed in one layer, quite a few cause double hits. Because the photon rate from the LH_2 target, at a threshold of 20 KeV, is ~75% of the total rate, the number of doubled hits in the four regions was estimated.

A double hit is defined as a hit in both layers of a region where the second hit is, at most, one readout strip away from the first hit. The double hit to single hit ratio varies by region—4%, 2.5%, 1.5%, and 1.0% in R1–R4 respectively. The double hit to single hit ratio for R2 is shown in Fig. 3.2.10.

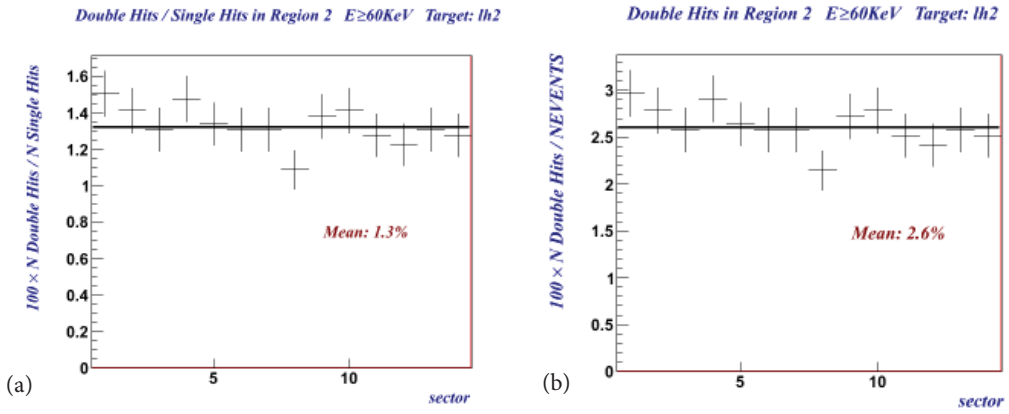


FIG. 3.2.10. (a) The double hits/single hits ratio of the physics background at CLAS12 luminosity. (b) The probability of having a double hit. Both plots are for R2.

Accidental tracks have two components, *sister* and *fake* tracks. Sister tracks are caused by using most of the hits that are used for reconstructing the real track, along with some background hits. This situation occurs when accidental hits are close to a real hit. Sister tracks have nearly the same momentum as the real track. Fake tracks are caused by using all or most of the background hits. Fake tracks give rise to a smooth background and have no connection whatsoever to the real track. This smooth component peaks at small values of momenta. Studies show that the number of fake tracks is sensitive to a cut on the energy deposited in a single strip. These combinations will probably be removed during analysis, but they do degrade the resolution.

A study considered uncorrelated, evenly distributed background. An effect of this kind of background is to produce fake tracks. A cut-based track-finding algorithm was applied to a set of events generated from random hits in

each layer, augmented with a 10% punch-through probability, that is, for each hit, there was a 10% chance that a strip in the next layer would be hit as well. The 10% punch-through probability is an over estimate compared to the results of the simulation. The cuts were tuned so that true tracks were found with a greater than 95% probability.

Fig. 3.2.11 shows for two cases the number of reconstructed fake tracks vs. the assumed rate of accidental hits per layer: in one case with a six-layer and in the other with an eight-layer SVT. For both configurations, at low background, there are few fake tracks. The number of fake tracks grows exponentially as the background increases. Fake tracks can be reduced significantly by using information from the CTOF counters; nevertheless, the goal is to keep the level of fake tracks as low as possible.

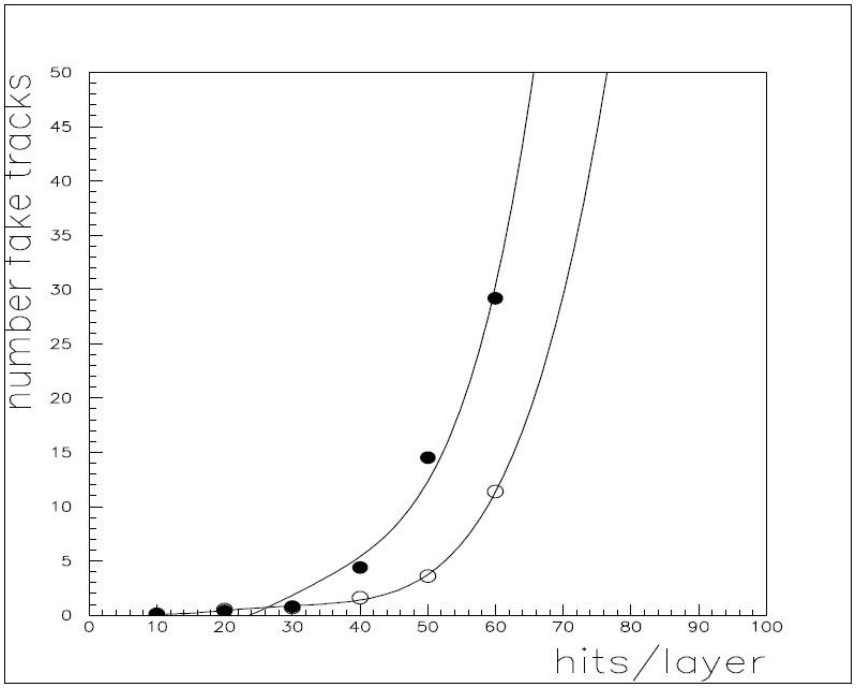


FIG. 3.2.11. A plot of the number of reconstructed fake tracks as a function of the number of accidental hits per layer for two cases: a six-layer (filled circles) and an eight-layer (open circles) version.

Fig. 3.2.11 shows that for five fake tracks per event, an eight-layer design extends the luminosity reach by ~20% over a six-layer design. For a background hit rate of 45 MHz in a 130-ns-acquisition time bin, there will be ~6 accidental hits per plane; at this background hit rate, no fake tracks are reconstructed.

To understand the loss of tracking efficiency and the number of accidental tracks reconstructed by the tracking code in the presence of background hits, a study was conducted, in which, first, Geant4 generated the background hits. Hits from a true track then were embedded among the background hits. The tracking code was optimized and tasked to find the true track. It was found that there was a loss of efficiency in reconstructing real tracks and that accidental tracks were reconstructed as well. These effects depend upon the number of background hits.

Figure 3.2.12 shows the number of reconstructed tracks for different levels of background, from none to 100% of the nominal background (translates to 1.6 times the design luminosity). Less than 5% of events have more than one track reconstructed.

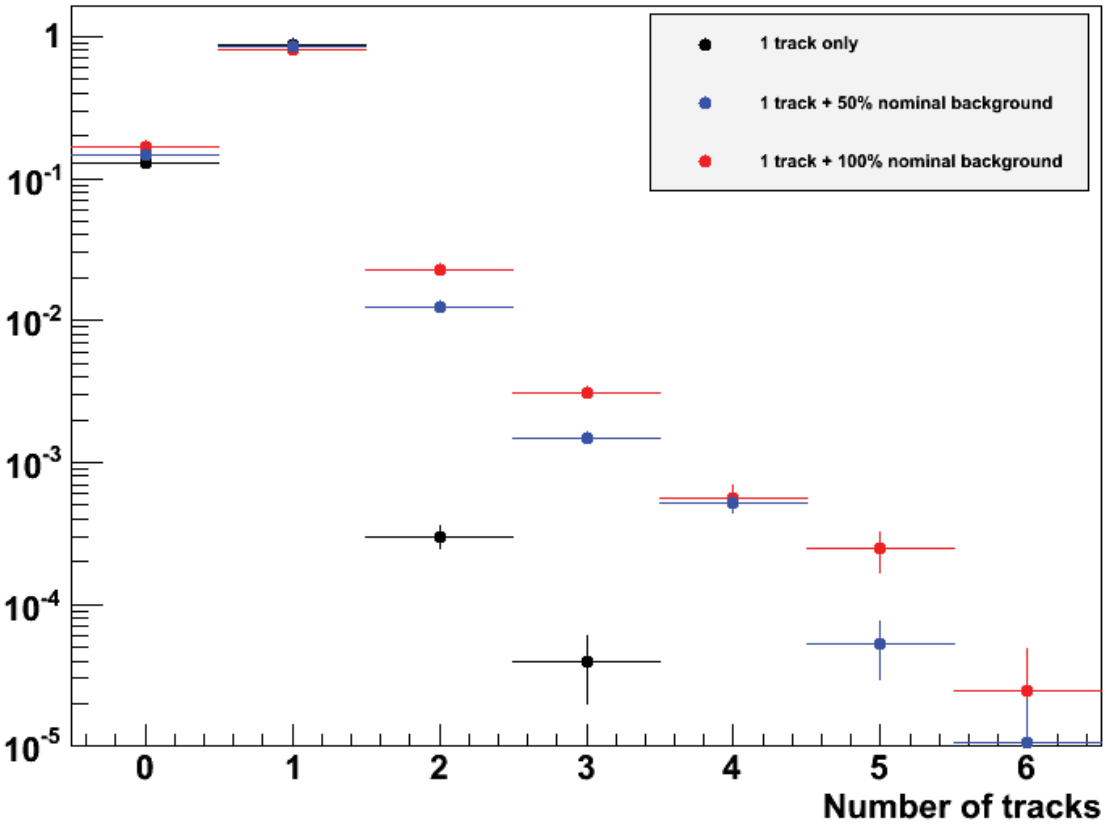


FIG. 3.2.12 The number of reconstructed tracks for different levels of background.

Figure 3.2.13 shows the resolutions of the momentum p, azimuth φ, and polar angle θ as a function of the momentum of a single-proton track generated at $\theta = 60°$; the momentum of the single proton track ranges from 0.2 to 1.8 GeV/c. To study the effect of the background on the resolutions, the background was varied, as before. The results show that the resolutions meet requirements even for a background level 100% higher than that expected for nominal luminosity.

To consider a signal generated in the sensor as a hit, the reconstruction algorithm requires a minimum energy deposition of 20 KeV. This requirement reduces background noise and multiple track candidates, Fig. 3.2.14. The overall tracking efficiency is estimated to upwards of 80% for a proton track in the momentum range 0.3–1.8 GeV/c. The tracking efficiency is flat in θ between 40°–120°. The inclusion of charge-sharing in the simulation has negligible effect on the tracking efficiency.

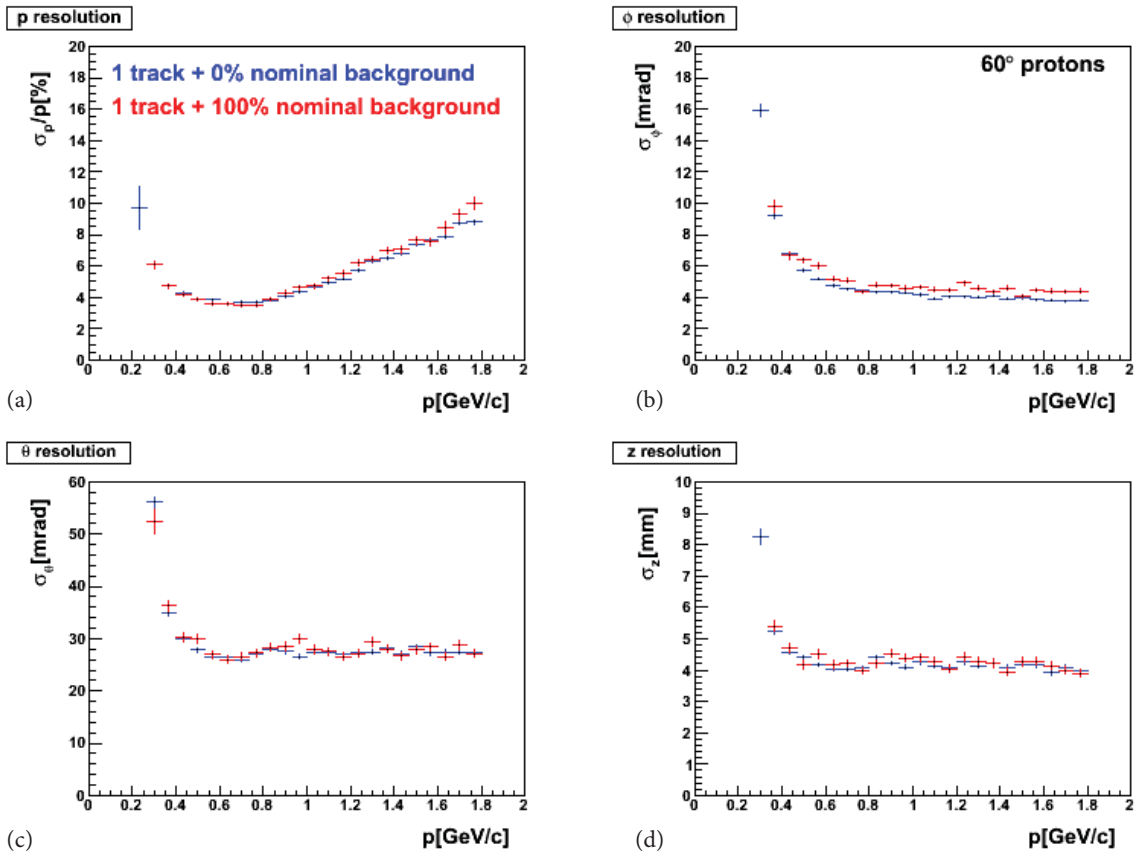


FIG. 3.2.13. The momentum p (a), azimuth φ (b), polar angle θ (c), and vertex position in z (d) resolution as a function of momentum corresponding to a single proton track generated at $\theta = 60°$ over a momentum ranging from 0.2 to 1.8 GeV/c.

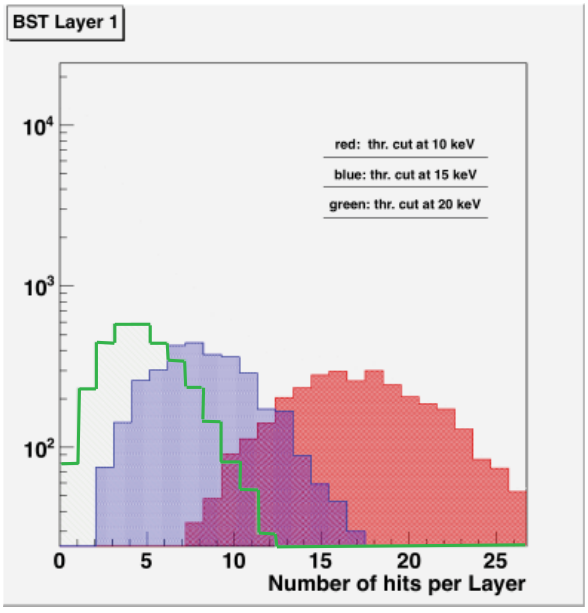


FIG. 3.2.14. Hit multiplicities in layer 1A for threshold energy cuts at 10, 15, and 20 keV. The multiplicities in layer 1A are sensitive to the choice of threshold value.

3.3 Expected Physics Performance

A series of programs have been used to calculate the acceptance of the central detector and have reconstructed physics parameters for types of events that are of interest. The program CLASEV [6] served as an event generator and analysis program. Depending on the value of input flags, CLASEV produces a set of four momenta for the primary hadrons in the hadronic center-of-mass and allows some of them to decay into the final-state hadrons and transforms their momenta to the lab system. For each final-state track, CLASEV calls the fast Monte Carlo (FASTMC) program to determine whether the track falls within the fiducial acceptance window, and if it does, determines the track's smeared lab momentum. CLASEV then produces selected physics analysis variables (e.g. missing mass) from calculations involving the smeared momenta of the tracks. Fig. 3.3.1 shows the missing mass resolution expected for CLAS12 from FASTMC simulation studies based on the current design for a number of different reactions. For all cases studied, the results show that it is possible to identify the missing particle for each reaction.

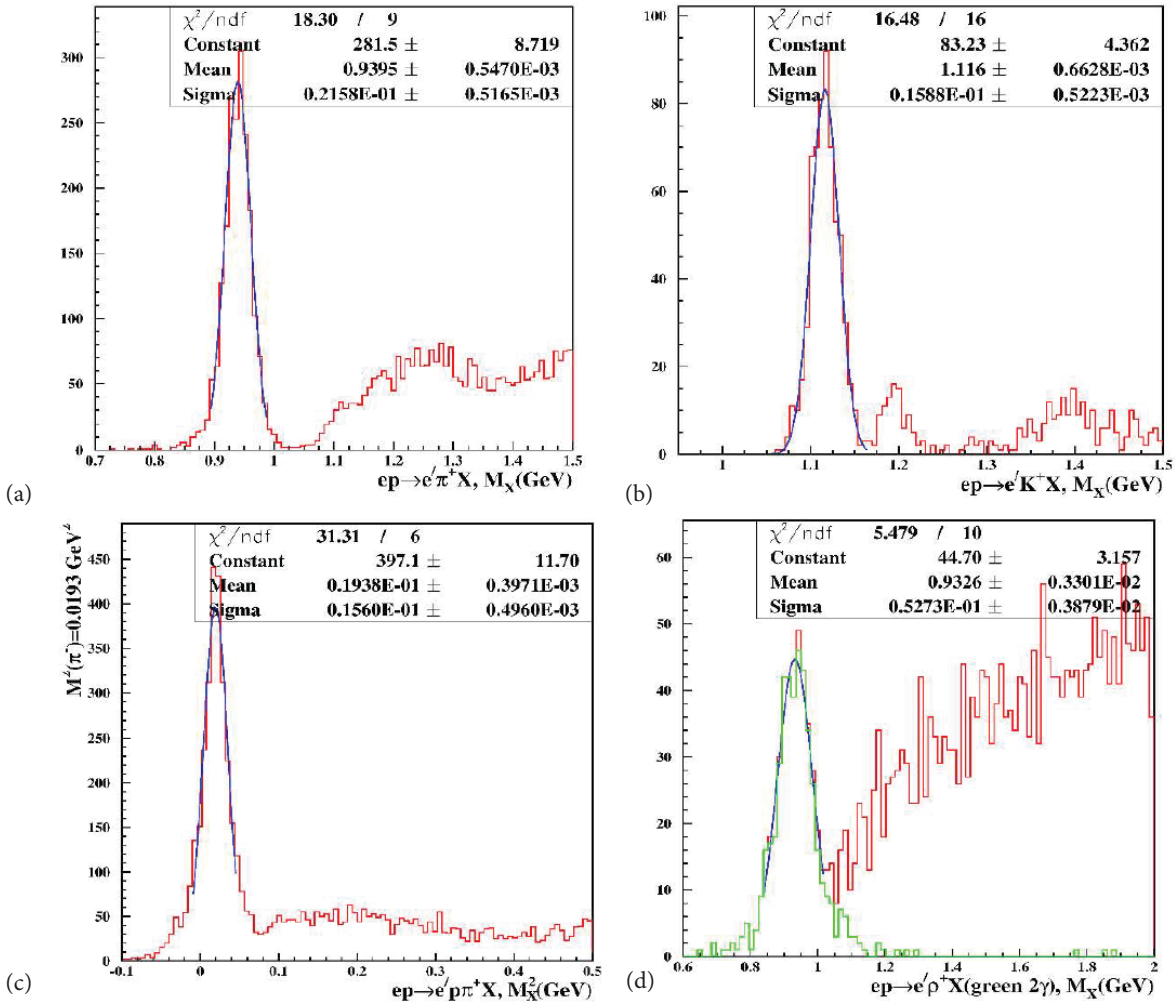


FIG. 3.3.1. Simulation results from FASTMC highlighting the expected missing mass resolution of CLAS12 with the nominal design specifications for the tracking detectors (drift chambers and SVT). Shown are the spectra for the reactions $ep \rightarrow e'\pi^+X$ (a), $ep \rightarrow e'K^+X$ (b), $ep \rightarrow e'p\pi^+X$ (c), and $ep \rightarrow ep^+X$ (d).

Results from the FASTMC simulation of $e\pi^+$ events in which the recoil baryon is detected by missing mass are shown in Fig. 3.3.1. Figure 3.3.2. shows the missing mass spectrum expected when the π^+ is detected in the forward tracker (a) or central tracker (b). There is sufficient resolution to study resonant production and to compare, for example, *s*, *t, u* channel processes.

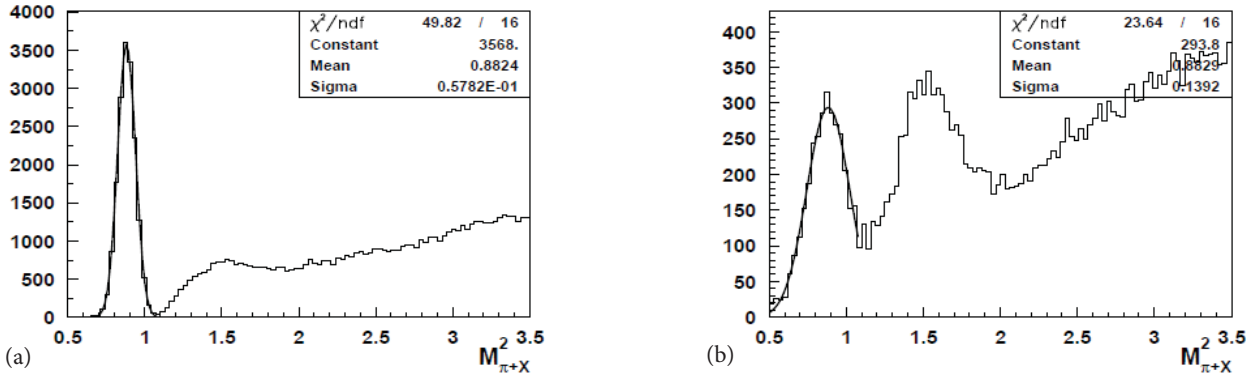


FIG. 3.3.2. Simulation results from FASTMC highlighting the expected missing mass resolution of CLAS12 for events in which only a π^+ and the electron are detected: (a) the π^+ is detected in the forward tracker, and (b) detected in the central tracker.

4. Sensor Design

4.1 Dicing Layout of the Wafer

The dicing layout of the 6-in. wafer was such that it provided two sensors, thereby maximizing the yield of sensors from a single wafer, which in turn reduced overall cost. The wafer dicing process requires a 0.25-in. keep-out zone around the edge of the wafer, Fig. 4.1.1. All sensors have a cut size of 111.62 mm x 42.00 mm.

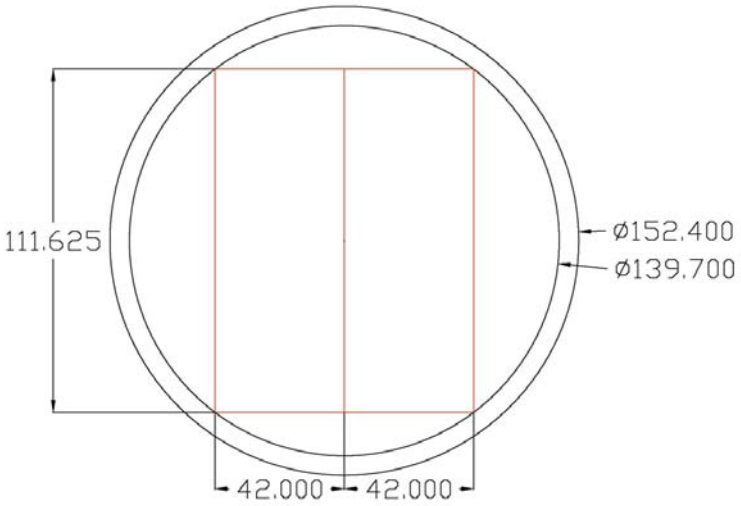


FIG. 4.1.1. Sensor dicing from a standard 6-in. wafer. All units are in mm.

4.2 Sensors

Figure 4.2.1 shows the cross-sectional view of the sensor. The aluminum strip width is 26 µm and is AC-coupled via the SiO_2 layer to the 20-µm wide p+ implant strips, which are ~1.2 µm below the aluminum strips. The unpassivated aluminum backplane (ohmic contact) is connected to the positive side of the power supply; the n-bulk volume of the sensor is depleted via the highly doped n++ layer. The 42-mm width of the sensor accommodates 256 readout strips and the ~1 mm keep-out zones along the edge of the sensor. Table IV lists the sensor specifications.

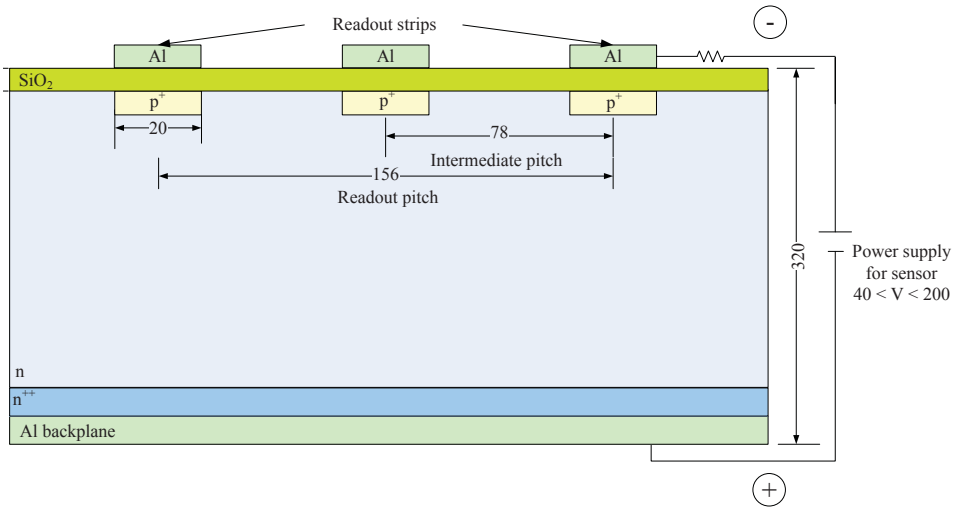


FIG. 4.2.1. Cross-sectional view of a sensor showing the different layers and the spacing of the strips (all units in μm).

Doping	*n*-type
Surface orientation	<100>
Wafer size	6-in.
Bulk resistivity	5 k Ω ± 30%
Thickness	300 μm ± 15 μm
Bowing	< 100 μm
Uniformity of thickness (single wafer)	< ±25 μm
Test structures	located on each wafer
Coupling	AC
Biasing scheme	bias ring to resistor
Biasing location	resistor at one end
Biasing type	poly-silicon resistor
Bias value	1.5 MΩ ± 0.5 MΩ
Readout	single-sided via Al strip
Implant strip type	*p*+
Strip-side covering (except for pads)	passivation - SiO_2
Back side Ohmic contact	aluminum - unpassivated
Outer size	42.0 x 111.62 mm
Active area	40.032 x 109.955 mm
Dicing lane	60–80 μm
Dicing tolerance	±20 μm
Roughness of cut edge	< 10 μm
Number of readout strips	256
Number of intermediate strips	256
Total number of strips	512
Implant strip pitch	75 μm
Readout strip pitch	150 μm

Implant strip width	35 μm
Aluminum strip width	41 μm
Overhang of Al strip (over implant)	3 μm (on each side)
Implant length	on resistor end of strips, implants extend to within 20 μm of bias ring
Guard ring	*p*+ implant ring DC coupled to Al electrode
Bias ring	same as guard ring; connects to bias resistors
Number of sensor types (masks)	3 (3)
Nomenclature of sensor types	Hybrid, Intermediate, and Far
Number of Hybrid sensors	144
Number of Hybrid wafers (2 sensors per wafer)	72
Number of Intermediate sensors	144
Number of Intermediate wafers (2 sensors per wafer)	72
Number of Far sensors	92
Number of Far wafers (2 sensors per wafer)	46
Total number of wafers	190
Total number of sensors	380
Bias ring pads (4)	250 x 100 μm (in corners of bias ring)
DC pad	50 x 160 μm (at bias resistor)
AC pads (test and readout)	200 x 60 μm (triple row at each end of strip)
N-sub contact	on bias resistor end
Mask dimension error	< 0.5 μm
Mask placement error (any direction)	< 1.0 μm
Full depletion voltage	40 < V < 100 (25°C at <45% RH)
Total leakage current (at full depletion voltage)	< 1 nA/cm^2
Interstrip capacitance	< 1.2 pf/cm
Strip to back side capacitance	< 0.2 pF/cm
Interstrip isolation (at 150 V)	> 1 GΩ
Resistance of Al electrode on strips	< 20 Ω/cm on strip
Dielectric of coupling capacitor	multiple thin layers of SiO_2 and Si_3N_4
Coupling capacitance	> 10 pf/cm
Break down voltage of capacitor	> 300 V
Total (strip) capacitance	($C_{tot} = C_{int} + C_{back}$ at 1 MHz) ≤ 1.3 pf/cm
Value of poly-silicon bias resistor	1.5 MΩ ± 0.5 MΩ
Single strip DC current	< 3 nA
Bad channel rate (average over every 100 sensors)	< 0.2%
Max number of bad channels/sensor	< 2 channels (0.8%)

(Note: Included in the bad channels count are: short circuit of coupling capacitor, short circuit of strip implant or Al electrode to other strips or bias ring, open circuit of readout electrode, bad connection of bias resistor, strips with DC current > 3 nA@150 V.)

TABLE IV. Sensor specifications.

For sensor evaluation, Hamamatsu provided *baby* test sensors and test structures. The test sensors have 20–30 strips and all the features of the full-size sensors. The test structures have pads for a planar diode, a gated diode, a field of wire bonding pads, a MOS capacitor, and for resistance measurement. On each wafer, there are two sets of *baby* sensors and test structures. Figure 4.2.2 shows the locations of the test structures on the mask. The test structures are used to measure specific features and characteristics of the silicon sensors, Table V.

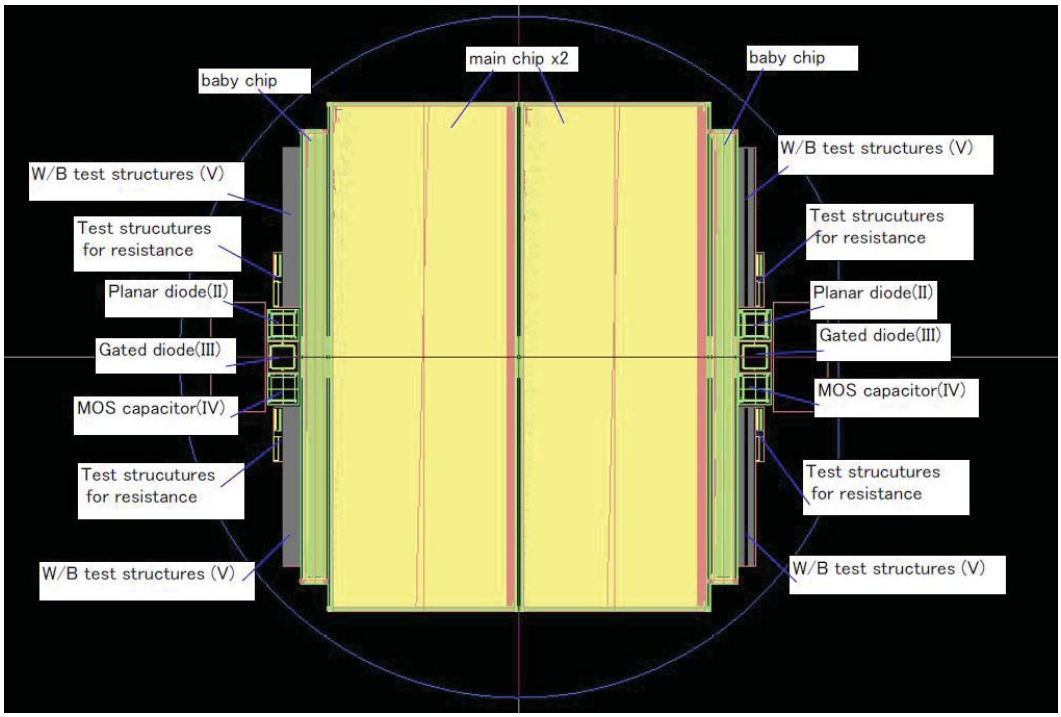


FIG. 4.2.2. Wafer diagram.

Spec. section	Parameter being tested	Test structure name	Structures per wafer
5.8.b	I/V curve	gated diode	4
5.10.b.(i)	measure implant resistance	resistance test structure	4
5.10.b.(ii)	metal and poly-silicon layers	test structure	2
5.10.b.(iii)	currents in the bulk	planar diode	2
5.10.b.(iv)	thickness of dielectric layers	planar diode	2
5.10.b.(v)	depletion voltage and interstrip resistance	planar diode, *baby* sensor	4
5.10.b.(vi)	interstrip, backplane, and total capacitance	planar diode, *baby* sensor	4

TABLE V. Test structures and parameters to be tested.

Of the 607 sensors received, 594 will be used for first article module construction and for module production. The 594 sensors that have been selected out of the 607 sensors do not have any bad channels. Test results from measurements made on all 607 sensors are listed in Table VI.

Specification #	Specification	Specification value		Hybrid	Intermediate	Far
5.8.a	full depletion voltage	40 < V < 100	min	65	65	65
			max	80	85	80
			avg	77	78	72
5.8.b	total leakage current	≤ 10 (nA/cm²)	min	2.0	1.8	2.1
			max	6.8	5.0	6.9
			avg	2.7	2.6	2.8
5.8.c	interstrip capacitance	< 1.2 (pf/cm)	min	0.50	0.50	0.46
			max	0.57	0.55	0.59
			avg	0.52	0.52	0.52
5.8.f	Al electrode resistance on strips	< 20 (Ω/cm)	min	6.51	6.59	6.57
			max	7.60	7.50	7.59
			avg	7.06	6.96	6.96
5.8.k	poly-silicon bias resistor value	1.5 ± 0.5 (MΩ)	min	1.03	1.02	1.09
			max	1.43	1.53	1.53
			avg	1.21	1.19	1.27

TABLE VI. Specification tests done by Jefferson Lab on sensors.

4.3 Strip Layout

The readout strips have graded angles—readout strip #1 is parallel to the longitudinal axis of the module, the *z* axis; the last readout strip, #256, has an angle of 3° with respect to the longitudinal axis of the module. The angle between any two consecutive readout strips increases by $1/85^{th}$ of a degree, a constant φ pitch—this approach minimizes dead areas on the sensor.

Because of the constant φ pitch, the lengths of the readout strips of the modules vary from 0.5 cm to 33 cm. The intermediate strip pitch is 0.078 mm and the readout pitch is 0.156 mm. The strip-to-pitch ratio is 0.256 for all three types of sensors.

In a binary readout architecture, such as the one in the FSSR2 ASIC, each channel generates either a hit (data word) or no-hit (status word) information. The single strip resolution is given by the strip pitch *P*:

$$\sigma_{strip} = \frac{P}{\sqrt{12}} \approx 45 - 58\ \mu m$$

$$\sigma_{\perp} = \sigma_{strip} \times \cos(\alpha) \approx 45 - 58\ \mu m$$

$$\sigma_{||} = \frac{\sigma_{strip}}{\sin(\alpha)} \approx 860 - 1662\ \mu m$$

Since *P,* of the module depends on both the *z* position and the strip number *n*, Fig. 4.3.1, the strip resolution σ_{strip}, in microns, is given by:

$$\sigma(z,n) = \frac{1}{\sqrt{12}}\left(0.156 + z\left[\mathrm{Tan}\left(\frac{n+1}{85}\right) - \mathrm{Tan}\left(\frac{n}{85}\right)\right]\right)$$

where *z* is between 0 and 330 mm and $n \in [1, 256]$.

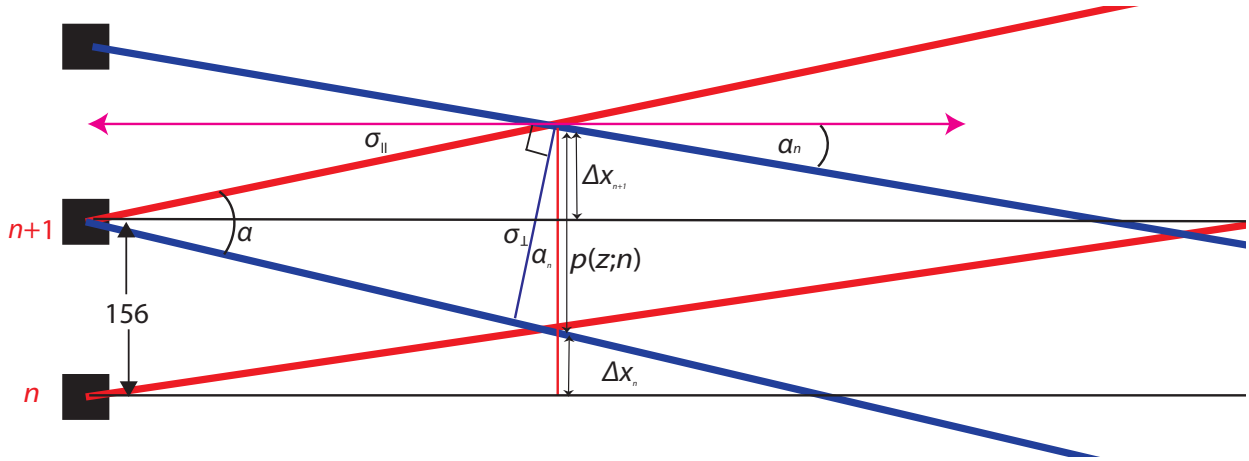


FIG. 4.3.1. Strip layout for the n^{th} and $(n+1)^{th}$ strip. The pitch depends on z position and strip number n.

4.4 Pitch Adapters

To keep the wire bonds straight between the sensor, which has a pitch of 156 μm, and the FSSR2 ASICs, which have a pitch of 50 μm, a pitch adapter is required. There are two fiducials on the pitch adapter edge next to the sensor and three on the edge next to the HFCB to facilitate alignment. The pitch adapter is 41.5 mm by 4 mm, with a tolerance of ±50 μm on both dimensions. A section of the pitch adapter is shown in Fig. 4.4.1.

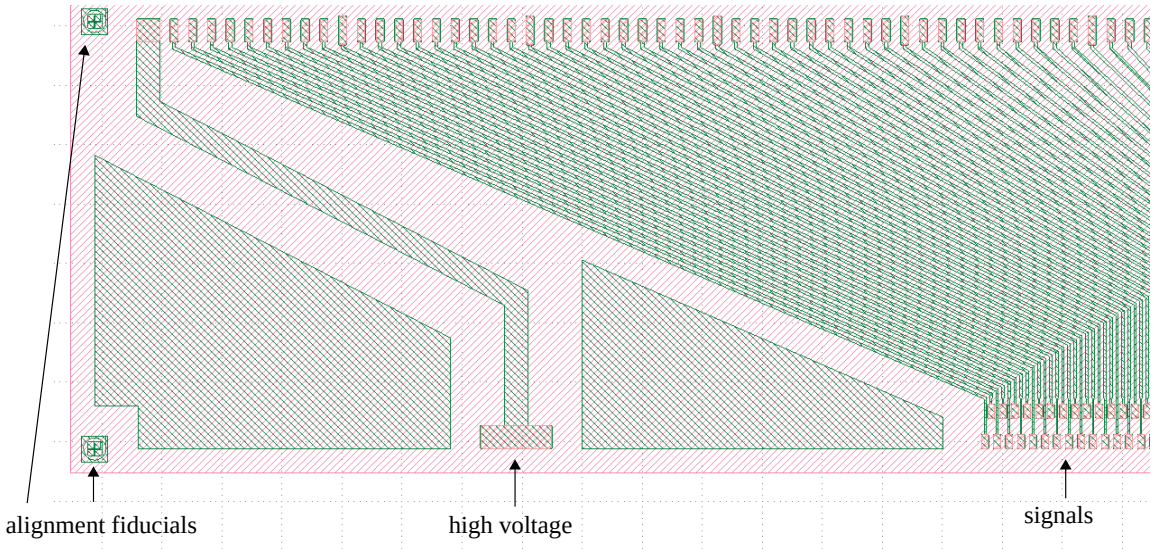


FIG. 4.4.1. One end of the pitch adapter mask, showing alignment fiducials, wire bonding pads, and traces.

The pitch adapter is a glass plate with metal traces made of an alloy of aluminum and copper. The alloy improves electromigration hardness and bonding. The metal layer is sputter deposited. The passivation layer protects the soft aluminum traces from damage and is made from SiO_2, which is better than photoresist. The specifications of the materials used are summarized in Table VII.

Pitch adapter materials		
Type	Material	Thickness [μm]
glass substrate	Nikon NIFS	800 ± 25
metal traces	Al (99.5%) + Cu (0.5%)	1 ± 0.25
passivation	SiO_2	0.5 ± 0.1

TABLE VII. Materials used in the pitch adapter.

The manufacturer, Centro Nacional de Microelectronica (IMB-CNM, CSIC), performed optical tests to check continuity of traces and to find short-circuits. No more than one open trace or two short-circuited traces are allowed per pitch adapter.

5 Modules

The module backing structure, which is a composite panel consisting of carbon fiber skins and a Rohacell 71 core, supports the sensors, the pitch adapters, and the HFCB, Fig. 5.1. The carbon fiber skin is made from K13C2U fibers oriented in a quasi-isotropic (45/-45/0) pattern. It is co-cured with the bus cable, which is made from Kapton sheet with 0.003-mm thick copper traces, which are 0.5 mm wide; on one side the traces that provide high voltage to the sensors, on the other side they form a 5.5 mm x 5.5 mm copper mesh over the entire area for grounding the carbon fiber. The Rohacell core under the HFCB is replaced by a copper heat sink to remove ~2 W of heat generated by the four FSSR2 ASICs on a module.

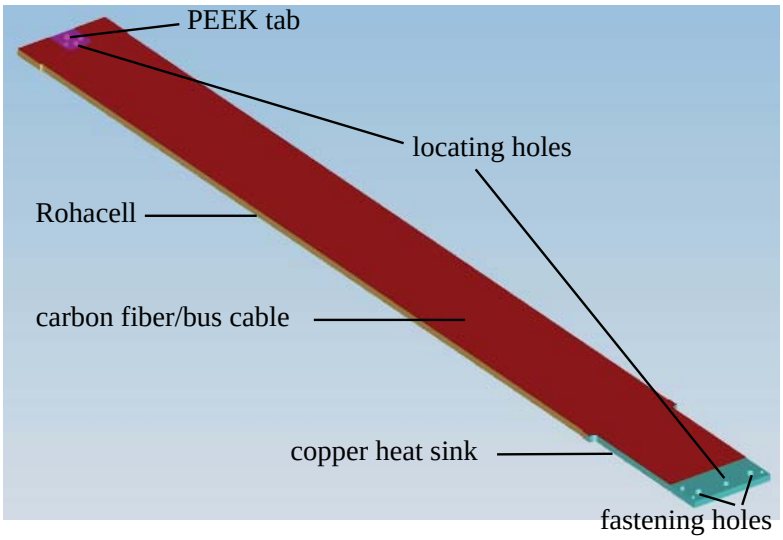


FIG. 5.1. Module backing structure.

The sensors, the pitch adapters, and the HFCB are glued with Huntsman TDR 1100-11 resin/hardener to both sides of the backing structure. The HFCB is wrapped around the backing structure with a flexible fold-over cable, the wing cable, Fig. 5.2. The copper heat sink, located under the hybrid area of the HFCB, is machined with holes that are for mounting and surveying the upstream end of the module.

At the downstream end of the module, the Rohacell core is replaced by a polyether ether ketone (PEEK) core. PEEK is machinable, moldable, and radiation resistant, characteristics well-suited to a silicon detector's environment. The PEEK core has machined holes that are used for locating, surveying, and handling the module, as well as allows the module to be positioned between the upstream and downstream rings of the detector without over-constraining the module. The module has two fiducial holes in the copper heat sink and one in the PEEK tab. After the module is fabricated, the position of these fiducials will be measured with respect to the fiducials etched on the sensor and the data will be recorded to be used during detector software calibration.

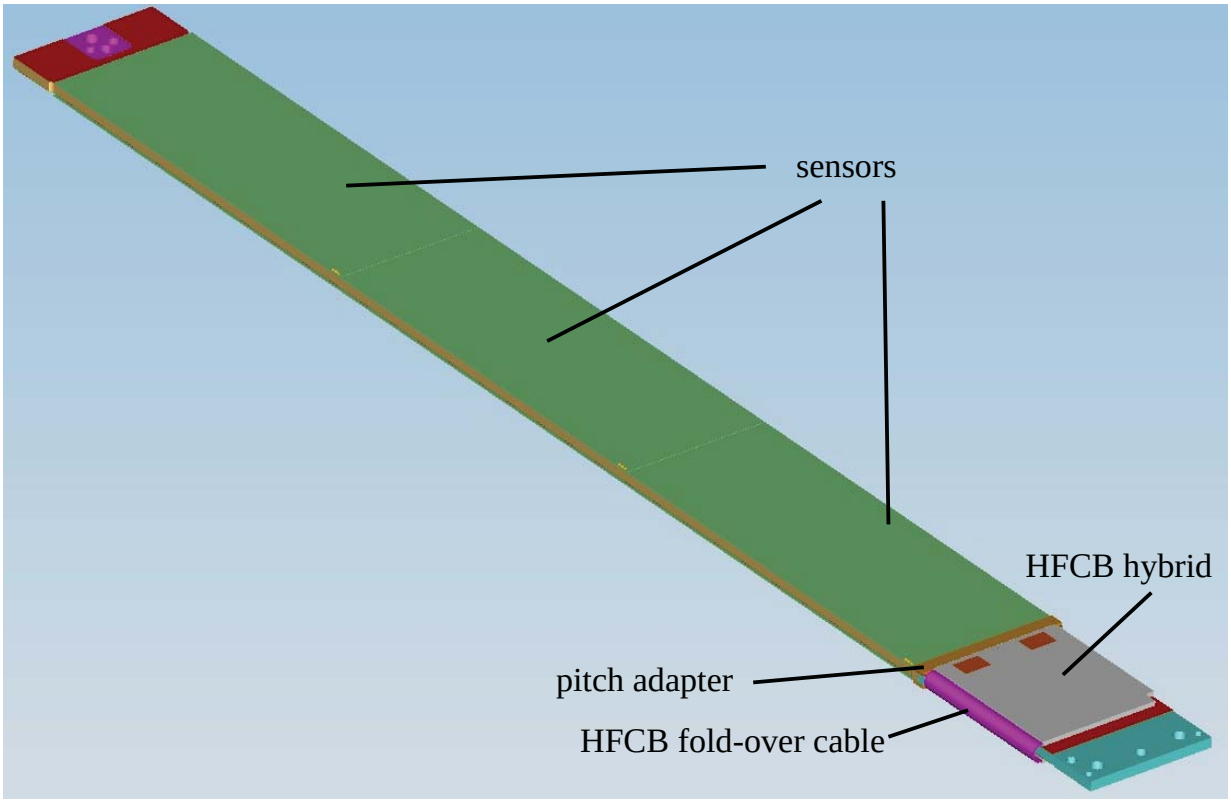


FIG. 5.2. Module.

Table VIII gives the thicknesses and radiation lengths of the materials used for the module structure. The total radiation length X_0 of a module is ~1%.

Material	Radiation length [mm]	Thickness [mm]	Thickness [%X_0]
Silicon	93.700	0.320	0.342
Epoxy	443.700	0.100	0.023
Bus cable	14.3	0.031	0.217
Carbon fiber K13C2U	250.000	0.190	0.076
Rohacell 71	4500.000	2.500	0.056
Carbon fiber K13C2U	250.000	0.190	0.076
Bus cable	14.3	0.031	0.217
Epoxy	443.700	0.100	0.023
Silicon	93.700	0.320	0.342
Total per module [%X_0]			1.372

TABLE VIII. Material thicknesses with radiation lengths for the different layers of the modules.

Figure 5.3 shows a portion of the layout of the module mask between two sensors. On each side of the module's backing structure, three sensors, one of each type, are placed with a clearance of 110 ± 10 μm between the sensor edges. Wire bonds connect the readout strips of the sensors, connect the sensors to the pitch adapter, and the pitch adapter to the associated FSSR2 ASICs. The spacing between the pitch adapter and the sensor and the pitch adapter and the HFCB is 500 μm $^{+110\ \mu m}_{-90\ \mu m}$ and 300 μm $^{+150\ \mu m}_{-50\ \mu m}$, respectively.

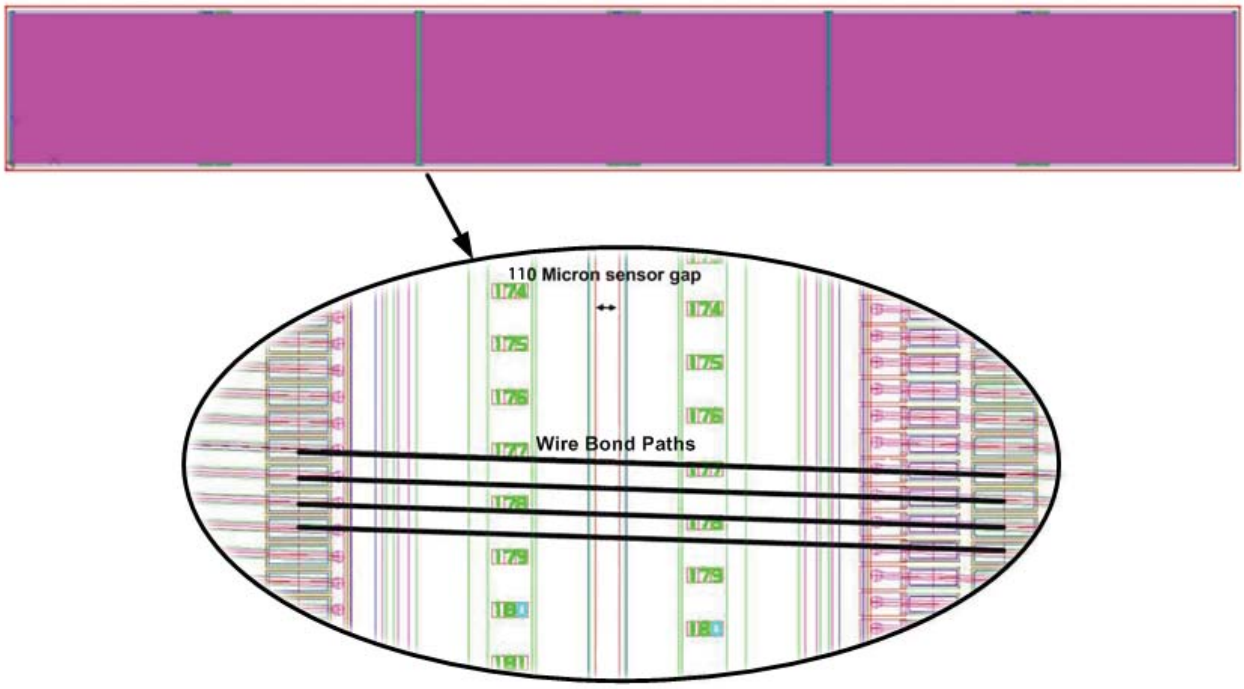


FIG. 5.3. Area of sensor mask layout between two sensors.

Figure 5.4 shows the readout strip pattern on the module. The red lines, *V* strips, are the readout strips on the top side of the module, layer *B*; the blue lines, *U* strips, are on the bottom side of the module (closer to the beam), layer *A*.

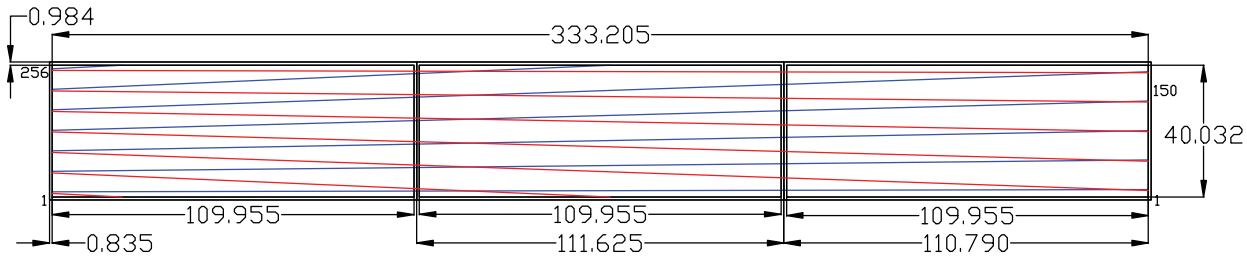


FIG. 5.4. *U* (blue lines) and *V* (red lines) strips on a module. (All units in mm.)

5.1 Deflection

Structural finite element analysis of the module was done with ANSYS v11 to calculate the deflection due to the gravitational load on a module. At the upstream end, the module was assumed to be fixed because it is fastened to the upstream support ring of the detector. At the downstream end, a simply supported condition was assumed because the module is supported by the downstream ring, which is not rigidly attached to a structure. The weight of a module was taken to be 84 gm. An additional weight of 20 gm for the HFCB was added as a static load. The deflection of an individual module is shown in Fig. 5.1.1. The maximum deflection of ~14 μm is for the horizontal orientation of a module and is roughly halfway between the upstream and downstream ends of the module.

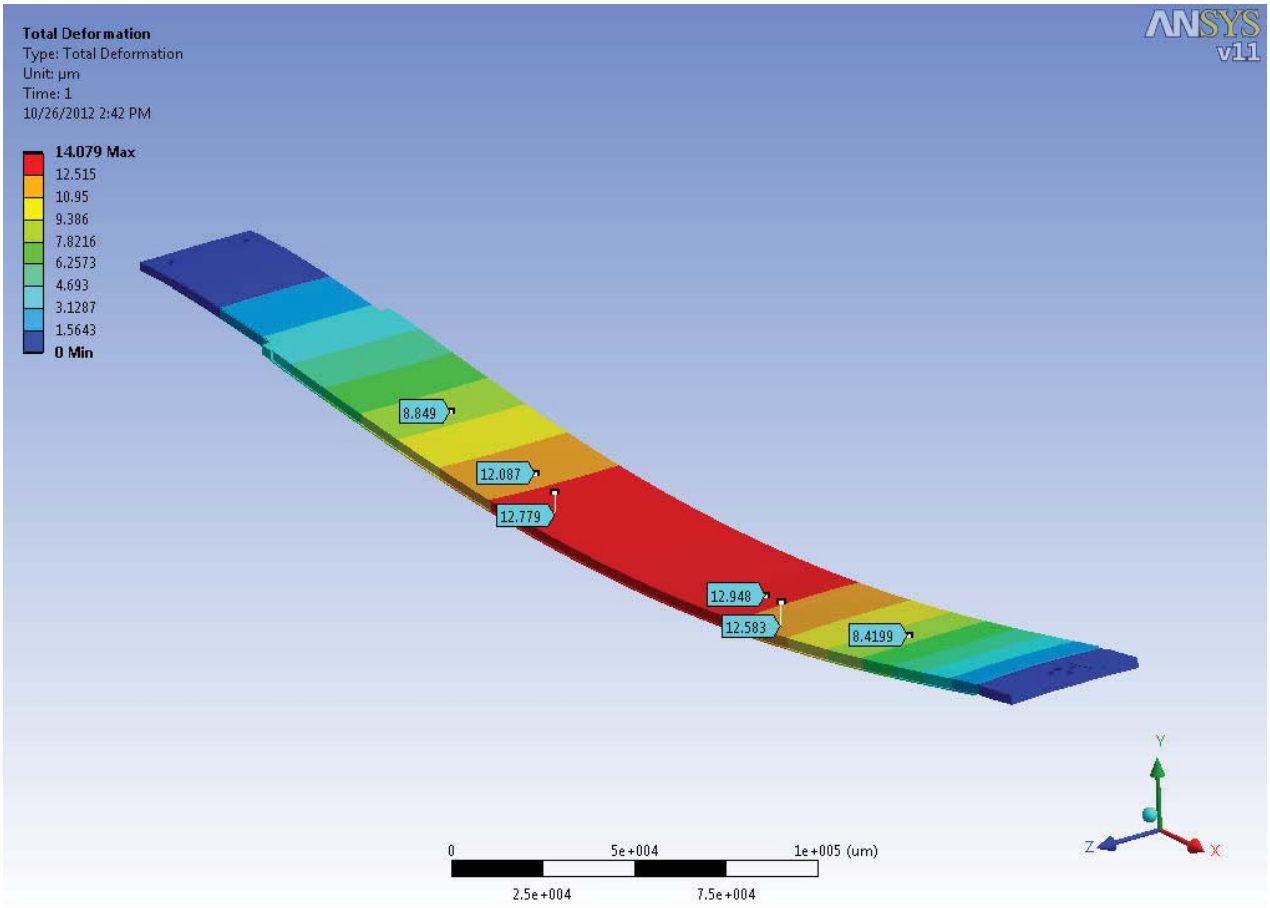


FIG. 5.1.1. Deflection of an individual module, due to gravity.

5.2 Thermal Analysis and Heat Removal

For the thermal analysis, the module was modeled with the copper support and the heat sink insert. The heat output from each module is ~2 W. Cooling the cold plate with water, which flows around the fins of the heat sink inserts inside the cold plate at 15°C, at a rate of 2 LPM, results in a temperature differential of the water between the inlet and outlet of the cold plate to be < 1° C.

The temperature distribution on the module is shown in Fig. 5.2.1. The maximum temperature on the FSSR2 ASICs is ~28°C. The maximum temperature of the sensors at the readout end is ~21.5°C. The variation in temperature from the upstream end of the Hybrid sensor to the downstream end of the Far sensor is ~1°C.

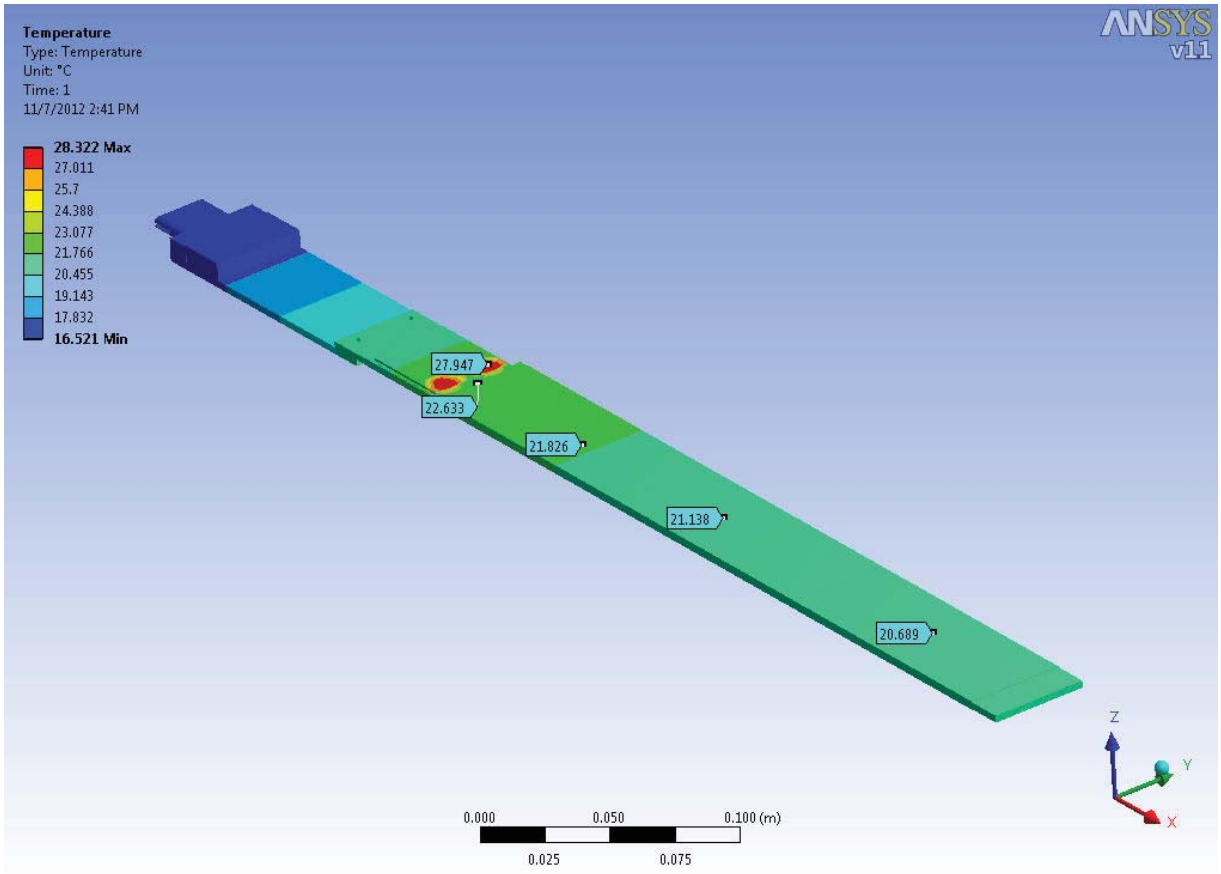


FIG. 5.2.1. Temperature distribution in module.

5.3 Module Assembly

For production, a set of detailed assembly procedure documents has been developed to aid the assembly work.

Upon receipt at Fermilab, the HFCBs, which have already been populated with components, except for the FSSR2 ASICs, and have been tested electrically will be stored in Lab D.

FSSR2 ASIC wire bonding on the HFCBs will be performed with the aid of wire bonding maps because bonding of each FSSR2 ASIC is slightly different to properly register the FSSR2 ASICs' IDs. Electrically-conductive epoxy, Tra-duct 2902, will be used to connect the underside of the FSSR2 ASICs to the metallized mounting pad on the board. To place the FSSR2 ASICs in an accurate and repeatable way, a small, setup fixture will be used. The FSSR2 ASICs will be located on the base plate and then transferred to the HFCB with a vacuum pickup fixture. Wire bonds on the HFCB, except for those that go to the pitch adapter, will be encapsulated with the Dow Corning product Sylgard 186.

It might be possible to incorporate some features in the HFCB storage box that is to be built to allow placement of the FSSR2 ASICs to be done without having to remove the HFCB from its box, thus eliminating extra handling. Additionally, the HFCB storage box will provide protection to a fully wire bonded and assembled unit and will be used as a robust shipping container. The issue of HFCB storage has been addressed so that the HFCBs will be handled, tested, and stored in a safe manner during the production workflow.

Prior to installation on a module, fully-assembled HFCBs will be tested to verify quality. Testing of the fully-assembled HFCB will be done while it is in its box. In February of 2012, the assembly and testing work was done successfully on two HFCBs that were part of the electrical-grade module.

Upon receipt at Fermilab, the backing structure parts will be stored in Lab 3. All parts will be inspected with go/no-go gauge pins to check the size of precision alignment holes and a caliper or micrometer will be used to check thickness. A percentage of the parts will be checked on the CMM to evaluate their flatness. Inspection results will be logged.

The bottom surface of the bus cable contains a mesh which is used to ground the conductive carbon fiber skins. Since simply gluing the cable to carbon fiber lamination does not provide adequate electrical conductivity, the cable is co-cured into the carbon fiber lamination at the same time the lamination is prepared. By introducing the cable prior to curing the prepreg epoxy, the electrical connectivity between the ground mesh and the fibers is maximized. Figure 5.3.1 shows the carbon fiber/bus cable lamination process. Hence, the first step in fabricating the backing structure is to co-cure the bus cable panel to the carbon fiber skin, which has cynate ester prepreg, during ply layup.

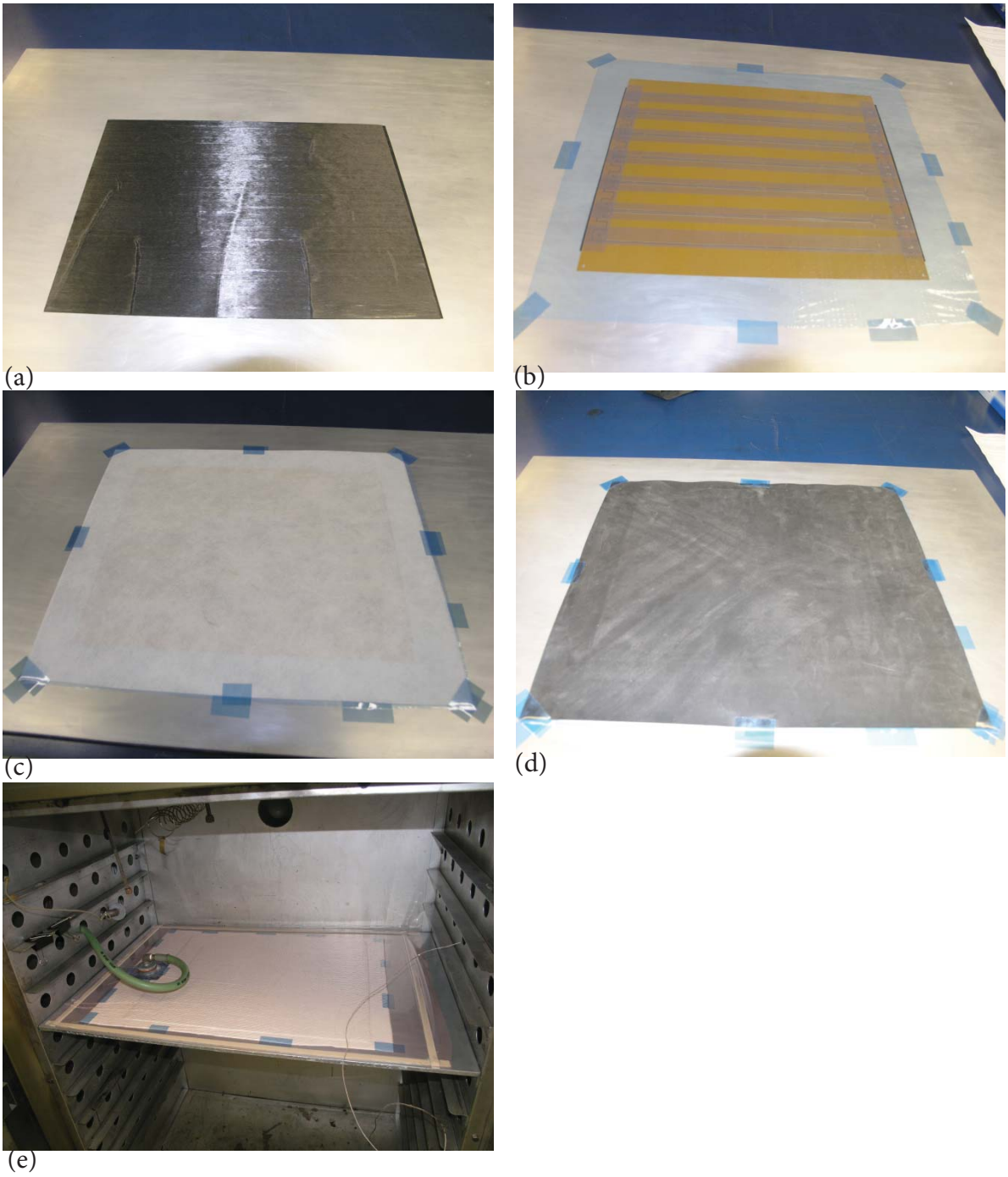


FIG. 5.3.1. Building of carbon fiber skin (a) carbon fiber prepreg, (b) bus cable, (c) bleeding cloth, (d) laminate covered with caul sheet, (e) vacuum forming of carbon fiber/bus cable laminate.

The top layer circuitry of the bus cable connects the bias voltage to the underside of the sensors. Pads on the upstream side of the bus cable are connected to bias voltage pads on the HFCB and traces route this voltage to two pads under the first sensors, where spots of silver-filled epoxy Traduct 2902 will be used to provide contact to the back of the sensor. To connect sensor to sensor, two sets of these silver-filled epoxy pads are used. Artwork has been added at the downstream end, beyond the far sensor, for the addition of a surface mount capacitor between the bias voltage and ground.

Carbon fiber of Mitsubishi type K13C2U will be used for the backing structure skins. The carbon fiber will be a prepreg with a Cyanate Ester resin that cures at 250–275°F and which is free of halides, high-Z components, and additives. The two opposing skins on a single backing structure have two different lamination stack-ups. The stack-up on the composite structure is: carbon fiber (+45°/−45°/0°), Rohacell, carbon fiber (0°/−45°/+45°); 0° is along the length.

Since the two cut skins will be indistinguishable, to distinguish them, one corner on each of the skins will be clipped. The upper and lower right corners will be clipped on the top and bottom skins, respectively. When mated back-to-back to form a backing structure, alignment of the trimmed corners will ensure that one of each type of skin was used. To aid this visual cue, the corner of the Rohacell will be trimmed to match as well. The written assembly procedure specifies alignment of these corners to ensure the correct final configuration. The backing structure drawing defines this instruction.

Bus cable/carbon fiber cutting will be similar to the process used in Sept/Oct of 2011 to make the prototype skins. The layout of six bus cables on a panel has a minimum of 5.05 mm between adjacent cables on the panel. This spacing is sufficient for the 1/8-in. diameter routing bit plus a small amount of additional material to be left on the skins for post-machining at the backing structure level , Fig. 5.3.2. Completed sheets will be cut to shape by the CNC routing group in Lab 8. A drawing will be prepared for use in programming the cutting of multiple skins from a single sheet.

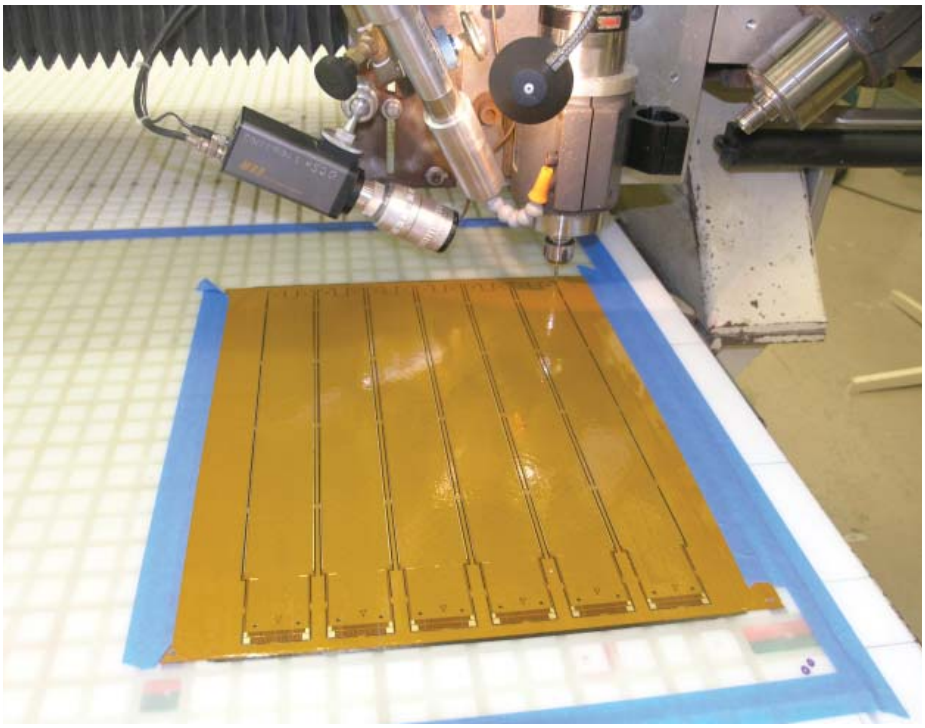


FIG. 5.3.2. Cutting of the bus cable.

Next, the Rohacell core will be cut to size by a CNC routing shop. Some additional material will be left on the cutting profile. This additional material will be removed during a post-machining process on the backing structure, which is necessary to achieve the width tolerances.

To assemble the backing structure, a mold and 3M Scotch-Weld 2216 epoxy that cures at room temperature will be used. The base plate of the mold is flat and contains precision features for pinning and fastening the copper and PEEK inserts in place, as well as locating pins and threaded fastening holes to align and mount other portions of the mold. The perimeter plate, which is thicker than the backing structure and whose thickness must be precisely controlled, will mount on top of the base plate and will have a cutout in the shape of the backing structure. The shim sheet, a thin stainless steel sheet, will have a profile cut to accommodate the inner carbon fiber/bus skin, which is slightly offset from the plane defined by the module mounting surfaces. The spacer plate will fit inside the cutout in the perimeter plate and will be placed above the backing structure components. The spacer plate thickness must be precisely controlled because the final backing structure thickness will be the thickness of the perimeter plate minus the thickness of the upper spacer and the shim sheet. The spacer plate is needed because the perimeter plate must be significantly thicker

than the backing structure itself, otherwise it will be difficult to position the outer skin. The top plate caps off the top of the mold and when fastened in place, applies pressure during epoxy curing to the backing structure components. Mold release applied to the various pieces will be used to keep the backing structure from sticking to the tooling.

The assembly sequence will be as follows: the perimeter plate would first be installed on the base plate. Then the shim sheet, lower carbon fiber skin (with a thin layer of epoxy already applied), PEEK and copper inserts, Rohacell foam (with some epoxy on its edges where it butts up against the copper and PEEK inserts), and upper carbon fiber skin (again with a thin layer of epoxy applied). The spacer plate is then put in place and the top plate installed. After the epoxy has cured overnight, the fixture is disassembled to expose the completed backing structure, which will then be visually inspected and excess epoxy will be removed. Once ready, the backing structure will be stored in a specially designed container to protect it from damage.

Holes in the backing structure are provided for handling, positioning, fastening, and as fiducial references. The hole for the mounting pin has a tight diameter tolerance and is used as a key feature in defining the alignment of the module. Copper is used for thermal conductivity in the region of the hybrid, where radiation length is not a concern. During assembly, pin engagements in this hole are limited to minimize the amount of wear on this feature. The fiducial holes need not be well-positioned, but their use as metrology reference features demands that they are accurately machined roundness and perpendicularity. The etched serial number used to mark the part can be used as the serial number assigned to each module during production. At the downstream end of the module, the Rohacell core is replaced by PEEK plastic. The slot in the PEEK insert has a tolerance of ± 5 μm.

To accurately control the width of the backing structure, post-machining of the width at the downstream end and near the pitch adapter will be done. A jig has been fabricated to hold the backing structure in place during machining. The precision hole and slot in the backing structure will be pinned to the jig to accurately register its position.

After post-machining of the precision edge, any foam exposed due to that process will be encapsulated with 3M DP190 epoxy. This application will be done by hand, with care to minimize the migration of DP190 to unwanted areas. A visual check will be made of the core. Thickness will be measured at several locations with calipers and results recorded on the traveler. The backing structure will be fastened to a precision-flat inspection plate in such a way that only the copper and PEEK mounting surfaces will contact the plate and the OGP CMM will then be used to measure the following features: locating hole and slot measured to establish a coordinate system, slot straightness measured relative to the coordinate system, edge locations along width measured in tight-tolerance areas near pitch adapter and PEEK insert, and grid of flatness points measured with autofocus on the surface of the bus cable.

The backing structure will be mounted on a base plate with features to register its position. After masking the appropriate regions, TDR 1100 epoxy will be spread on the backing structure. The top half of the HFCB, to be located using pins with the board's temporary alignment tabs, will be placed on the backing structure and clamped during curing. Temporary tabs will be used to aid module assembly, after which these tabs will be removed. The center-point positions of the four holes in the tabs are dimensioned relative to each other and to the edges of the hybrid board. During wire bonding, bias and ground connections are made from the back end of the HFCB down to the bus cable. It may be desirable to replace these wire bonds with soldered-on strips of copper foil. Provisions have been made for this choice, as well as for the placement of a capacitor between bias and ground at the downstream end of the module. The pitch adapter will be placed on a loading plate, which is part of the main base plate, and picked up with a pin-guided vacuum transfer bar. The bar then engages a matching set of features on the base plate to set the pitch adapter location. The front and rear ends will be open to inspect for epoxy runout. After curing, the temporary tabs on the HFCB used for positioning will be removed.

The setup will be flipped for repeating the process on the bottom side. The base plate will have clearance cutouts for the previously-glued items as well as the still-unbent portion of the HFCB. After spreading the TDR 1100, the HFCB will be folded over, its position will be set with pins in its temporary tabs, and it will be clamped in place. Once the HFCB has been placed, the pitch adapter will be placed as described above. This procedure requires two overnight epoxy curing steps.

There exists the possibility of using soldered copper strips rather than wire bonds for the bias connections between the HFCB and the pads at the upstream end of the bus cable. If such connections are to be incorporated, this step will be performed at this point in the process, before the installation of the sensors.

After installation of the HFCBs and pitch adapters, the module will be stored in a box to protect the module's sensitive features. Loading and removal of a module will cause minimal handling risks. To minimize the wear on the module's precision alignment features, these features will not be used for mounting the module into the box. The box will be designed to allow storage of partially and fully fabricated modules. The areas near wire bond connections will be accessible for inspection and laser testing. The box will provide protective support of the HFCB cable without

folding. There will be thermal contact between the module's copper insert and a feature of the box so that it can be cooled externally. The box will securely restrain a complete module during shipping to Jefferson Lab. The quantity of boxes produced will match the total number of modules to be produced.

The backing structure will be mounted into a sensor installation fixture plate with its location set by precision alignment pins and secured with vacuum. The plate is also equipped with several optical fiducials that are precisely positioned on the fixture such that the alignment pin holes' locations are known relative to the fiducial locations. This setup will be mounted on a Ziess UMM 500 CMM equipped with a microscope camera. This fixture is used also to hold the module during wire bonding. The entire fixture with the module is mounted to a wire bonding fixture.

Tape masking is applied to selected regions of the exposed bus cable surface and the epoxy (TDR 1100) is applied and leveled. With the masking tape removed, spots of silver-filled epoxy (Tracon 2902) are applied to the pads on the bus cable.

Before starting sensor alignment, the CMM is used to establish a coordinate system traceable to the module's mounting features. On the upstream end, this cannot be done directly since the HFCB pigtail covers the mounting hole. Therefore, the two optical fiducials, whose position is known relative to the mounting point on the fixture, will be used to establish the coordinate system at this end. At the downstream end, the sides of the slot in the PEEK insert are viewable. Similar sets of optical fiducials could be added to the fixture as an alternative to establish the coordinates.

The technique used to position the three sensors is adapted from the process developed for the PHENIX detector at BNL. The sensor is picked up by a frame that plugs into the fixture base and uses micrometer heads to adjust the sensor position once the frame is locked into place. Positioning is performed with the CMM to locate the sensors in a coordinate system based on the backing structure. An IDEAS model of the frame to be used for sensor placement is shown in Fig. 5.3.3.

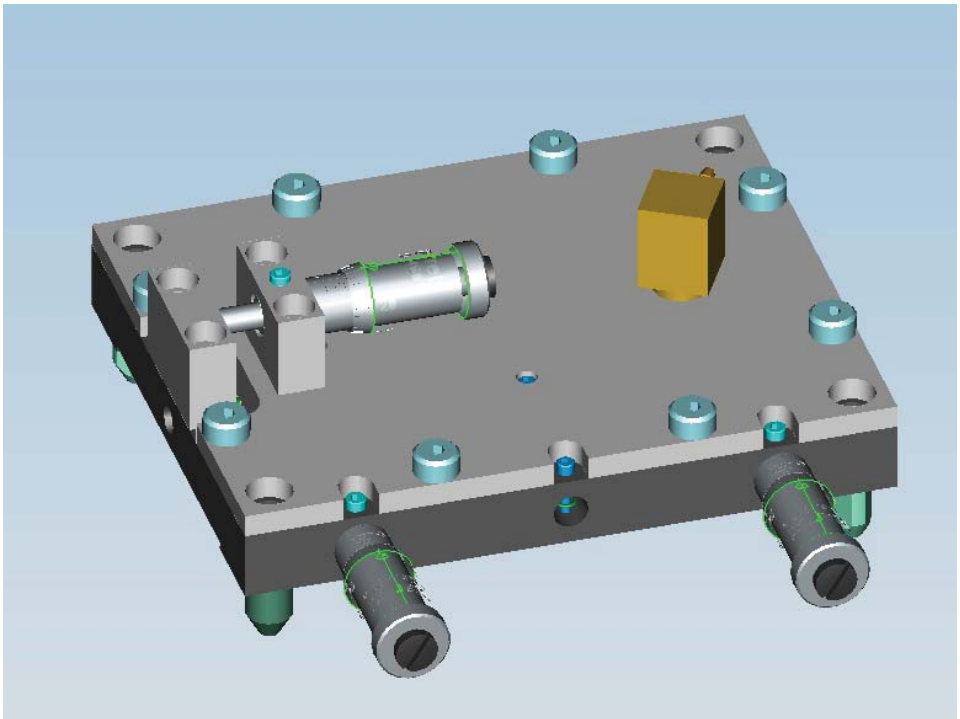


FIG. 5.3.3. Sensor alignment fixture.

The frame will be used to pick up the sensor from a loading plate, which holds the sensor in place with vacuum, with its edge butted up against the retractable pins. After lowering the pins, the frame vacuum is applied, the loading plate vacuum is terminated, and the frame is used to transfer the sensor to the backing structure. The sensor positioning on the loading plate would be set such that the silicon would start off a little too far from the HFCB when first placed, thus providing a little extra clearance when installing adjacent sensors. The frame's positioners would then be used to meet the required tolerances.

The frame's pin engagement with holes in the fixture plate supporting the module will set its initial alignment. Set screws will lock the pins in place for stability and a weight placed on top of the frame will help seat the sensor in the epoxy. Then the optical CMM will measure the fiducials in the exposed corners of the silicon and the micrometer heads will be adjusted to steer the fiducials to their desired locations. After the process is repeated for all three sensors, the alignment will be rechecked and then the epoxy would be allowed to cure overnight.

After subsequent removal of the positioning frames, a temporary cover will be installed over the module. The fixture base plate holding the module will be moved within the Lab D clean room to the OGP CMM for final inspection of the tolerances. The required sensor placement tolerances, based on calculations and simulations, are: φ direction ±30 μm, r direction ±750 μm, and z direction ±150 μm. Locations of the sensor fiducials and the reference holes in the copper and PEEK inserts will be measured in the module's coordinate system.

It is expected that the silicon-to-silicon φ-direction relative alignment on a single side of the module will be significantly better than the required value. Some variation is expected for the position of the silicon relative to the mounting features. These effects, combined, are expected to satisfy the specifications through use of precision fixtures and by using the precision of CMMs to aid sensor installation.

The z-direction alignment is expected to be achieved. Again, the combined effects of sensor relative alignment and alignment relative to the module mounting features are expected to satisfy the requirements by use of precision fixtures and by using the accuracy of CMMs to aid sensor installation.

The r-direction locations within a module will depend on thicknesses of the various material layers used to construct the module. Deviations from nominal material thicknesses will arise due to deviations of individual components, for example carbon fiber ply.

The sensor locations on each side of the module will be inspected on an optical CMM in a coordinate system related to the module's mounting features. The three fiducial holes in the backing structure also will be measured in this coordinate system. These CMM inspection reports will be transmitted to Jefferson Lab for use in modeling the as-built detector alignment. After this inspection, the module will be ready for wire bonding.

With a fixture serving as both assembly fixture and wire bonding fixture, it will be difficult to accommodate an accelerated production rate with only one set of tooling. For a faster assembly rate, multiple fixture bases will be made.

To minimize module handling, the support plate from the sensor installation jig also serve as a support during wire bonding; the tooling design will accommodate this feature. The sensor placement and wire bonding process of the bottom side will be similar to the steps described above for installation of sensors on the top side of the module. On the bottom side, the mounting hole and slot in the backing structure's copper and PEEK inserts are both visible. It is therefore desirable to use these features directly in establishing the coordinate system on the CMM.

Full characterization of the module's performance will be done after encapsulation. After bonding, the module is transferred into its storage box and is ready for testing. It is intended that the module storage box will double as a shipping container for an individual module. Groups of modules in their storage boxes will be packed together with a desiccant, wrapped in ESD-safe plastic, and shipped in a foam-lined shipping container. The crate could be strapped to a pallet to facilitate handling. "Traveler" paperwork will also accompany each module during production to record the specifics of assembly.

A secure way to handle the shipping would be to use a dedicated air-ride truck from Fermilab to Jefferson Lab. The DES telescope camera was sent by dedicated air-ride truck from Fermilab to Miami in November of 2011.

Aspects of the workflow for the assembly of the module were input back into the design at several levels. For instance, the bus cable layout on a panel was based on the co-curing of the bus cables with the carbon fiber (for electrical grounding) and on the CNC-cutting of completed sheets into individual skins for backing structure fabrication. Several elements of the workflow were performed during the construction of the two electrical-grade prototype modules fabricated at Fermilab. Other elements, for example the inclusion of the precision mounting features into the backing structure, will be incorporated into the final assembly techniques used for production.

6 Support and Cooling Structure

The four regions of the SVT, are cantilevered off a water-chilled cold plate that is designed to remove the heat generated by the electronics, which are located at the cold plate end of the detector. External cooling has been chosen over internal cooling—tubes in the modules—to preclude the noise problems associated with modules that have internal cooling tubes [7,8] and to keep the amount of material in the active area as low as possible.

The support tube will be mounted on the solenoid cart. The HFCBs will be routed through slots in the cold plate

that have a 10-mm radial opening and will be attached to the support tube. Data, high/low voltage, pulser, and slow controls cables will be routed along the surface of the support tube to electronics racks located in the insertion cart located on the space frame.

The modules will be mounted between an upstream and a downstream ring. Each region's upstream ring will be attached to the cold plate; these rings are independent of each other. The mounting surfaces of the upstream and downstream rings will be machined in a single step, to guarantee planarity to each other and to reduce twist forces on the module, which result if the two surfaces are non-coplanar. The holes for the locating pins and tapped holes for fasteners on the upstream and downstream rings are machined at this stage as well. The downstream rings will be independent, not constrained. Figure 6.1 shows the assembled R2 of the detector.

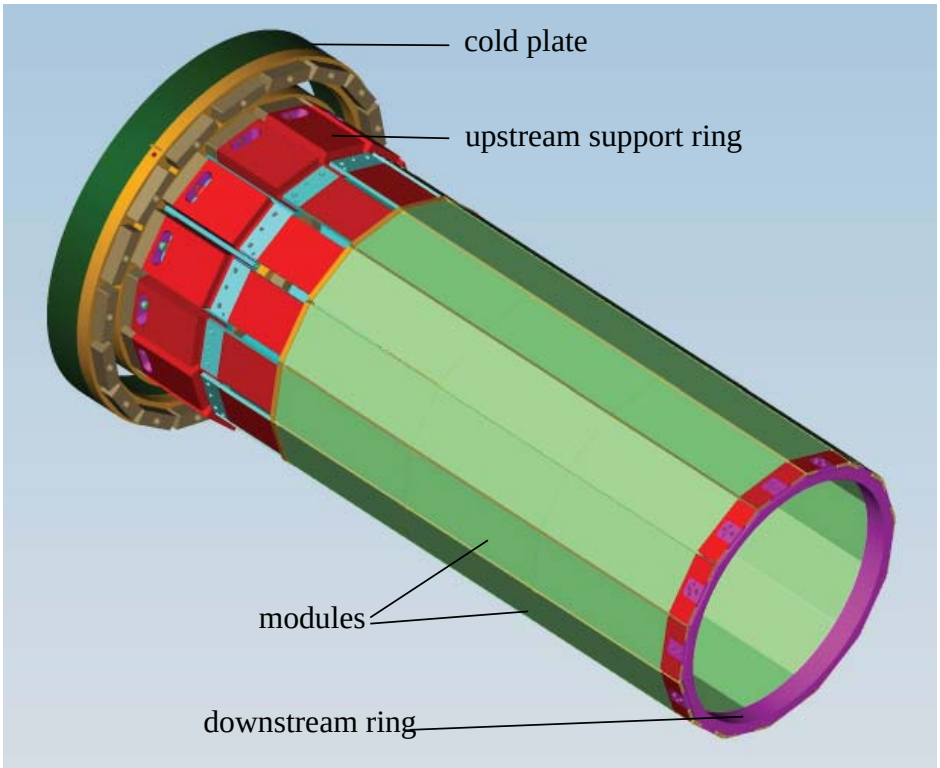


FIG. 6.1. Assembled R2.

The cold plate, Fig. 6.2, includes two plates made from Noryl filled with 30% glass, glued together, and plugged with finned copper inserts. One plate is machined with a spiral cooling channel and the other plate with slots for the copper inserts, and the entire cold plate has machined slots through which the HFCBs will be routed.

The upstream support ring consists of a copper module-mounting surface glued to the polygonal Noryl ring, Fig. 6.3. The upstream support ring is attached to the cold plate's copper inserts with screws and provides a mounting surface for the modules on the upstream end of the detector and a conduction path for heat to be transferred from the modules to the water flowing through the cold plate. The upstream support ring, Fig. 6.3, is fastened to the cold plate by a single screw that goes through each of the copper module supports. This ensures good thermal contact between the inserts on the cold plate and the module supports. A layer of thermal grease, Arctic Silver, will be applied between the mating surfaces.

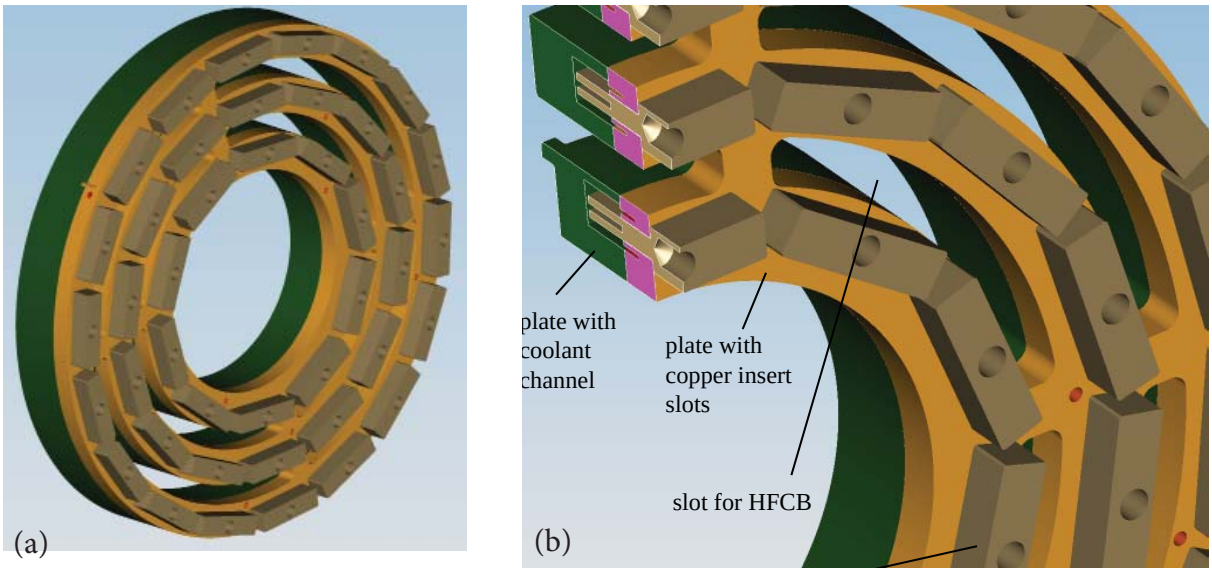


FIG. 6.2. Cold plate assembly. (a) full assembly, (b) close-up section.

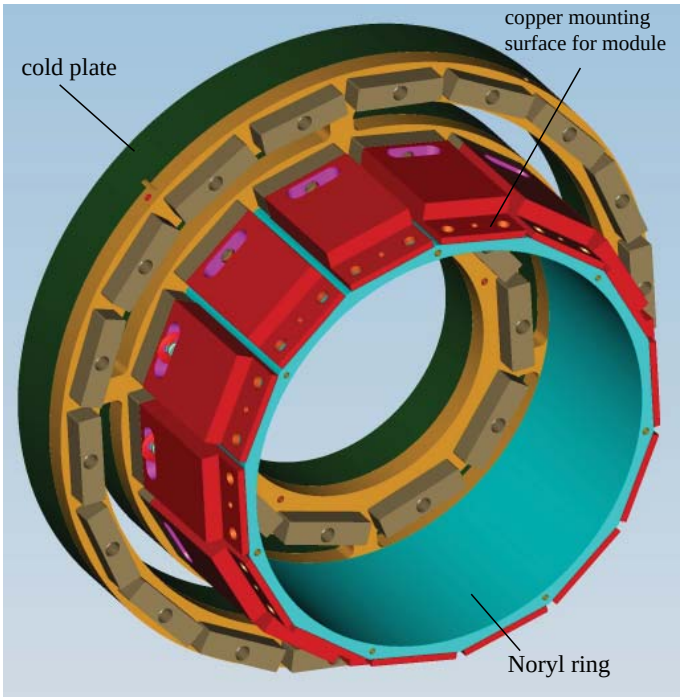


FIG. 6.3. Upstream support ring attached to cold plate.

The downstream rings of each region are independent from each other, Fig. 6.4. Such a design prevents over-constraining the detector assembly. Modules in the vertical and near vertical orientation around the barrel provide stiffness to the region. Downstream rings will have holes for accommodating dowels and screws for locating and mounting the module on the downstream end.

A slot will be machined into the module to accommodate the locating dowel. This slot does not constrain the module in the axial direction, only in the tangential direction. Other holes on the downstream end of the module will be used for surveying the module's location and for handling the module during assembly.

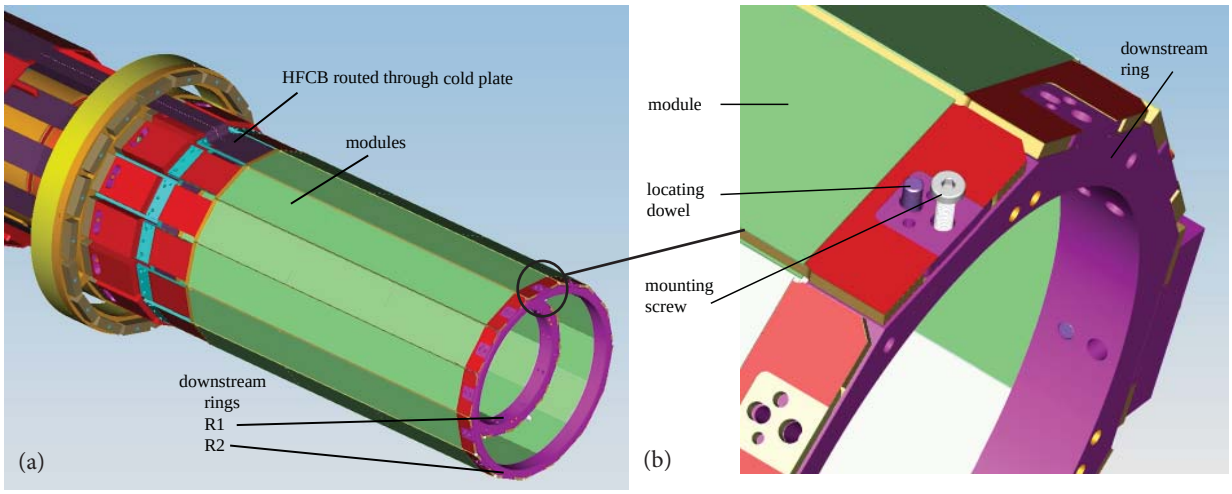


FIG. 6.4. (a) Assembled R1 and R2 (b) close-up of downstream ring.

Since the upstream support ring for a region can be detached from the cold plate and the downstream ring is an independent ring, this design allows an entire region to be removed as a unit, rather than module by module.

6.1 Support Structure Deflections and Vibrations

The deflection, due to gravity, of a region is calculated with all the modules in a region fixed at the upstream end and attached at the position of the fasteners at the downstream end. The results are shown in Fig. 6.1.1. The maximum deflection of a module in this case, considered as a part of a region, instead of as an independent entity, is ~16 μm, similar to the analysis of an individual module. The deflection of the downstream ring is <7 μm. The deflection of the entire SVT once it has been attached to the support structure is ~230 μm.

Vibrational analysis shows that the fundamental frequency of the module is 144 Hz and that of the entire SVT, 30 Hz.

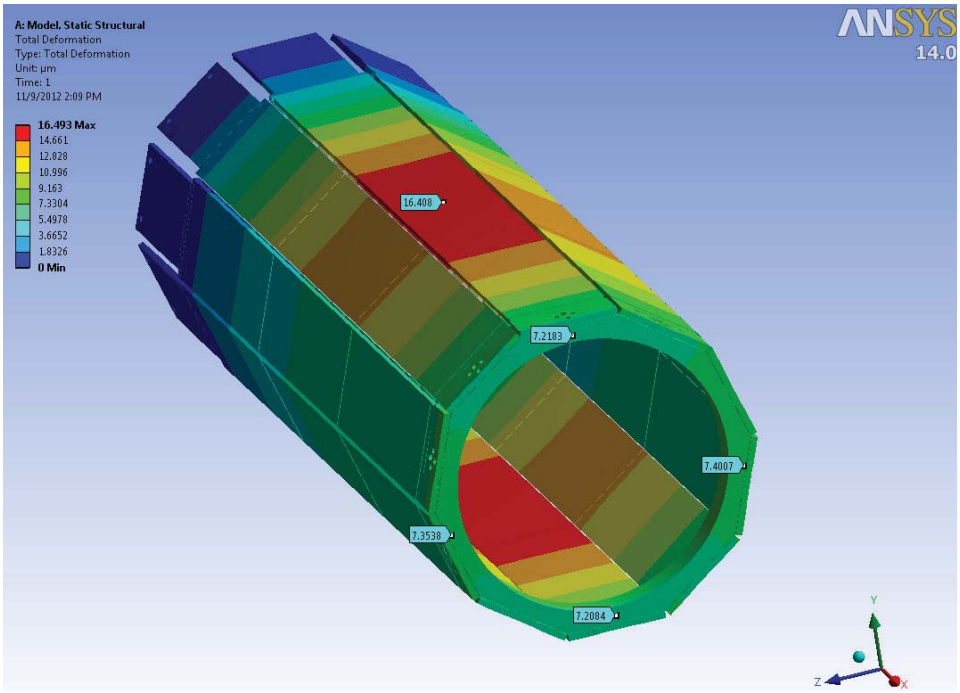


FIG. 6.1.1. Deflection of assembled R1.

6.2 Detector Assembly Sequence

R1–R4 will be assembled in sequence. The assembly will be in a vertical position on a granite table. Surveying will be done using a FaroArm Quantum CMM.

The cold plate and upstream ring will be mounted to a mounting tube. The larger flange on the mounting tube will be on the granite table. The downstream ring then will be positioned by means of four aluminum bars, which will have precisely-positioned holes and mounting surfaces to position the downstream ring. There will be a removable aluminum tooling plate fastened to the downstream ring that will provide stiffness to the ring during assembly and handling. This tooling plate will be removed when all modules of the region have been assembled. The assembly sequence is illustrated in Fig. 6.2.1.

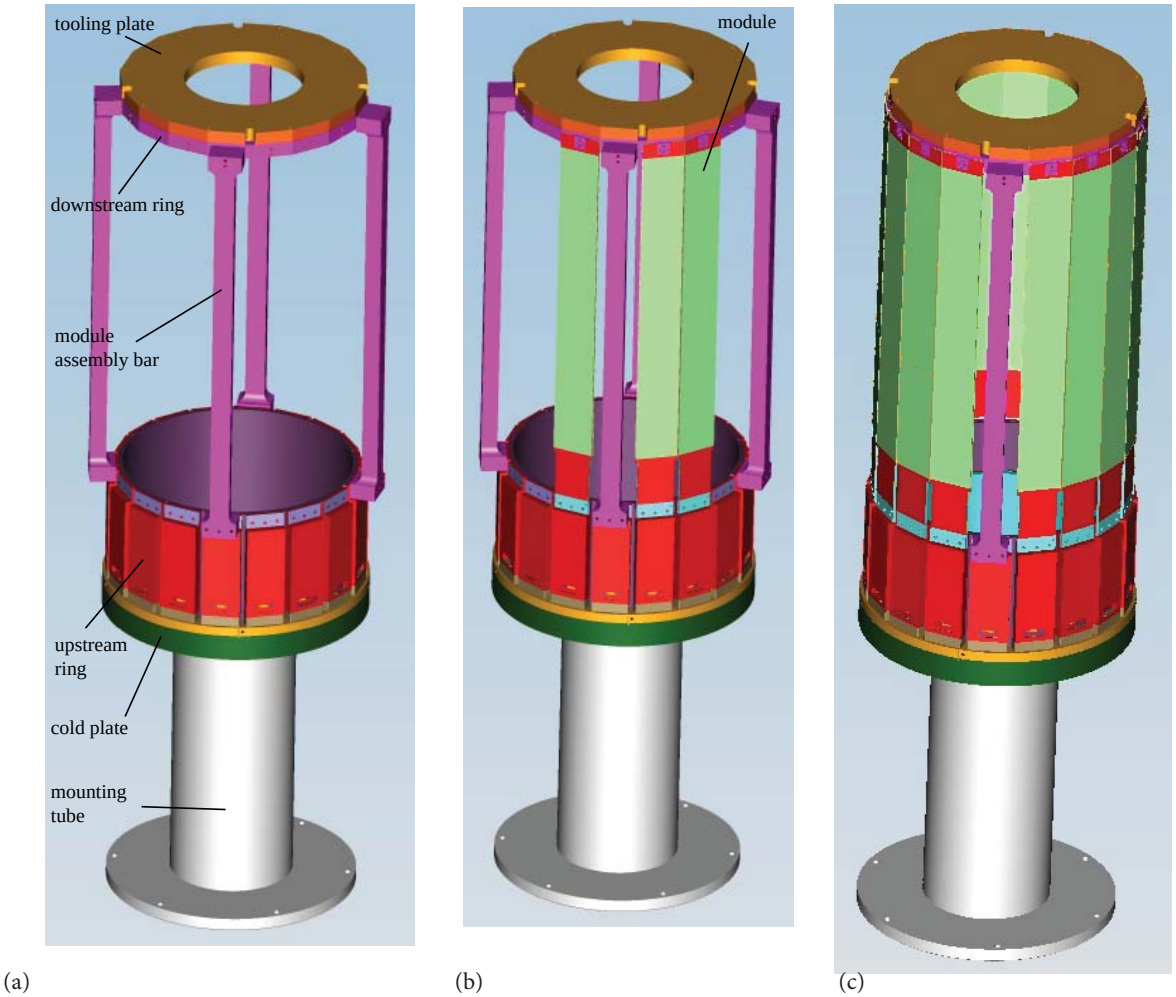


FIG. 6.2.1. (a) Cold plate, upstream ring and downstream ring in position prior to assembly of modules, (b) during assembly of modules, and (c) just prior to removal of final assembly bar.

Once the downstream ring and the tooling plate are in position, the CMM will be used to establish a coordinate system and a central axis for the detector, based on fiducials machined on the flange of the mounting tube and the tooling plate. The modules will be mounted between the upstream and downstream rings as shown in Fig. 6.2.1(b). As the modules are mounted sector by sector around the polygonal ring, each of the four assembly bars will be replaced by a module, in sequence. Figure 6.2.1(c) shows R3 prior to the replacement of an assembly bar. During assembly of each module, the position of the fiducials machined onto the module will be measured relative to the established coordinate axes. The tangential, axial, and radial inaccuracies in the position of the modules will be recorded. Upon completion of each region, the downstream tooling plate will be removed and locations of fiducials on the downstream

ring will be measured with respect to the coordinate axes. Upon completion of the assembly of all modules, the detector will be moved to a horizontal position and the relative positions between the downstream rings of all regions will be measured and recorded.

7 Power Systems

Each side of a module has a high voltage channel, ~80 V (40 μA), and two low voltage channels, 2.5 V (0.3 A). In all, 132 and 264 channels of high and low voltages are needed, Table IX.

	R1	R2	R3	R4	All
# of low voltage channels	40	56	72	96	264
# of high voltage channels	20	28	36	48	132

TABLE IX. Breakdown of high and low voltage channels per region.

To power the FSSR2 ASICs and to bias the modules, W-Ie-Ne-R's Universal Multichannel Low and High Voltage System (MPOD) crates, Fig. 7.1, are used. The crates are 19 inches tall, rack-mountable, and capable of housing 10 low voltage W-Ie-Ne-R cards or 10 high voltage ISEG cards, or a combination of the two. Output voltage channels of the cards are floating. All power supply channels have programmable voltages, ramp rates, and limits. Hardware limits on voltage and current can be set on each card. Local control of the crate and cards is available on the LCD front panel; remote control is facilitated by a 10/100 Ethernet connection.

FIG. 7.1. MPOD crate.

For low voltage, the Wiener eight-channel low voltage cards will be used. These cards have a peak-to-peak voltage (Vpp) ripple of 10 mV and are capable of providing up to 8 V @ 5 A per channel via a 2 x 37-pin, sub-D connector. Each output channel has a 12-bit voltage setting and measurement resolution, as well as a 12-bit current monitoring resolution.

To bias the modules, the ISEG high precision, 16-channel high voltage cards will be used. These cards have a Vpp ripple of 5 mV and are capable of providing up to 500 V at 10 mA via a Redel multi-pin connector. Each output channel has a 21-bit voltage setting and measurement resolution, as well as a 21-bit current monitoring resolution. Clean power, provided by shielded isolation transformers, is used for the high and low voltage power supplies.

8 Electronics

8.1 Readout ASIC, FSSR2

The FSSR2 ASIC, fabricated by Taiwan Semiconductor Manufacturing Company in the 0.25-µm CMOS process, has a data-driven architecture. The block diagram of the FSSR2 ASIC is shown in Fig. 8.1.1. Internally, the FSSR2 ASIC has four sections: core, data output interface, programming interface, and programmable registers.

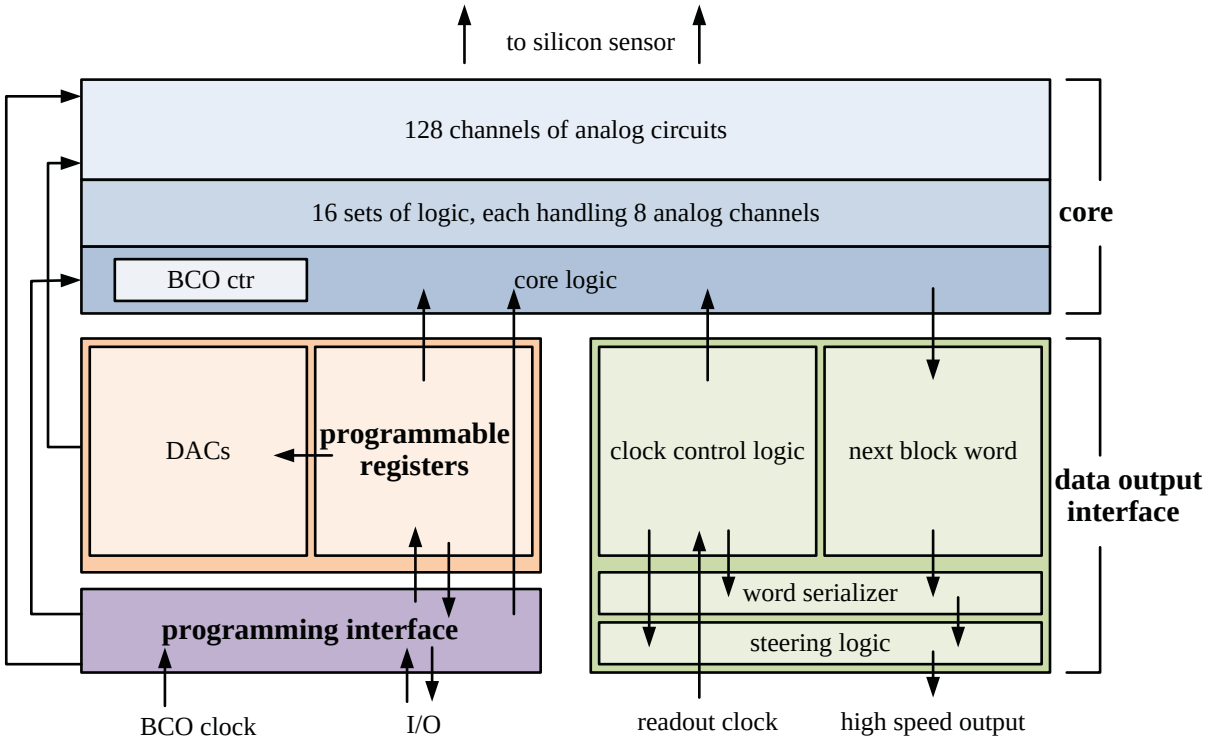


FIG. 8.1.1. FSSR2 block diagram.

The 128 analog channels of the core are structured as an 8 x 16 matrix. Each column has eight analog readout strip inputs. Each matrix element corresponds to a readout strip; the eight readout strips mapped into a column are contiguous. The period T of the clock called the beam crossing oscillator (BCO), which is selectable from the interval [66 ns, 396 ns], sets the data acquisition time. If a hit is detected in one of the channels, the core logic transmits pulse amplitude, channel number, and time stamp information to the data output interface.

The data output interface accepts data transmitted by the core, serializes it, and transmits it to the data acquisition system. To send the 24-bit readout words over the serial data lines, one, two, four, or six data lines can be used. Both edges of the 70-MHz readout clock are used to clock data, resulting in a maximum output data rate of 840 Mb/s over the six low voltage differential signal lines (LVDS). The readout clock is independent of the acquisition clock.

The programming interface handles the slow controls communication link between the FSSR2 ASIC and the data acquisition system. The internal programmable registers, accessed via the programming interface, are used to set up the FSSR2 ASIC and to provide control functions.

Each of the 128 input channels of the FSSR2 ASIC has a preamplifier, a shaper that can adjust the shaping time (50–125 ns), a baseline restorer (BLR), and a 3-bit ADC. An inject-capacitor is provided for testing and calibration. If needed, any one of the 128 channels can be turned off.

Each column of the core is handled by an end-of-column (EOC) logic set, Fig. 8.1.2. The EOC logic communicates with the core logic that handles the output. The core receives the BCO and the readout clock signal from an external source.

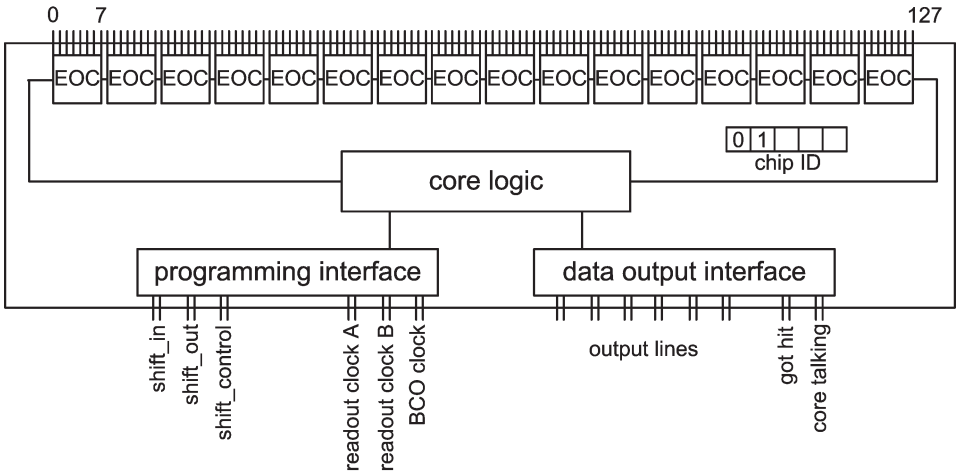


FIG. 8.1.2. FSSR2 logic.

If a hit is detected in one of the channels, the channel sends a signal to its EOC logic and then the channel goes into the idle state. The EOC logic then indicates to the core logic that it has a hit and stores the current BCO number broadcast by the core. Once the core switches to the output mode, the column outputs the hit data, the EOC logic appends a time stamp to it, and the core forms and transmits a data word.

Hits that occur during a BCO cycle on the different matrix elements are processed simultaneously. However, once the EOC logic is notified by a column that it has a hit, the wait period of that column's elements to acquire the next hit is three BCO clock cycles. The FSSR2 ASIC continuously transmits 24 bits of either status or data words. Figure 8.1.3 shows these EOC operations.

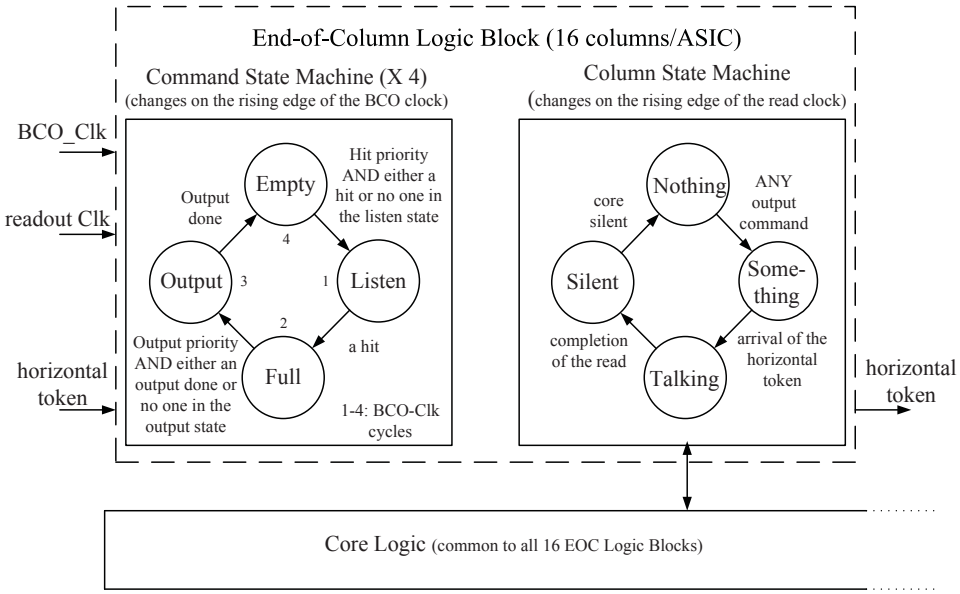


FIG. 8.1.3. End-of-column logic block.

The FSSR2 ASIC has 24 programmable registers, Table X. There are three 1-bit, sixteen 8-bit, one 2-bit, and two 128-bit registers. Two registers do not have data bit; these are used to reset the FSSR2 ASIC either via a smart core reset, (resets hits and/or BCO number, depending on the instruction), or a smart programming reset, which sets the currents and voltages to default values.

Register #	Name	Bits	Default
1	internal pulser value	8	0
2	internal pulser control	1	0
3	integrator Vbn	8	139
4	shaper Vbp2	8	121
5	shaper Vbp1	8	116
6	baseline restorer Vpb1	8	80
7	discriminator Vtn	8	0
8	discriminator Vtp[0]	8	255
9	discriminator Vtp[1]	8	255
10	discriminator Vtp[2]	8	255
11	discriminator Vtp[3]	8	255
12	discriminator Vtp[4]	8	255
13	discriminator Vtp[5]	8	255
14	discriminator Vtp[6]	8	255
15	discriminator Vtp[7]	8	255
16	active lines	2	0
17	kill mask	128	0
18	inject mask	128	0
19	send data	1	0
20	reject hits	1	1
24	smart programming reset	N/A	N/A
27	digital control register	8	0
28	smart core reset	N/A	N/A
30	acquire BCO number	8	0

TABLE X. Default register values.

The 1-bit registers are used for turning the internal pulser on or off, rejecting or accepting hits, and for sending or not sending data. The 8-bit registers are used to store: pulser magnitude, integrator reference current, shaper reference current (two), BLR reference current, and eight voltage thresholds for a 3-bit ADC. The 8-bit digital control register contains a set of values packed together: shaping time, feedback capacitor value, BLR enable/disable, and modulo 159/255 (BCO cycles). The 128-bit registers contain two masks: kill and inject. The kill mask is used to disable specific channels. The inject mask connects specified channels to the built-in pulser. The 2-bit register stores the number of output lines to be used (one, two, four, or six). Data or status words are split according to the number of output lines selected. The FSSR2 ASIC uses serial mode for both input and output. Shift_in and shift_control lines are used for programming the FSSR2 ASIC, Fig. 8.1.4.

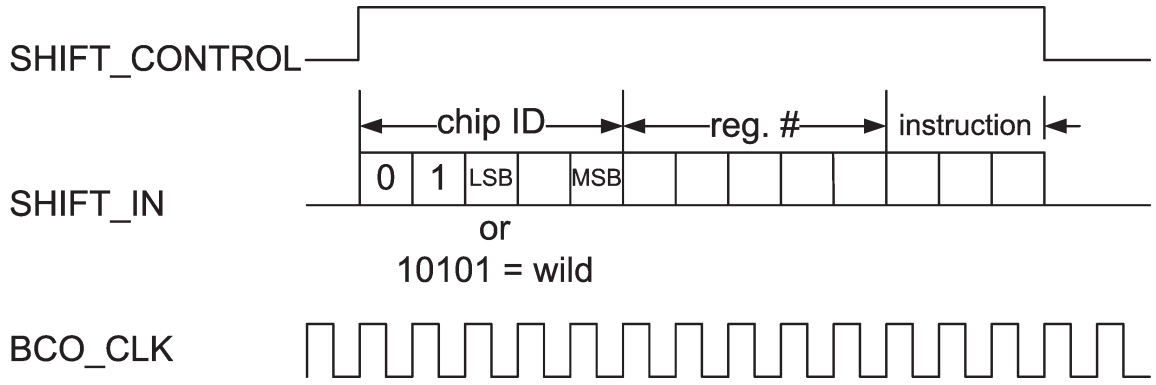


FIG. 8.1.4. Command sequence.

When shift_control goes high, the FSSR2 ASIC is set to receive command sequences on the shift_in line. Bits from shift_in are latched to the programming interface on the falling edge of the BCO clock.

A command consists of thirteen bits: five bits for the ID of the FSSR2 ASIC and channel, five bits for register number, and three bits for instruction. The FSSR2 ASIC has instructions to set (all bits to 1), reset (all bits to 0), restore default values, write, and read. The write instruction must be followed by 1, 2, 8 or 128 bits of data.

Shift_control must go low after the last instruction or data bit, and a delay of one BCO clock cycle is required before another instruction can be processed. Data structure of all of the registers, except for kill and inject, is most significant bit first, least significant bit last. The kill and inject registers cannot be set or reset; they only accept the write command.

After a read instruction, the register value is latched to the shift_out line on the rising edge of the BCO clock after a one-cycle delay. For all registers, except kill and inject, the bit order is reversed—data is shifted out least significant bit first, most significant bit last. Kill and inject registers are reset to default values after readout. Shift_control must stay high while the register is being read out, Fig. 8.1.5.

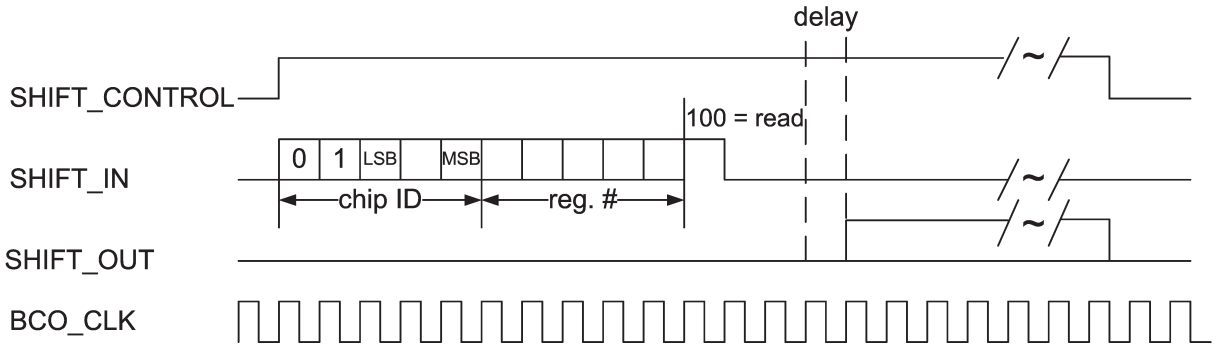


FIG. 8.1.5. Readout sequence.

If the FSSR2 ASIC is idle, it continuously sends out 24-bit status words. The bit sequence is described below and shown in Fig. 8.1.6.

B0 – word mark (1)
B1-13 – unused (0)
B14-16 – chip ID
B17 – pulser status
B18 – modulo
B19 – acquiring BCO
B20-21 – number of output lines
B22 – reject hits setting
B23 – send data setting

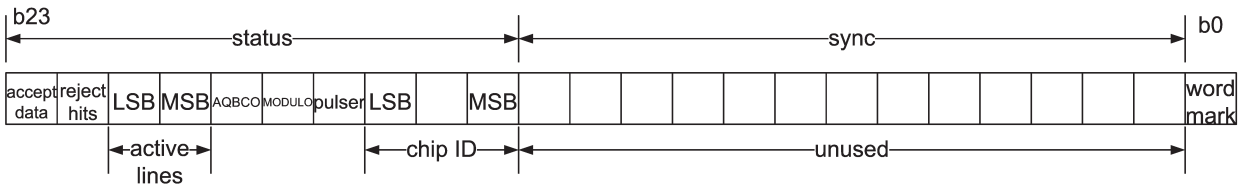


FIG. 8.1.6. FSSR2 ASIC status word.

If a hit is detected and the FSSR2 ASIC is set to send data, it transmits a 24-bit data word. The bit sequence is described below and shown in Fig. 8.1.7.

B0 – word mark
B1-3 – pulse height (from the 3-bit ADC)
B4-11 – BCO number
B12-16 – column number
B17-20 – row number
B21-23 – unused

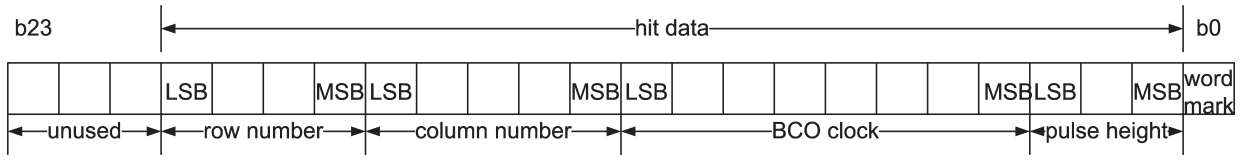


FIG. 8.1.7. FSSR2 data word.

Row and column numbers are set so that a sequence of thirteen zeroes can never occur in a data word. After powering the FSSR2 ASIC, it must be reset for it to work correctly. A master reset (hardware) resets all programmable values and hits on the FSSR2 ASIC. Once the master reset has been executed, the FSSR2 ASIC defaults to a silent state—does not accept hits or sends data; further, the discriminator thresholds are at the highest level.

A simple instruction sequence which makes the FSSR2 ASIC send data words is:

1. master reset
2. adjust discriminator thresholds
3. reset reject hits
4. smart core reset
5. set send data

For setting kill/inject masks, the instruction sequence is:

1. master reset
2. set reject hits
3. set kill/inject patterns
4. reset reject hits
5. smart core reset
6. set send data

Readout of the input matrix to the core of the FSSR2 ASIC is by columns: $M_{1,1}$ ... $M_{8,1}$; $M_{1,2}$, ..., $M_{8,2}$; $M_{1,16}$, ..., $M_{8,16}$.

Calculations and simulations show that at a hit rate of 2 MHz on an FSSR2 ASIC, due to double hits on a strip during a BCO of 132 ns or due to the fact that the EOC was busy, or both, ~3% of the hits are lost, Fig. 8.1.8.

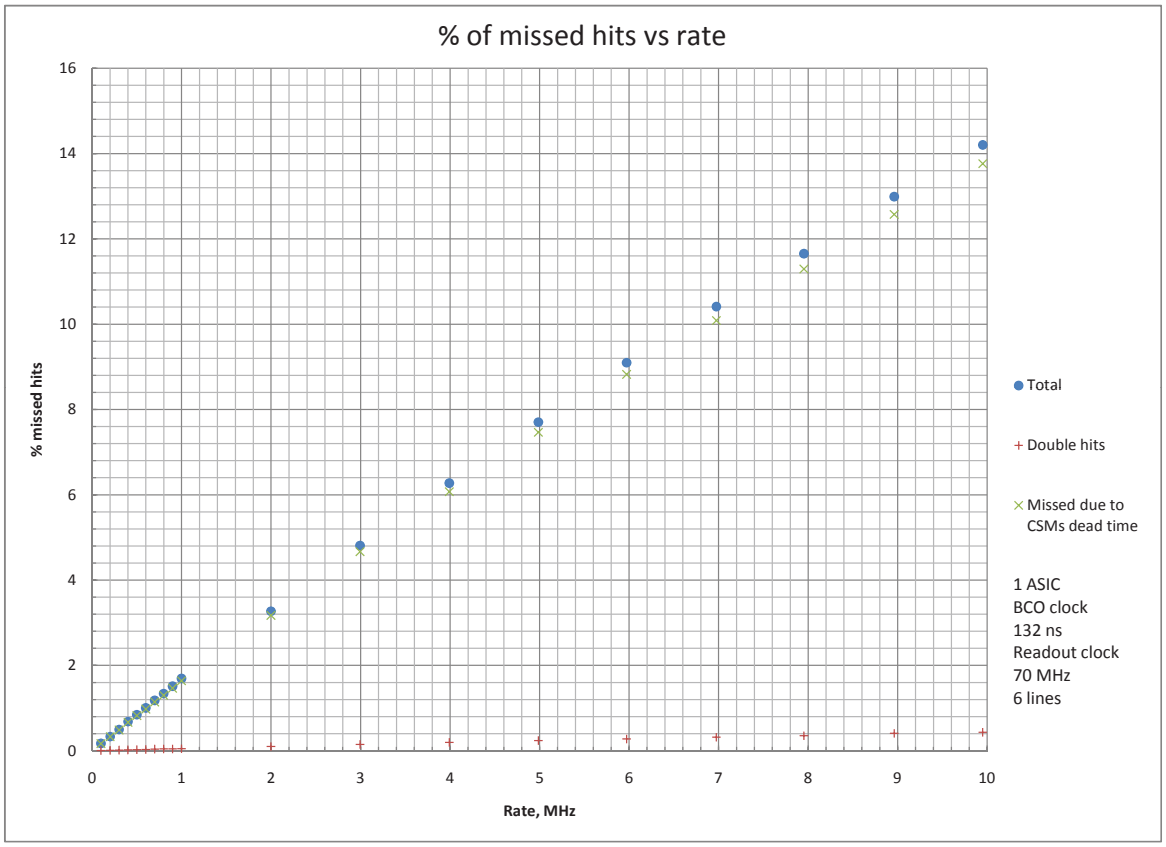


FIG. 8.1.8. Percentage of hits lost as a function of the FSSR2 ASIC hit rate.

Simulations show that on the LH_2 target, at a threshold of ~40 KeV, the total hit rate is ≤ 15 MHz, ~0.75 MHz/FSSR2 ASIC in R1; at this hit rate, < 1% of the hits are lost. The average arrival time of the CLAS Online Data Acquisition interrupt is expected to be once every 1000 μs.

8.2 HFCB

Located at the upstream end of the module, the HFCB reads out both sides of a module, Fig. 5.2. The HFCB is instrumented with two FSSR2 ASICs for the top and two for the bottom side of the module. Each FSSR2 ASIC reads out 128 channels of analog signals, digitizes them, and transmits them to a VXS-Silicon-Control-Module (VSCM) card in the VXS crate. Additionally, the HFCB provides 2.5 VDC of low voltage filtered power for the FSSR2 ASICs, as well as the high voltage for the module.

The HFCB, a rigid/flex circuit board, has five areas: two hybrid areas, the Level 1 connection (L1C), and two polyimide sections, the straightaway section and the wing cable between the hybrids, Fig. 8.2.1. The hybrid areas and L1C are rigid and 1.53 mm thick; all components are located in these areas. These rigid areas have twelve layers—two sets of three layers of FR4 that sandwiches six layers of polyimide, Fig 8.2.2. In the rigid areas, the top and bottom layers are made from 1 oz copper, the inner layers from 0.5 oz copper. The six layers of polyimide (0.49 mm thick) compose the core of the circuit and exist in all five areas. The wing cable and the straightaway section are flexible because they do not have any FR4 layers. The dimensions of the HFCB are 83.5 mm x 441 mm x 1.53 mm.

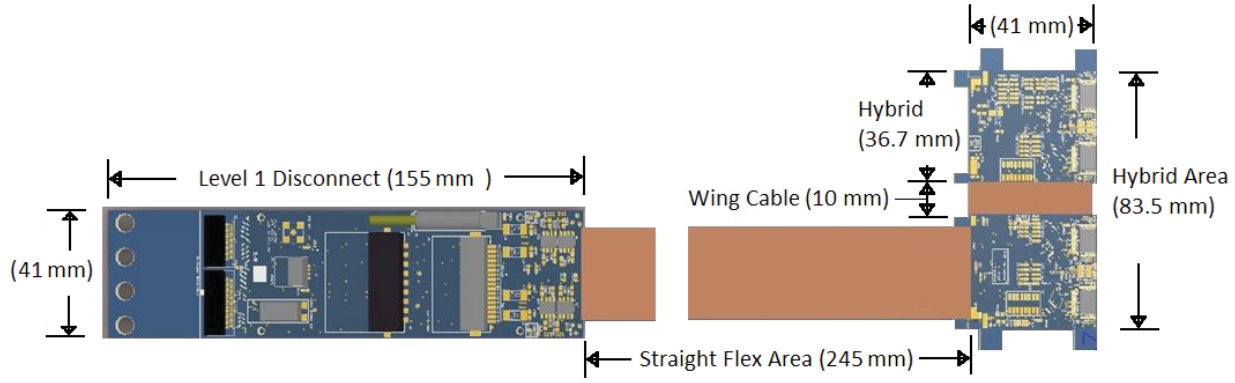


FIG. 8.2.1. Five areas of the HFCB.

0.0012	Layer 1 copper plating			
0.00035	Layer 1 copper foil - 9 micron			
0.003	One 1080 PP			
0.0006	Layer 2 copper			
0.003	Core			
0.0006	Layer 3 copper			
0.003	One 1080 PP w/ Pre-Routed Slot			
0.003	Filler w/ Pre-Routed Slot			
0.006	Two Pre-Routed 1080 PPs		DuPont LF7001 Coverlay	0.001
0.0006	Layer 4 copper			0.0006
0.004	Core AP8545			0.004
0.0006	Layer 5 copper			0.0006
0.005	One 1080 & one 106 Prepreg	.008"	DuPont LF0131 Adhesive	0.0045
0.0006	Layer 6 copper			0.0006
0.002	**Core AP8525**			0.002
0.0006	Layer 7 copper			0.0006
0.002	**One 106 Prepreg**		**DuPont LF7021 Adhesive**	**0.0012**
0.0006	Layer 8 copper	drill		0.0006
0.002	**Core AP8525**			0.002
0.0006	Layer 9 copper			0.0006
0.006	Two Pre-Routed 1080 PPs		DuPont LF7001 Coverlay	0.001
0.003	Filler w/ Pre-Routed Slot			**0.0193**
0.003	One 1080 PP w/ Pre-Routed Slot			0.49022
0.0006	Layer 10 copper			
0.003	Core			
0.0006	Layer 11 copper			
0.003	One 1080 PP			
0.00035	Layer 12 copper foil			
0.0012	Layer 12 copper plating			
0.0601				
1.52654				

FIG. 8.2.2. Material stack-up of HFCB. The 12 layers on the left are the rigid areas and the layers on the right are the flex area. The numbers indicate thickness in inches, except the numbers at the bottom of the columns are totals in mm.

The hybrid areas are wire bonded to the pitch adapter; the detector bias, bias return, and the ground for the carbon fiber of the backing structure are soldered to the hybrid. The straightaway section and the L1C will be routed through cold plate slots, which have a radial opening Δr of 10 mm. Hence, the profile of the L1C, including components, has to be <9 mm. The L1C is mounted to the support tube on its own support structure, which keeps each L1C in line with its module.

Each hybrid area contains passive electronics, a temperature sensor, a high voltage filter, and a diagnostics header. The hybrid areas are 36.7 mm by 41.4 mm, excluding the two flexible alignment tabs (7 mm x 7 mm), which will be removed after installation of the hybrid on the module.

Each hybrid area has flexible tabs that will be used to make soldered electrical connections to the bus cable, to provide the ground connection for the carbon fiber, and to provide the module's bias voltage. The top corners of each hybrid have wire bond pad areas for connecting the bias return to the bond pad on the pitch adapter. Each bond pad is large enough to have ten 25-μm-diameter aluminum wire bonds. The bottom hybrid contains the split termination

resistors and capacitors for the front-end and back-end clocks, reset, and for the termination resistors for the shift controls and external pulser.

The hybrid areas are connected together by the 10-mm long wing cable, Fig. 8.2.3, which transmits data to the L1C from the bottom hybrid, and provides bidirectional controls, clocks, signals,and voltages. The length of the wing cable is optimized for folding around the module support structure, without interfering with the adjacent module.

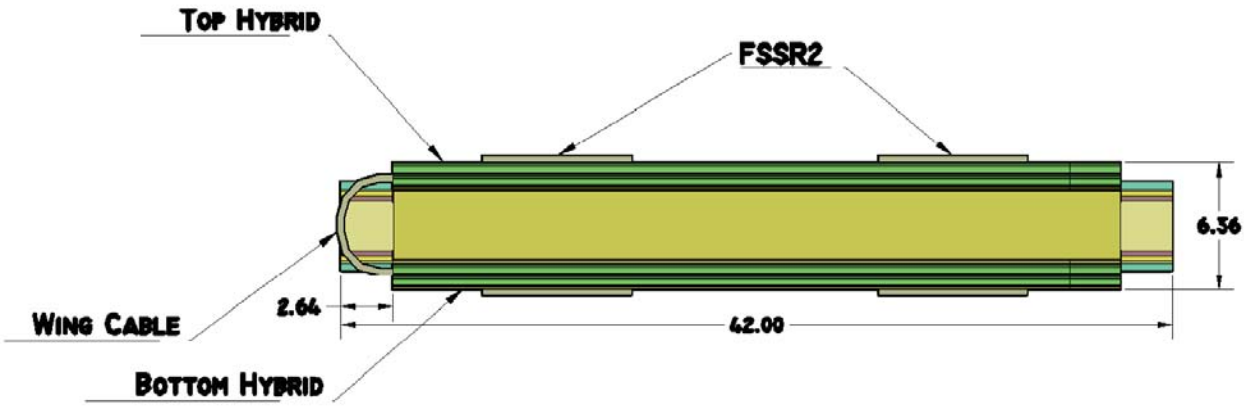


FIG. 8.2.3. Cross-section of HFCB at hybrid end.

The L1C, 155 mm long and 41 mm wide, has four mounting holes and a 30-mm extension, which has non-plated holes for tie wraps, beyond the last connectors to provider strain relief of the six cables that connect to each L1C.

For the 2.5 VDC lines needed to power the FSSR2 ASICs, the L1C has an analog and a digital regulator LP2989AIM-2.5-ND for each side of the module, . If the regulators cause problems, they can be bypassed and an inductor capacitor filter circuit could be used instead.

Each L1C contains one micro barrier block, which connects the cable shields to the overall detector shield. In addition to this, the L1C has seven connectors listed in Table XI.

Connector	Description	Comments
Amp Mini CT 17	17-pin low voltage	handles 2 digital voltages, 2 analog voltages, 4 sense pairs, and a cable shield connection
Molex Micro-Fit	9-pin high voltage	2 channels to provide 50–200 VDC; cable shield connection
Sabritec NDL-Q	triaxial	external pulser with cable shield connection on the outer braid
H&S MMCX	coaxial	voltage reference with cable shield connection on the outer braid
Molex CLIK-Mate 4	4-pin	for slow controls, has 2 temperature sensor outputs and cable shield connection
Nanonics dual lobe 37	37-pin	connects to U3 and U4 data output; cable shield connection for the data cable
Nanonics dual lobe 51	51-pin	connects to U1 and U2 data output and the clock and status register bus

TABLE XI. Seven connectors used on the L1C.

The L1C is connected to the top hybrid via the 245-mm long straightaway section. All signals and voltage are carried from their connectors on the L1C to the respective planes and components on the hybrid areas via the straight away section.

The top layer of the hybrid areas has a copper pour, which is connected to the low voltage return and is finished with Electroless Nickel Gold (ENIG), which facilitates electrical contact for all methods of connection—bonding, soldering, and epoxying. The FSSR2 ASICs' substrates are fixed to pads on the hybrids with conductive silver epoxy,

Tra-duct 2902. These pads are the reference for the analog return of the FSSR2 ASICs. Bypass capacitors for the analog returns connect between these reference pads and the analog voltage pads, Fig. 8.2.4. All FSSR2 ASIC voltages are decoupled from the low voltage return with a 0.1 uF or a 0.022 uF capacitor. Due to size limitations and the number of capacitors (19 per chip), 0201 package capacitors are used.

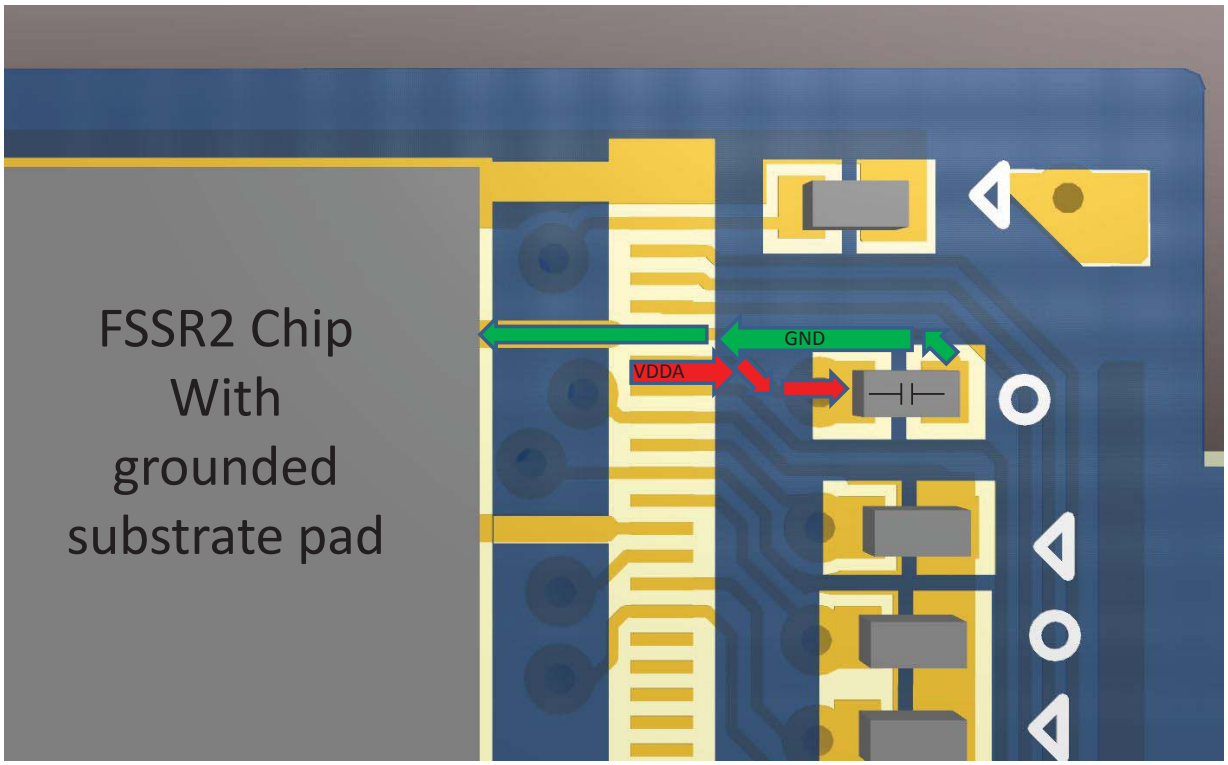


FIG. 8.2.4. Analog voltage bypass capacitor circuit.

There are two internal trace routing layers—INT0 and INT1. INT0 exists only in the FR4 and provides connections for traces that need to change layers. INT1, which is a polyimide layer and is the most densely routed layer, contains all signal and clock traces from the L1C to the hybrids. Minimum trace clearance on the INT1 layer is 3 mils and the minimum trace width is 3 mils. All clock traces are separated from differential signals by guard traces, which are stitched to the ground planes with *vias*. Where possible, all sets of differential pairs are separated from each other by 7 mils; this narrows to 3 mils near the FSSR2 ASICs due to the layout of the bond pads.

The HFCB has four ground plane layers. GND0, in the FR4, provides reference for the top layer and INT0. The remaining three ground layers are in the polyimide. GND1 and GND2 sandwich INT1; GND3 covers the polyimide and protects the analog low/high voltage layer. There is only one ground net for low voltage; all ground planes are tied together by ~500 *vias*.

There are two voltage layers in the polyimide, one split plane for digital voltage and one split plane for analog voltage. The analog voltage layer accommodates the high voltage.

Two FR4 layers have dedicated planes for high voltage returns. The filter for each side of the module is located on the associated hybrid area. At the input location, there are two series resistors with a capacitor between them, which connects to the ground plane of the VDDA/high voltage layer. At the output location, the capacitors (56 µf and 1 MF) are located between the FSSR2 ASICs. The high voltage return plane is connected to the low voltage return at the FSSR2 ASIC substrate.

The layers called *bottom* are in the FR4 areas only and are void of features and traces, with the exception of copper pours in each area that are connected to low voltage return. In the hybrid areas, the bottom layer is designed to conduct heat generated by the FSSR2 ASICS to a copper insert built into the module support structure. The heat generated by the FSSR2 ASICs is conducted to the bottom layer by a 6 x 4 matrix of *vias* that are 8 mils in diameter.

Data output and clock signal lines stipulate trace routing requirements. There are a total of 43 differential pairs:

four sets of nine data output pairs (one for each FSSR2 ASIC) and seven sets of control signal pairs that go to the FSSR2 ASICs before being terminated on the bottom hybrid. The output pairs for an FSSR2 ASIC consist of six pairs for address, a pair each for GotHit, Coretalking, and the output clock. The seven control signal pairs are: the front-end clock (BCO), the back-end clock, two pairs of clock signals, which are 90° out of phase from each other and make up MCLKA and MCLKB lines, three pairs of shift register controls (Shiftin, Shiftout, and Shiftcntrl), and a pair for reset (OR).

With regards to the layout of the pairs, one critical parameter is pair length difference. The layout of the pairs has been done to ensure that the differential pair length difference is ≤40 mils The front-end/back-end clock length difference is ≤1mil. The front-end/back-end clock comparison (longest difference in time) is shown in Tables XII and XIII.

Clocks	Δt [ps]
BCO	6.47
MCLKA	6.14
MCLKB	6.64

TABLE XII. Time difference between the lines of a differential pair of a clock.

FSSR2 ASIC	Δt [ps]
U1	27.7
U2	15.9
U3	40.5
U4	12.9

TABLE XIII. Time difference between out-clock and the longest output signal line of an FSSR2 ASIC.

9 Data Acquisition

The four FSSR2 ASICs on the HFCB communicate with the VXS architecture-based segment collector module (VSCM), which configures the FSSR2 ASIC registers, provides analog calibration pulses to the FSSR2 ASICs, sets/monitors proper control signals (clock, reset, status), and acquires serialized event data from the FSSR2 ASICs. Each VSCM can interface with two HFCBs. Up to 16 VSCM cards can reside in a VXS crate. When multiple VSCM cards are used, additional cards, the Trigger Interface (TI) and Signal Distribution (SD), Fig. 9.1, are required to ensure event and timing synchronization. The VSCM supports a stand-alone mode, useful when only one or two HFCBs are used.

Each FSSR2 ASICs has six LVDS pairs with a source synchronous clock to transmit event data. The VSCM supports receiving data from all six LVDS pairs of each FSSR2 ASIC running at 70 MHz double data rate (DDR) (840 Mb/s from each FSSR2). Xilinx Spartan 6 FPGAs are used to buffer and deserialize data from two FSSR2 ASICs each. Four of these FPGAs are used to support eight FSSR2 ASICs' simultaneous data streams coming from two HCFB interfaces; the FPGAs in turn send their information to the master FPGA where the event builder resides.

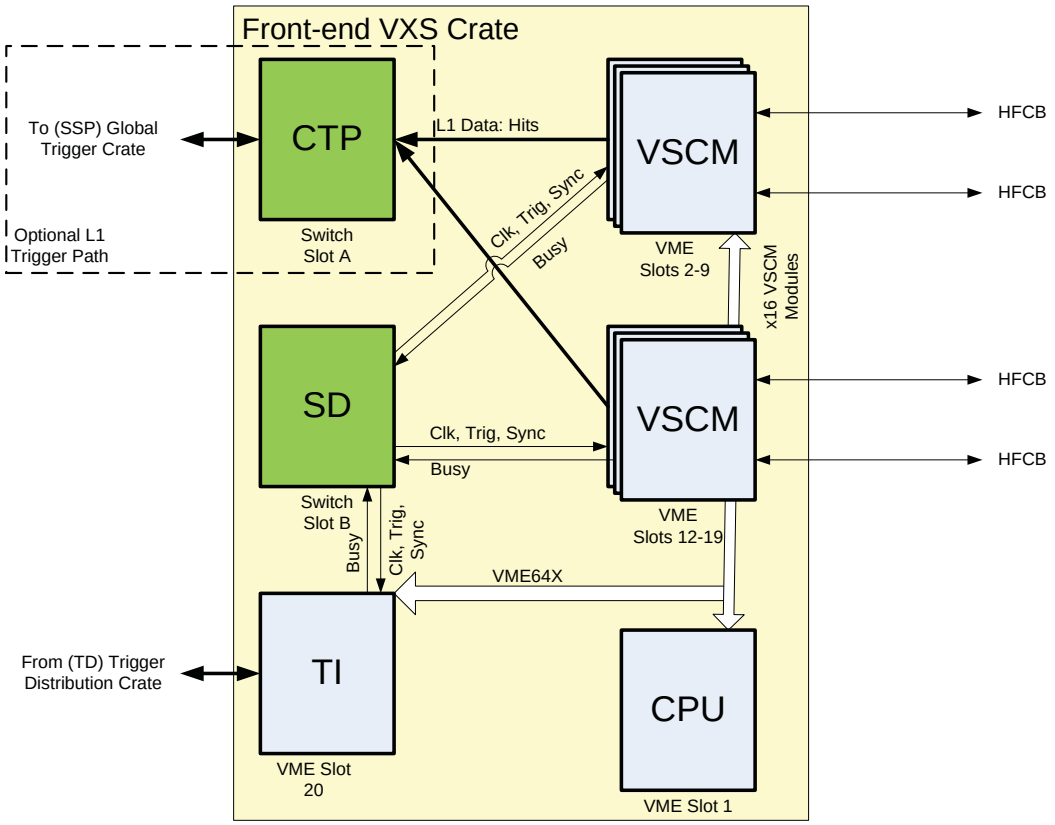


FIG. 9.1. Schematic of the VSCM.

The FSSR2 ASICs' architecture is such that it sends out 24-bit data words if a channel has a hit or a 24-bit status word if the channel does not have a hit (idle state) within a BCO clock cycle. The FSSR2 ASICs transmit these data over six lines.

First, the data is de-serialized. The 24-bit data words are appended with 8 bits to make the time range longer, and the 32-bit words are correlated to the trigger, which is generated by other detectors. The status words are suppressed to minimize the data size of an event. However, the status words are monitored to diagnose the performance of individual FSSR2 ASICs.

The event builder of the VSCM uses the BCO clock timestamp from the data word of each FSSR2 ASIC and matches it to the timestamp of the global system clock, given by the CLAS trigger. The FSSR2 ASIC data is tagged with a global trigger timestamp (48 bits, 8 ns resolution). Since the BCO clock is derived from the global system clock, triggers received by the VSCM enables the event builder to extract hits with specific BCO timestamps that fall in a programmable time window within which the event could have occurred. When a trigger is received, the data words from the FSSR2 ASICs are copied to an event buffer and pushed into an event FIFO. These events can be read out in order with other modules in the system while event-level synchronization across all modules in the system is maintained.

The VME interface provides for event readout, access to the configuration registers on the VSCM, bridges access to the registers of the FSSR2 ASICs, and provides an interface to the CPU. The A32 address space, ~2 MB in size, is dedicated to the event builder FIFO, which can be read using single-cycle and block transfer VME protocols. Block transfer protocols will be used for event readout; the 2eSST protocol planned for use is to maximize performance. The 2eSST protocols provide ~200 MB/s sustained transfer rate and supports the proprietary Jefferson Lab token-passing scheme that allows a single DMA operation on the CPU to transfer data from all VSCM modules sequentially, eliminating overhead (compared to individual board transfers).

The event builder buffers data received from all FSSR2 ASICs for a programmable latency time up to 16 µs. The VSCM is set up to extract event data within a programmable lookback window of ~16 µs relative to the received trigger. The trigger latency is expected to be ~8 µs. Since the FSSR2 ASIC data is tagged with the equivalent global

trigger timestamp, the event builder takes FSSR2 ASIC data words with global trigger timestamps that fall within the programmed lookback window. These data words are copied into the event FIFO and marked with the event number, trigger time, and other data acquisition-related bits, to add redundancy and to ensure reliable event-level synchronization with error checking. FSSR2 ASIC data words can be reported multiple times if triggers happen to have overlapping lookback time windows that include the same FSSR2 ASIC data word.

To form an event FIFO, the event buffer uses a 2 MB external SRAM— ~500,000 thirty-two-bit words. This buffer is large enough to hold events in which all 1024 channels of a VSCM card have registered a hit (100% occupancy), allowing the event builder to create readout blocks containing many events, which significantly improves readout efficiency. There can be anywhere from one event per readout block to 128 events per readout block, which is to be selected and programmed by the user before data acquisition is started. The number of events in a readout block must be an agreed upon number across the whole data acquisition.

The event structure for the least efficient case, one event per block, is:

1 word - Block Header

1 word - Event Header

2 word - Event Timestamp

N words - N FSSR2 ASIC hits

1 word - Filler word (put in to force even number of data words to satisfy VME 64bit/128bit transfers if needed)

1 word Block Trailer

Based on 1024 channels per VSCM, Table XIV shows the maximum events as a function of occupancy of the VSCM.

Occupancy [%]	Hits	Words per event	Events
5	52	58	8620
10	103	108	4629
15	154	160	3125

TABLE XIV. Maximum events as a function of occupancy.

In event blocking size of 1, there needs to be space for one event so no data is lost. There could be 488 hits per channel for all channels in a single event and there is no loss of data, as long as the board is read out. If the readout is done in a more efficient readout mode, such as 128 events per block, the limit of maximum events as a function of occupancy becomes roughly 1/128th that of the single event per block case, 3 hits per channel on all channels in each of the 128 events in the block.

The ethernet's transfer rate of ~100 MB/s per crate allows sustained 2500 hits per crate at a 10 kHz trigger rate for 11 boards per crate. If this rate becomes an issue, the VSCM firmware can be changed to pack multiple hits per word (two hits per word), which would support 5000 hits at 10 kHz. Occupancies can be higher than the sustained amount, due to the large VSCM event buffer; it is the average occupancy that could be a problem, which will show up as dead time, not corruption or loss of event data. For 2500 hits per crate at 10 kHz (2500 hits x 4 bytes/hit x 10 kHz = 100 MB/s), the 1 Gb/s ethernet limit on the CPU link to the event builder dead-time will not be a function of occupancy until the 100 MB/s limit is reached. Since all the VSCM units share the VME/ethernet bandwidth, the number of VSCMs per crate must be considered. VME will allow ~200 MB/s, ethernet will allow ~100 MB/s (ethernet could be upgraded, if needed, to 10 Gb/s ethernet so that the 200 MB/s VME becomes the bottleneck). Further, the VSCM can handle peak trigger rates at ~64 MHz (for maybe a few events in a burst). If the average occupancy is not exceeded, there will be ~0 dead-time due to the VSCM.

It is likely that CLAS12 will operate with at least a 100 ns hold-off time (trigger is accepted, and for the next 100 ns, triggers are ignored). This hold-off time will be the dominant dead-time source as long as modules are well under the sustained average occupancies that the module and/or crate readout capacity allows. Dead-time will be 10 kHz times the trigger hold-off time up to the 100 MB/s point. So, if hold-off is 100 ns, dead-time is 0.1%, due to the Trigger Supervisor. Trigger hold-off could be 1 μs or more if a slow readout module exists somewhere else in DAQ, in which case dead-time will grow accordingly.

The calibration pulser circuit provides a 2 Vpp dynamic range, up to 125 MS/S, and 14-bit resolution (for pulse height steps in sub mV increments). The bandwidth is sufficient to allow ~10 ns rise times to be delivered over 15 feet of 50-ohm coax cable terminated with 50 ohms. Two independent pulser outputs are provided to drive both HCFB

modules. The pulser signal phase can be placed in a deterministic phase relationship to the BCO clock that drives the FSSR2 ASIC. Table XV lists the specifications of the VSCM.

Specification	Value
trigger rate (peak @ 100% occupancy)	~30 MHz
trigger rate (sustained @ 24% occupancy)	10 kHz
trigger latency (max)	16 µs
event buffer size	2 MB
event buffer max events	limited by buffer size and event size
event buffer max hits	2 MB
event readout rate (max)	200 MB/s
FSSR2 BCO clock period	128 ns–400 ns
FSSR2 readout	840 Mb/s

TABLE XV. VSCM specifications.

10 Grounding and Shielding

Figure 10.1 shows a schematic of a single channel in a sensor. The signal from the aluminum readout strip is input to the FSSR2 ASIC. The returns of the floating high and low voltage supplies are isolated from the Hall B ground.

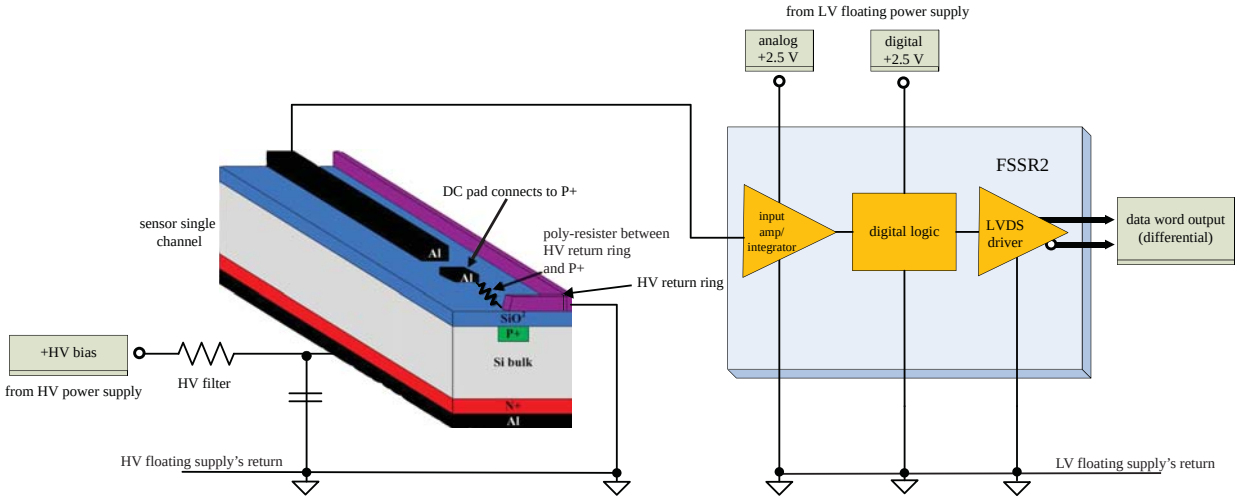


FIG. 10.1. Low and high voltage returns for a single channel of a sensor.

To maintain the reference voltage level of the carbon fiber, the copper mesh on one side of the bus cable is connected at the hybrid area of the HFCB to the return line of the low voltage.

Module connections are shown in Fig. 10.2. Modules are read out by the FSSR2 ASICs located on the hybrid area of the HFCB. Power and readout connections are made at the L1C. There is no coupling of power or return lines of different modules—each module is independent of other modules. Further, all modules will be electrically isolated from the detector support structure.

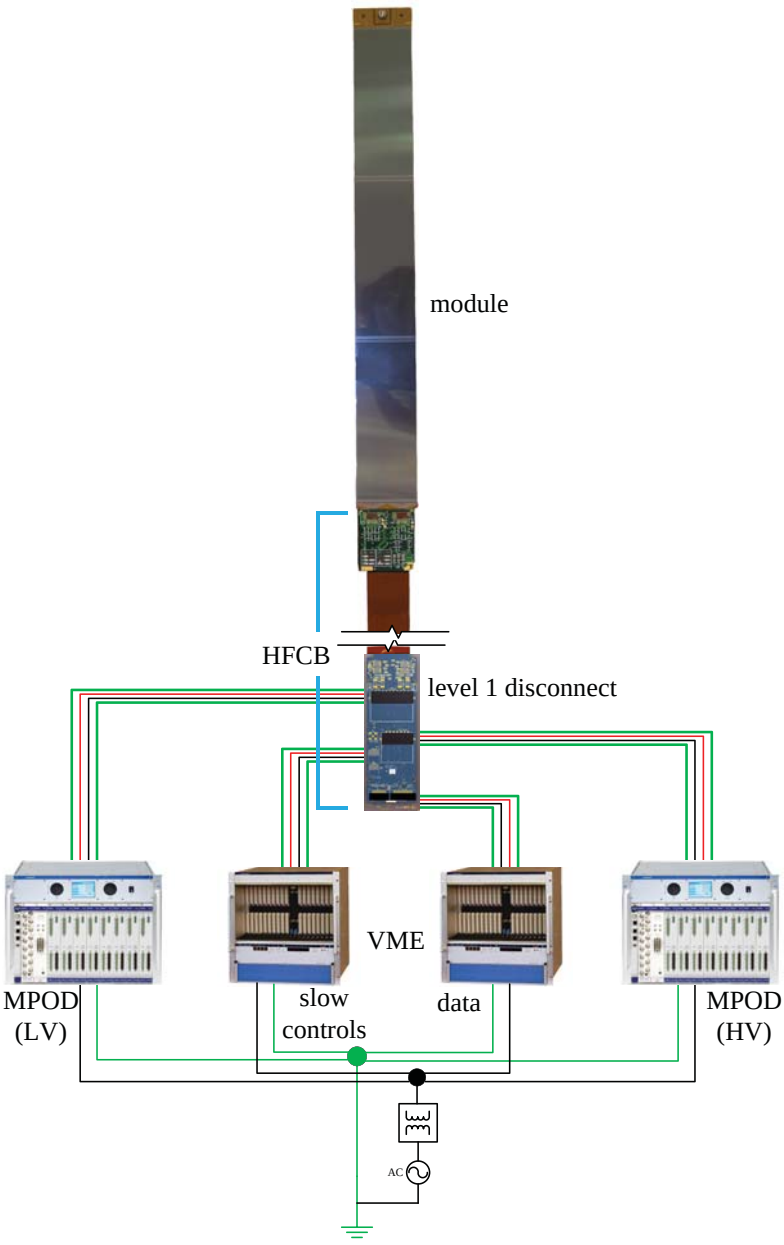


FIG. 10.2. Module connections. (Green = shield, red = hot, black = return.)

Each crate in the system will have a safety ground—achieved on purchased power supply crates by the UL-rated power plug that plugs into a common isolation transformer, Fig. 10.2. All AC cables will comply with NFPA 70E section 110 and 120 [9].

To shield against EMI, the cable shields—signal, power, slow control, and pulser—of each module will be connected together at that module's L1C, Fig. 10.2. The L1C of all the modules are located at the entrance of the Faraday cage, and from each of the L1C a cable will connect the shields to the Faraday cage, which in turn will be connected by a single cable directly to the Hall B central ground, Fig. 10.3, [10]. To minimize voltage offsets on the shield lines, the impedance of the shield connections will be as low as possible. To shield against electromagnetic interference, the SVT is located inside a Faraday cage that comprises the cold plate, a forward disk, and a cylindrical carbon shell.

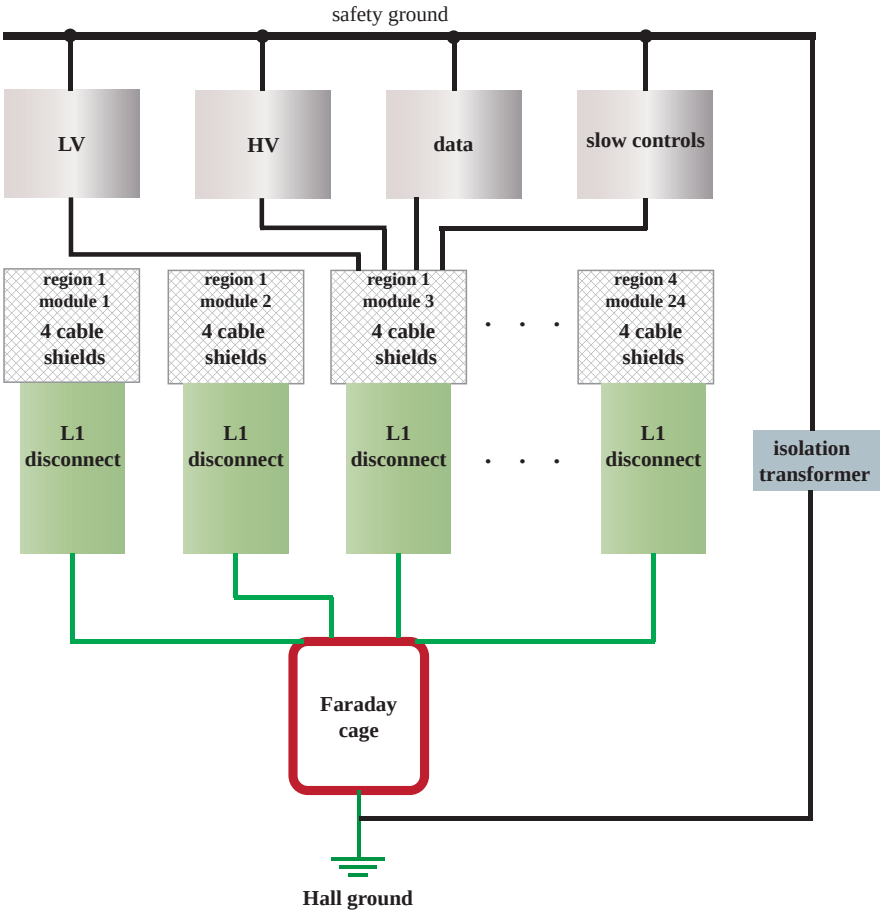


FIG. 10.3. Shielding scheme.

The grounding scheme will be tested first in the lab for validation of the design. The design allows adjustments during and after installation.

11 Slow Controls

The Slow Controls System (SCS) controls run-time parameters and monitors the status of hardware components. SCS remotely sets alarms and reaction protocols that enhance safety by providing early warnings of malfunctioning equipment and by providing the ability to check the data quality. SCS transmits parameters to the DAQ system for insertion into the data stream. In case of a malfunction, or when monitored parameters are outside set limits, SCS has the ability to trigger alarms to notify shift personnel and the capability to automatically disable modules and associated DAQ equipment or the ability to notify the expert on call so that appropriate action can be taken.

SCS controls and monitors via LabVIEW software and a custom graphical user interface (GUI) on a desktop PC. SCS is divided into two sections, *User* and *Expert*. Settings and alarm thresholds will be maintained on the PC and a redundant Computer Center server to ensure that, in case the PC fails, the failed PC can be replaced without affecting the operation of the SVT. Data will be passed to the EPICS server. The PC will have a backup power supply with surge protection. SCS software will communicate with the monitoring and control hardware (Wiener MPOD high and low voltage crates, the Wiener VXS DAQ crates, the cooling system, and the National Instruments CompactRIO modules) *via* 10/100 Ethernet.

The MPOD crate supplies high and low voltage to the silicon on the modules. Four MPOD crates, nine high voltage modules, and thirty-three low voltage modules will be monitored when the LabVIEW control GUI communicates with the MPOD crates via ethernet. Parameters listed in Table XVI and Table XVII can be controlled and monitored.

Controlled signal	Number of channels	Nominal level
MPOD crate status alarm	3	crate OK
set low voltage channel voltage	132	2.5 V
set low voltage trip	132	2.5 V
set low voltage current trip	132	0.5 A
turn channel on/off	132	-
set high voltage channel voltage	132	75 V
set high voltage trip	132	75 V
set high voltage current trip	132	40 μA
set high voltage ramp rate up	132	5 V/s
set high voltage ramp rate down	132	5 V/s
turn channel on/off	132	-

TABLE XVI. Signals controlled by the MPOD crate.

Monitored signal	Number of channels	Location
MPOD crate status	3	rack
HFCB low voltage (top)	66	MPOD crate
HFCB low voltage (bottom)	66	MPOD crate
HFCB current (top)	66	MPOD crate
HFCB current (bottom)	66	MPOD crate

TABLE XVII. Signals monitored by the MPOD crate.

Signals of the Wiener VXS crates are monitored via Ethernet as well (Table XVIII). The VXS crates receive data from the modules and place the data into the CLAS12 data stream.

Monitored signal	Number of channels
VXS DAQ crate status	2
VXS DAQ board voltage	33
VXS DAQ board current	33

TABLE XVIII. Signals monitored by the VXS crate.

The National Instruments CompactRIO modules control and read back environmental parameters listed in Table XIX and Table XX. The CompactRIO chassis is a multi-core system for embedded monitoring and control applications. Each CompactRIO chassis controller contains a Spartan-6 LX150 FPGA for custom I/O timing, control, and processing, which allows the environmental monitoring system to operate as a stand-alone system, enabling predetermined decisions to be made, and to not depend on the control and monitoring PC. The CompactRIO chassis contains eight slots allowing for various National Instrument sub-modules to be installed, giving the system the ability to monitor and control almost an endless number of signal types. A total of two National Instruments CompactRIO modules will be used to control and monitor.

Control signal	Number of channels
set detector air flow	1
set detector air flow alarm	1
set detector N_2 gas flow	1
set detector N_2 gas flow alarm	1
set external cooling flow	1
external cooling flow alarm	1
external cooling temp alarm	1
cooling plate temp alarm	4
set isolation valve	1
set isolation return valve	1
set bypass valve	1
detector photosensor alarm	4

TABLE XIX. Signals controlled by the National Instruments CompactRIO.

Monitored signal	Number of channels
module temp (top)	66
module temp (bottom)	66
detector ambient air temp	12
detector ambient humidity	12
detector air flow	12
detector N_2 gas flow	12
external cooling temp	4
external cooling flow	4
cooling plate temp	4
detector light-tight interior	4

TABLE XX. Signals monitored by the National Instruments CompactRIO.

The cooling system's chiller will communicate with the control GUI via ethernet, passing monitored and controlled signals (Table XXI).

Signal	Number of channels	Nominal level	Sensor type
chiller status alarm	1	OK	chiller internal
set cooling temp	1	15°C	chiller internal

TABLE XXI. Cooling system signals that are controlled and monitored.

12 Laser Test Stand

The laser test stand (LTS) was designed and developed at the University of New Hampshire. LTS consists of an infrared laser system and a positioning mechanism with the capability of moving the laser in x and y directions with a precision of 5 μm and a repeatability of ±0.5 μm. Additionally, the system moves the laser in the z-direction for focusing. The response of the detector is read out by the data acquisition system and analyzed to check whether all channels function as expected, ascertain whether there are variations between strips in response to the input signal, and to determine noise, gain, and attenuation as a function of strip length.

Because silicon sensors can be damaged by particulates in the air, a clean, dust-free environment is required for the detectors. A 168 square-foot softwall, ISO 7 (class 10,000) clean room from Pacific Environmental Technologies, Inc. in Corona, CA has been built from a custom-designed kit. The clean room has an internal gowning room, and then an inner chamber that contains the dry storage system, the test stand, and the data acquisition system.

Because the noise in silicon sensors increases with humidity, the dry storage system is a nitrogen-purge system designed to keep the detectors in a stable, clean, low-humidity environment. The containment for the system is a commercially-available, top-loading, 19.7-cu. ft., GE Model FCM20SUDWW chest freezer, which has been modified. The freezer has been fitted with a brass inlet and is connected to a regulated nitrogen supply with 1/4-in. O.D. Teflon PTFE tubing. Teflon tubing was chosen to limit the amount of outgassing from the tubing into the line, and ultra-high purity nitrogen is used to purge the storage chest to ensure that no moisture or gaseous pollutants are present in the storage environment. The relative humidity inside of the storage chest and in the clean room are monitored by two battery-powered temperature/humidity loggers that sample the surrounding atmosphere at defined intervals. The flow rate of the nitrogen is varied to ensure that the humidity does not go out of pre-set bounds..

LTS is housed within a light-tight laser enclosure that was built with extruded aluminum framing from Bosch-Rexroth and 1.6-mm thick 5052 aluminum sheeting panels, with a hinged door that is 3.175 mm thick. The matte black enclosure measures 1080 mm x 1080 mm x 2080 mm, and has been fitted with interlocks that turn the laser off if and when the door is opened. Poron foam strips were used as seals between the panels and the framing because of its low outgassing and long lifetime under repeated use.

The laser, a commercially-available, combination pulse generator and optical module from Berkeley Nucleonics Corporation (BNC), operates at a wavelength of 1064 nm and has a maximum power output of 1 mW. The pulse generator is a BNC Model 6040 and consists of a crystal-controlled programmable pulse/digital delay generator mainframe. This mainframe can generate both TTL and ECL output up to 100 MHz with 1 ns or less rise time and 1 ns resolution for pulse width, delay, and double pulse timing. The optical module, Model 106C, mounts inside of the pulse generator mainframe and provides a maximum of 1 mW pulsed or continuous wave laser light at a wavelength of 1064 nm. A shielded fiber optic cable is used to guide the laser light from the laser out to the detector. A lens/collimation package from Thor Labs, with a focal length of 11.17 mm, is used to focus the laser light onto the sensor, with a focused laser spot of 10 μm. The lens/collimator package is secured to the vertical rail of the precision rail system with a precision-milled bracket purchased from Thor Labs.

The rail system is used to move and position precisely the infrared laser beam over the surface of the silicon sensor. Newmark Systems in Mission Viejo, CA manufactured the rail system. Five linear systems are used to make up the positioning system that moves in the x, y, and z directions. Three of these stages have high precision movement and are capable of an accuracy of 5 μm, a resolution of 0.1 μm, a repeatability of ±0.5 μm, and a maximum travel speed of 50 mm/s. One of the two remaining stages is non-motorized and is used to distribute the weight of the other high precision horizontal and vertical stages. The last stage, the detector rail, is a motorized stage with less demanding specifications. This rail supports the detector during testing, and allows for a rough positioning under the precision x, y, and z system. When combined, the xyz stages and the detector rail have the ability to travel up to 200 mm in the x direction, 200 mm in the y direction, and 50 mm in the z direction. The precision stages are mounted on precision-milled blocks to raise them above the detector rail. The entire assembly is mounted on an optical table to minimize vibration. A photograph of the rail system is shown in Fig. 12.1.

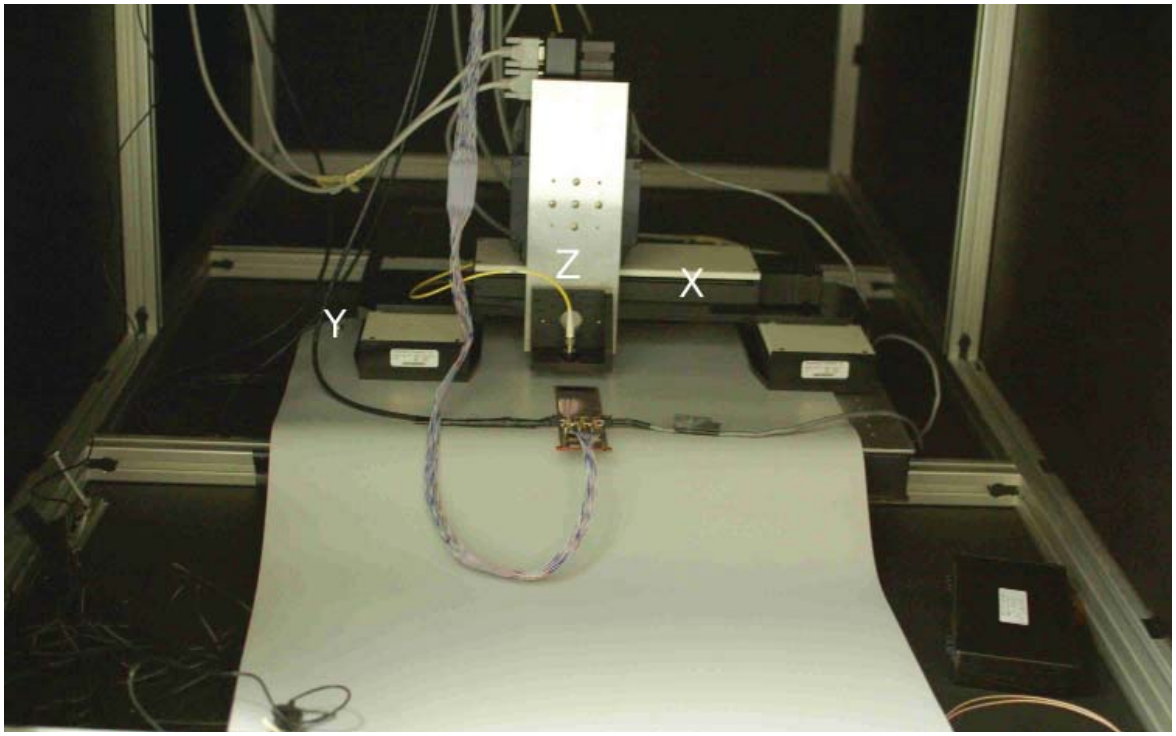


FIG. 12.1. Laser test stand *x*, *y*, and *z* rails inside dark box.

The data acquisition computer is a Dell Workstation 9200 that uses a Fedora Linux image as the primary operating system. The custom-made data acquisition cards from the Hall B instrumentation group are installed in the PCI bus of the computer. The data sets are analyzed using ROOT, a C++ data analysis framework developed by CERN.

The low voltage for the front-end electronics is supplied from a Tenma Model 72-6905 DC power supply. Bias voltage for the sensor is provided by an Ortec Model 710 Quad 1 kV Bias Supply, which is equipped with an overload circuit that trips at 20 μA, to prevent damage to the detector. When required for noise tests or as a diagnostic tool, the lab also is equipped with an Agilent model 33220A waveform generator, which is a 20 MHz synthesized function generator with a built-in arbitrary waveform and pulse generator.

Noise tests to measure the noise of the detector have been performed, as well as threshold and amplitude tests, which determine the sensitivity and the gain of the detector. Currently, the tests with the laser measuring physical quantities such as the amount of charge sharing between strips, voltage variation between strips, and the signal attenuation along the length of the sensor are being performed. Source tests are planned as well.

13 Quality Assurance, Commissioning, and Operation

The goal of the commissioning procedures is to ensure the quality of the SVT, by optimizing the sequence of operations during construction and installation, in terms of time, manpower, and computing resources; ensuring the proper functioning of the SVT before and after installation in Hall B; obtaining initial calibration data necessary for the reconstruction of physics events; determining the performance of the SVT; and optimizing the overall SVT configuration according to the requirement of the physics runs. SVT commissioning will be done in three phases: quality assurance (QA) and system checkout, commissioning without beam, and commissioning with beam.

For the first phase (QA and system check), QA planning is being done in conjunction with a value engineering (VE) approach for the design. It is expected that the VE for the SVT will improve the QA rating for the design. The steps that are taken for VE include: use of one module design, which allows for a lower number of spares and the possibility that modules can be interchanged between regions; previously-designed readout chips, which have been extensively studied and evaluated; standard circuit boards and electronic components, which will adhere to industry and Jefferson Lab standards; and off-the-shelf components.

QA and system checkout of the detector will consist of procedures that will be practiced, before and during assembly. On specific system components, such as ASICs, sensors, modules, cables, and electronics boards, QA procedures will measure their characteristics, check compliance with the specifications, verify that active components are responding correctly, and will enable the identification and replacement of faulty elements. Additionally, QA will include: encapsulation of the wire bonds to prevent breakage, requiring fiducial marks on silicon components for alignment; assembly in a clean room following established clean room rules; use of custom fixtures to prevent damage during shipment of components; and use of alignment markers on the support structure for detector installation.

System checkout procedure will be performed upon completion of assembly. System assembly procedures will include alignment and verification of the system positioning, as well as tests of high and low voltage systems, front-end electronics, readout electronics, data acquisition, and trigger systems.

The second phase will focus on the verification of the performance, after completion of the checkout procedures and before the beginning of the on-beam operation. The goal of this phase will be to optimize the system configuration, determine the initial calibration that will be used later in the reconstruction algorithm, and to verify that the system performance is consistent with the design goals. The verification will be achieved by data-taking with a radioactive source, laser as well as with cosmic rays in special configurations with dedicated equipment. Data will be collected in different configurations of the CLAS12 magnetic, data acquisition, and trigger to obtain the maximum information.

The third and final phase, commissioning, will be performed with beam. The commissioning of the SVT will be performed using the optimal configurations of beam energy and intensity, solenoid magnet, and the CLAS12 data acquisition. The accumulated data will be used to verify the response of the tracker to specific reactions, measure noise figures and rates, and determine the final detector calibration constant that is to be used by the CLAS12 reconstruction software.

13.1 Quality Assurance and System Checkout

Module performance tests will be done at various stages during module production at Fermilab and during assembly of the SVT at Jefferson Lab. These tests will check the sensor current behavior, the analog and digital functions of the FSSR2 ASICs, and measure the equivalent noise charge of the module. All test results will be documented and will serve as a reference for the module performance.

Sensor Current

The sensor current test checks that the sensor behaves like a diode and that it can be fully depleted. The current in the silicon sensor with applied reverse bias voltage is measured to check for breakdown problems. The reverse bias voltage induces a sensor current, which is composed of the generation current and the surface current. Generation current refers to the thermally-induced charge in the depletion layer and is therefore proportional to the depletion volume, which is proportional to $\sqrt{V_{bias}}$. The surface current can be approximated by an Ohmic resistance. The sensor behavior will be studied by plotting the measured leakage current versus increasing values of the sensor bias voltage to form an IV curve for each module. Each module uses six sensors, so the leakage current measured on the modules is the sum of the currents from multiple sensors. The maximum allowed leakage current (before irradiation) is 5 μA at V_{bias} = 100 V.

Analog Response of the Module Electronics

The readout of the strips will be tested to ascertain that strips can be read out and that the measured noise agrees with the expected value of the noise for that module. In the analog stage, the signal induced in the strip is amplified, shaped, and discriminated. A hit efficiency of 99% helps the tracking efficiency. Keeping the electronic noise occupancy as low as achievable, for instance $<10^{-3}$, reduces the number of false tracks.

For data-taking, the default setting of the threshold is chosen such that it corresponds to the output signal as created by an input signal equivalent to ~1 fC charge induced on the strip. A signal of 1 fC is well above the expected noise, and well below the average induced charge by the passage of a minimum ionizing charged particle. To find the threshold corresponding to 1 fC, the analog response needs to be reconstructed for each channel. The threshold set on a chip must have a well-known correspondence to the charge deposited in the detector. There is also a need for the threshold charge to be the same across the channels in a detector—if different channels responded differently to deposition of the nominal threshold charge, the track-finding algorithms would be biased by channels that have extra hits, which in turn leads to a requirement that the channel-to-channel variations in threshold and noise are kept to a minimum.

The FSSR2 ASIC has a base line restoration (BLR) circuit which can be turned on or turned off with BLR parameter. Typical pulse shape after the BLR is shown in Fig. 13.1.1 The threshold dispersion of the FSSR2 ASIC is within 500 e for BLR ON setting (800 e for BLR OFF) as shown in Fig. 13.1.2.

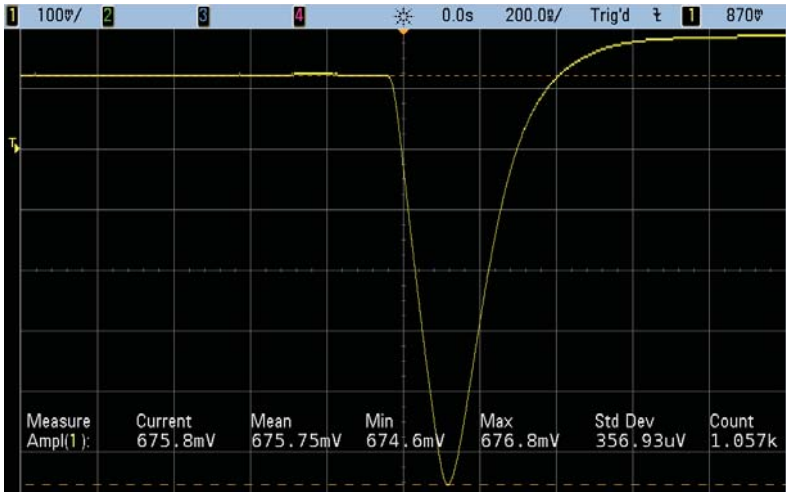


FIG. 13.1.1. Single channel analog output pulse measured after the base line restore circuit.

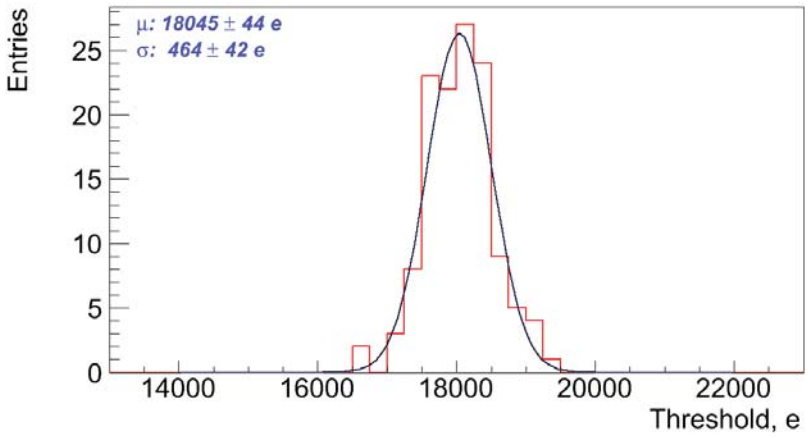


FIG. 13.1.2. Example of the chip threshold dispersion measurement.

Measuring the analog response signal on the strips allows the determination of the input noise of the strips. One of the goals is to keep the mean noise on the strips of a module less than 2000 electrons and the standard deviation to ≤500 e^-, which will for a threshold of V, guarantee noise occupancy on the silicon strips of less than 10^{-3}. The measurement of the input noise is used to determine the total number of usable channels in the SVT. To facilitate excellent tracking, it would be reasonable to expect about 99% of the channels to work. Several contiguous bad channels will reduce the sensitivity to multiple hits, hence the goal is to have as few as possible contiguous bad channels per module

Since the readout of the modules is by the FSSR2 ASIC, the analog channel response cannot be measured directly. The FSSR2 ASIC has a 3-bit FLASH ADC which is used for calibration. The analog response of the modules is reconstructed by injecting a calibration charge on the channel and measuring the corresponding occupancy over a range of threshold values. The calibration charge is generated by the charge injection circuitry of the readout chip. The injected charge is shaped and amplified in the analog circuitry to form an output signal. The discriminator threshold determines whether or not the output signal corresponded to a hit, so the probability that the injected charge produces a hit depends on the setting of the discriminator threshold. The average hit probability is measured by repeating the process of injecting charges and counting the fraction that produced a hit. This measurement is repeated over a range of threshold settings to produce an occupancy plot, the complementary error function Erfc, as shown in Fig. 13.1.3.

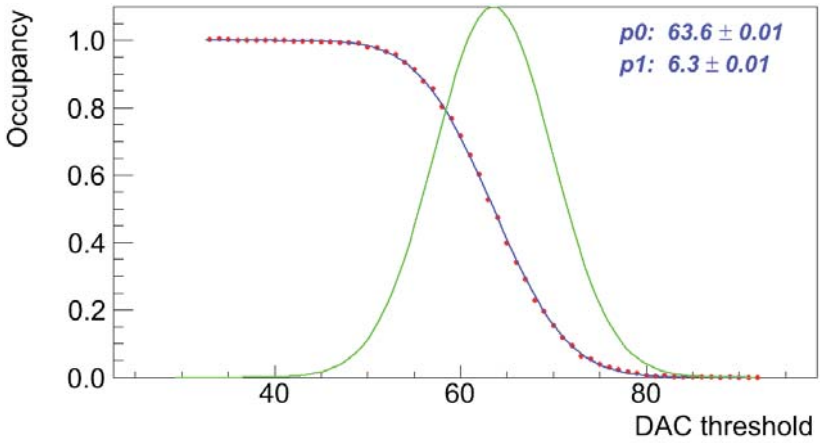


FIG. 13.1.3. Typical example of an S-curve (red dots) as measured on SVT channel. The corresponding fit (blue line) and signal response shape (green) as a function of signal height is also presented.

Erfc represents the probability *p* that a channel registers a hit at certain threshold voltage V_{thr}, given by:

$$p(V_{thr}) = \int_{V_{thr}}^{\infty} f(s)ds$$

where $f(s)$ is the probability density function that gives the chance of measuring a signal with a signal height s. The signal height distribution is assumed to be Gaussian:

$$f(s) = \frac{1}{\sigma_s\sqrt{2\pi}} \; e^{-(s-\mu_s)^2/2\sigma_s^2}$$

where μ_s is the mean signal height and σ_s is the RMS noise of the signal. In between the high and low threshold regions, the occupancy curve described by the error function can be fitted to the occupancy histogram for each channel and the mean value (discriminator threshold) and standard deviation (noise) can be determined. About 1000 events per threshold setting (~3% error) is recorded. Problem channels, such as those for which the fit fails, are tagged and placed in the database.

During the analog tests, Erfc-curves are measured for all FSSR2 ASIC channels over a range of values for the injected charge. The threshold setting at which the probability of getting a hit is 50%, corresponding to μ_s, is defined as the V_{th50}-point. The value of the V_{th50}-point for each channel should increase linearly with the value of the injected charge, while the output noise, s_s, is expected to be approximately constant as a function of the injected charge. In practice, the output noise of each channel on the module is determined as the value of σ_s from the Erfc-curve, obtained with a 3 fC input charge. (Scans with no charge injection are also part of the module characterization sequence.) By measuring the gain of the analog signal amplification, the input noise of each channel can be determined. The input noise can be used to identify several channel defects and helps to determine if the module can be properly biased.

The response curve is a 10-point gain scan. The data are then used to generate a response function, which maps injected charge to discriminator threshold.

Three Point Gain Test: the gain is determined for each FSSR2 ASIC by measuring Erfc-curves at three different values of the injected charge: 2 fC, 3 fC and 4 fC. One thousand events are sent for each bin and the range of threshold values is chosen according to the size of the injection charge. The gain in mV/fC is given by the slope of a linear fit to the three $\mathbf{V}_{th50}$-points, Fig. 13.1.4. The gain is used to measure the noise of a module and the similarity of response across the channels of a module. The output noise of each channel divided by the gain of the channel gives the value of the input noise.

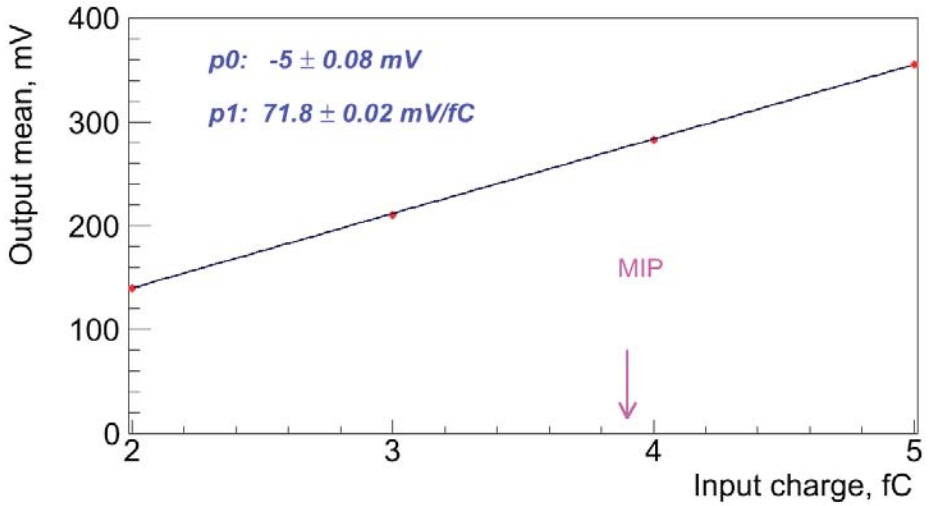


FIG. 13.1.4. Example of fit to determine gain (in mV/fC) from measurements of the $\mathbf{V}_{th50}$-points at four different values of the input charge. The $\mathbf{V}_{th50}$-points represent the average value for all channels on the readout chip.

For each channel, a straight line is fit to the mean and sigma parameters obtained from the three scans in the test. The slope represents the front-end amplifier gain, which is used to translate the noise recorded at the output of the amplifier to that seen at the input by the amplifier. The offset of the straight-line fit is recorded as well. Channels with 15% higher noise than average are tagged as defective. A summary of this data is recorded. The record includes the mean values of the gain of an FSSR2 ASIC, offset, output noise, and input noise. Also recorded for each FSSR2 ASIC are the parameters of the straight line fit.

The largest contribution to gain variation among the FSSR2 ASICs is due to the intrinsic ASIC-to-ASIC variation of gain. Changes in the low voltage or temperature can affect the gain of the readout channel as well. The response of all detector channels can be equalized during offline reconstruction by correcting the signal magnitude by a normalization factor. This procedure will be verified in further studies.

Figure 13.1.5 shows gain dispersion in one of the FSSR2 ASICs of the electrical-grade prototype module.

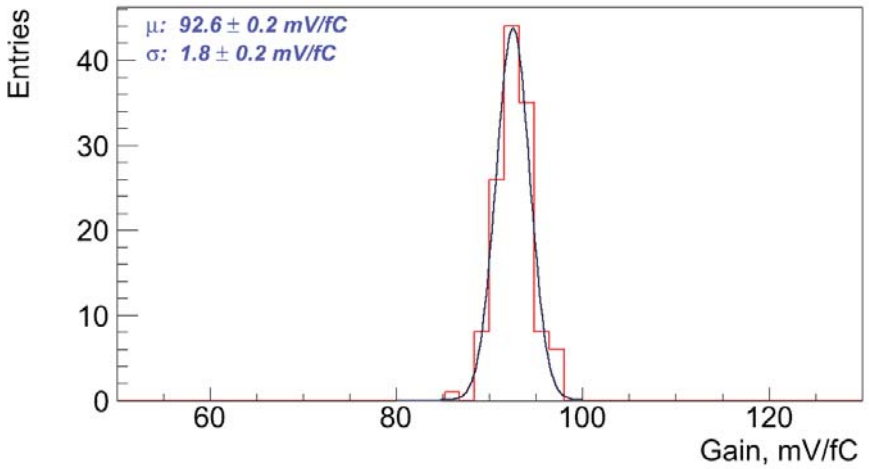


FIG. 13.1.5. Example of the channel gain dispersion measurement.

The noise and threshold dispersion constants for each channel must be measured, as these values are used by the zero-suppression algorithms implemented in the core logic of the FSSR2 ASIC and by calibration procedures which identify defective channels.

Noise is measured using external, low frequency calibration charge injected in the absence of signal. Noise calibration accounts for the different strip lengths and pitch adapter layouts that affect the input capacitance of the preamplifier. Threshold dispersion is defined to be the standard deviation of the means obtained from the parameters of the Erfc function fit. Fitting the mean noise versus silicon strip length, the following parameterization is obtained:

$$\text{Noise(e)} = A + B \times \text{length [cm]}.$$

Results of this parametrization should be compatible with the measurements performed during the SVT integration, prior to installation. Figure 13.1.6 shows examples of the input noise measured for the 256 channels of the top side of the electrical-grade prototype module.

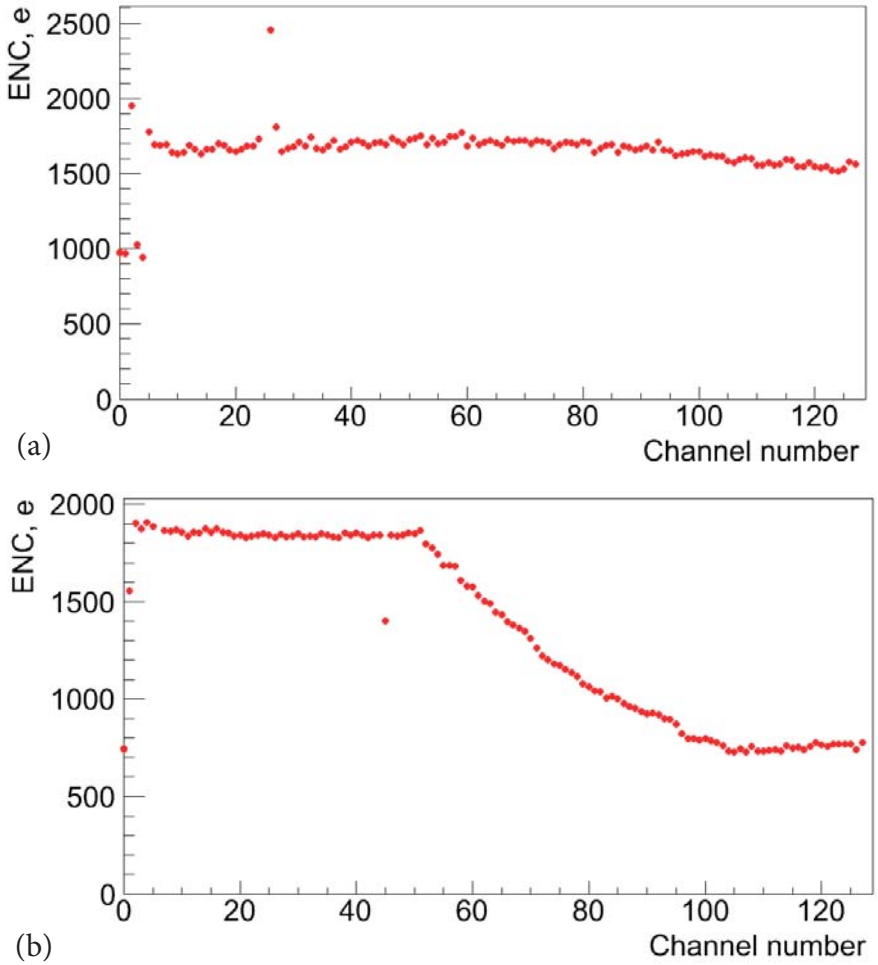


FIG. 13.1.6. Example of the input noise measured on the top side of the SVT module. (a) All channels of the FSSR2 ASIC are connected to the longest strips (~33 cm). (b) Part of the FSSR2 ASIC is wire bonded to the shorter strips due to variable pitch design of the sensors.

The average noise in these two FSSR2 ASICS is below 2000 electrons with a sigma of ~250 e^-. The expected value of the input noise depends on the length of the silicon strips as shown in Fig. 13.1.7.

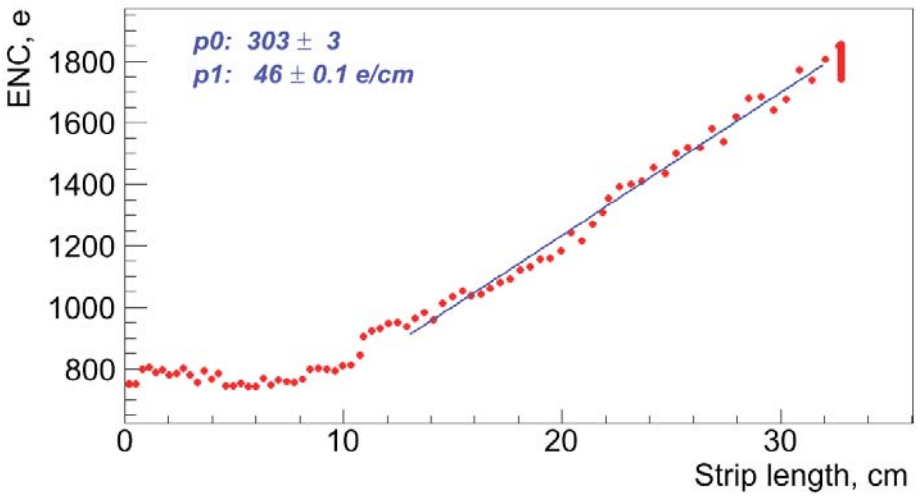


FIG. 13.1.7. Input noise versus strip length showing the straight line fit as expected from the linear dependence of the channel noise on the preamplifier capacitive load.

During calibration, a dedicated controller monitors the test results and when they are available, updates the configuration with the response curve parameters, and masks channels that are found to be defective. Calibration Client GUI monitors all the information and stores and displays a view of selected data, for instance the noise figures for all the active modules, in a color-coded diagram.

Noise sources of components on the module (sensors, pitch adapter, HFCB) can be identified and measured by plotting the ratio of the minimum to the median noise value for each FSSR2 ASIC. The ratio takes advantage of the fact that broken wire bonds on the detector modules effectively reduce the input capacitance to individual channels of the FSSR2 ASICs. Broken wire bonds can occur between, in ascending order of capacitance: the FSSR2 ASIC and pitch adapter, the pitch adapter and silicon sensor, and between the sensors. Fitting to these populations, corresponding to the previous broken wire bond configurations, provides an estimate of noise contributions from the above-mentioned components.

From the measurement of the input noise, several channel defects can be identified. The main channel defects are:

Dead: measured input noise = 0, no hits will be measured at any threshold for any injected charge.

Un-bonded: measured input noise is <800 e, most likely as a result of a broken bond between the FSSR2 and the first silicon strip sensor or the pitch adapter.

Partially-bonded: measured input noise is <1500 e (for the full three-sensor length of the strip), a result of a broken bond between the daisy-chained silicon sensors (the noise depends on the strip length).

Noisy: the input noise is greater than 1.15 times the average input noise of all channels on the same FSSR2 ASIC.

Hot: the input noise is greater than 1.25 times the average input noise of all channels on the same FSSR2 ASIC (the thresholds will be defined experimentally).

The assumptions made for the input noise of partially bonded and un-bonded channels is based on the fact that the capacitive load on the channel is decreased when the silicon strip sensor is removed from the readout chain, resulting in a lower noise contribution, typically ~1000–1500 e.

The input noise depends on the temperature of the silicon. The sensor temperature typically varies between modules and depends on the settings of the cooling used during the test. In the region of module temperatures (during the assembly tests), the temperature dependence of the input noise can be approximated by a linear function. The slopes of the straight-line fits can be used to apply a temperature correction to the average measured input noise on each module, so that all results for the input noise correspond to a hybrid temperature of 25 C.

Noise Occupancy Test: one scan (occupancy histogram) with no charge injection to find the noise value, see Fig. 13.1.8. This scan probes the tail of the noise distribution, which can show effects that are masked by the higher occupancy at low thresholds. The scan also provides a crosscheck of the noise value obtained from the response curve measurement.

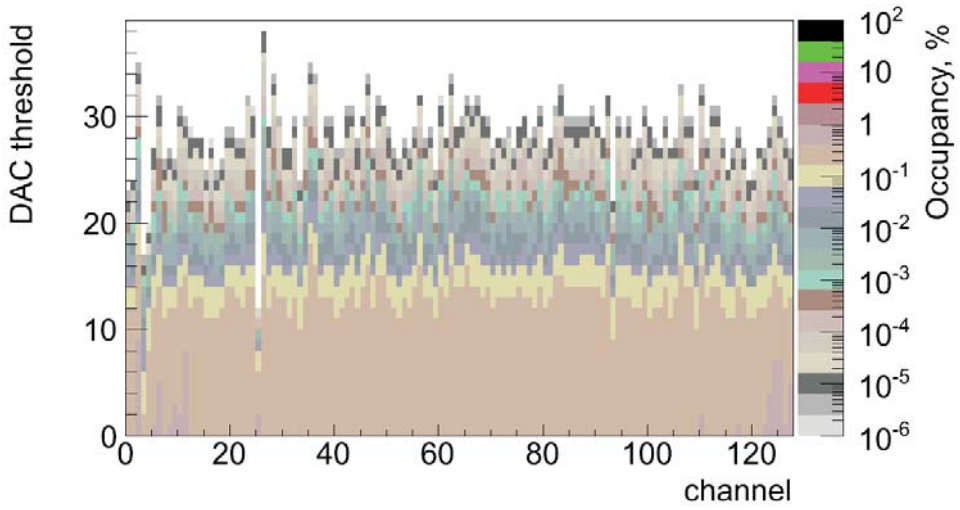


FIG. 13.1.8. Channel noise occupancy vs DAC hit/no-hit threshold (in DAC bins, One DAC bin corresponds to 3.5 mV).

It will be important to ensure that the input noise of the modules does not increase with services successively added to the system, as that would indicate problems in the grounding scheme and that common-mode noise has been introduced into the system.

Noise is one of the critical parameters that will affect the performance of the SVT. Though a direct comparison to the specification is not possible, due to the differences in the noise environments, the measurements can be used to verify uniformity and to reject modules with problems. Noise can be measured in two ways: interpolated from the noise measurements in the threshold scans using the calculated gain, or from the noise occupancy measurements at different thresholds. A fundamental difference between these two methods is the presence of the injection charge in the threshold measurements, which introduces extra circuitry. Additionally, the two analysis methods make different assumptions about the structure of the noise and of the front-end amplifier response curve at different threshold levels. The "noise" value is the input noise value calculated from the response curve test. The "noise occupancy" plots show the noise value calculated from the noise occupancy test.

Scan Production

The main function of the SVT data acquisition during calibration is to produce occupancy histograms for analysis by the higher-level data acquisition software, known as scans. The main parameters to describe a scan are: the configuration variable that is to change over the course of the scan, the values the configuration variable should take, the sequence of commands, known collectively as a trigger, sent to the modules for each event, the number of triggers to send, and which modules will send events to the data acquisition system.

A scan also can have some options that change the behavior of the scan process, for instance, whether the calibration line is in use or not. Once complete, a scan is identified to the data acquisition software by the run number, a scan number within the run, and the serial number of the module.

Many calibration histograms will have occupancies many times higher than that observed during a physics run. As the length of the bit-stream generated by the FSSR2 ASIC is proportional to the hit occupancy, the time taken to read out the FSSR2 ASIC is proportional to the hit occupancy. This means that the module cannot be read out at full speed, hence the trigger rate must either be slow enough to allow the readout of the maximum bit-stream length, or it must vary according to the actual occupancy recorded by the module during the scan.

The standard scan provides a histogram of the occupancy on a module as the threshold is varied. This is normally carried out with a particular amount of injected charge. Various scans are possible by modifying the various parameters on the scans. Two examples are the configuration check and noise occupancy. Configuration check is based on the probe scan and can be used to check the configuration of the connections between modules, which can then be compared to the configuration found in the database. The noise occupancy test scans thresholds around a 1 fC threshold, with no charge injection, and measures the occupancy, as shown in Fig. 13.1.9.

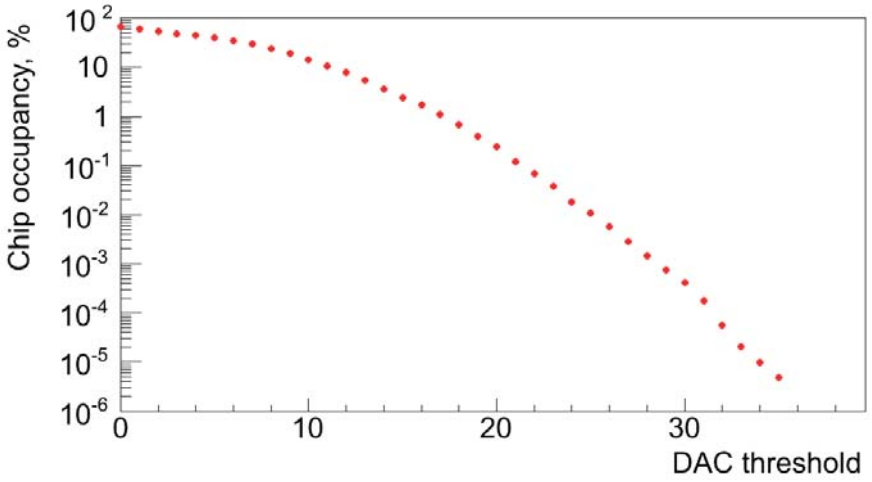


FIG. 13.1.9. FSSR2 ASIC occupancy vs. DAC hit/no-hit threshold.

To measure the lowest occupancy at high thresholds, about a million events are sent to the modules. At low thresholds and high occupancies, recording this many events takes a prohibitive amount of time, therefore the number of events sent to the module is reduced. The histogram code is constrained to send a constant number of events for each threshold setting. To send different numbers of events to different bins in the histogram, the procedure is repeated starting at a different bin each time. The first round puts the lowest number of events in all the bins. Subsequent repetitions accumulate more events in the later bins until all the requested events have been sent.

Digital Response of the Module Electronics

The digital tests check the ability of the FSSR2 ASICs to read out data from the module. All digital tests will be based on measuring the occupancy of each channel while varying a specific setting in the FSSR2 ASIC configuration. In addition to this, the channel masking and the FSSR2 ASIC's basic functions are tested Cabling has to be verified before the digital tests take place, as problems with the module communication would lead to test failures.

When first powered, basic communication is confirmed when the SVT modules write to the FSSR2 ASIC registers and read back their response. The front-end electronics will be set up to return the contents of their configuration registers, so a known bit pattern can be expected. A hard-reset test checks the initialization of the modules. Once the module has been checked for power and readout response, its performance can be tested.

A mask can be applied to the channels of the FSSR2 ASIC. A channel that is masked always returns 0. Masking is necessary for strip channels with high noise, as unmasked noisy channels add noise hits and increase the amount of data that has to be read out.

To check the capability of the FSSR2 ASICs to turn a mask on or to turn it off, the occupancy is measured using different settings of the mask register. During the test, the output is set such that any channel which is not masked returns a 1. The test starts with a mask register by which all channels are unmasked. For each consecutive mask register in the test, one more channel on each FSSR2 ASIC is masked, until all channels are masked by the final mask register. The result of this test is a 2D projection of a 3D histogram, where the shade of color indicates the occupancy as a function of the channel number and the mask register. If there is a channel that will need to be masked due to high noise, which also has a masking defect, it will have to be masked offline.

The binary threshold must be set so that a channel can effectively distinguish between the signal and noise. This means that the response to different signals must be known and the noise must be low enough to be excluded.

The testing of SVT modules is a check of their calibration and performance and also of the system itself. The key to the characterization of the modules lies in reconstructing the analog response of the modules from the binary readout by first setting the optimal chip parameters for the charge injection, then injecting a set of charges into the front-end, and scanning with the threshold to map out the response curve. A full test sequence contains procedures that verify the digital performance of the FSSR2 ASICs. These procedures exercise and test the channel mask registers and FSSR2 ASIC's logic.

13.2 SVT Assembly and Integration

The position resolution of the detector can be compromised if the alignment is not known. Strict positional tolerances are imposed so that minimal corrections need to be made to measurements. Therefore, both the position of the sensors with respect to each other and with respect to alignment points are measured and controlled during module production. A mechanical survey and metrology will be carried out before electrical testing. The metrology of the module checks whether the module fits within a well-defined envelope. This check ensures that a module will have no interference with other modules, both while on the support structure and particularly during mounting, where module separation reaches a minimum. QA testing of module components is described in [11].

Prerequisite for the module assembly is the QA test of the HFCB, after FSSR2 ASIC wire bonding. This test will be done at the dedicated test station at the Silicon Detector Facility (SiDet), Fermilab. Full electrical functionality of all the channels will be verified, and ENC data will be recorded for every FSSR2 ASIC in a database, along with total current on the low voltage lines. Additionally, a basic functionality test will be done after encapsulation of FSSR2 ASIC-to-HFCB wire bonds. Immediately after module assembly, the module will be tested in the clean room at SiDet. The aim of this test is to identify defects in the modules as early as possible in production, to provide an opportunity to fix the defect so that effort is not expended on faulty modules. Defective modules will be repaired.

Modules will be mounted inside carrier boxes and transported to Jefferson Lab. Upon arrival, the modules, still within the carrier boxes, will be tested in the clean room in the EEL building to check whether any problems developed during handling and transport. The module can be powered, cooled, and operated in this carrier box. The carrier box will be constructed to provide access to both sides of the module to facilitate inspection and debugging. The carrier box will be closed during the testing to prevent exposure of the silicon sensors to ambient light and to contain the nitrogen being flushed through the box, which will keep the dew point well below the temperature of the cooling circuits, preventing condensation on the modules.

After the reception tests, modules will be placed on the SVT support structure. After placement of each module on the support, all the modules on the support will be re-tested to find and resolve problems with cables routed on the outside of the cylinder. Defective modules will be replaced. Once assembly is completed, a light-tight Faraday cage will enclose the SVT. Dry air will be flushed through the SVT and the modules will be cooled. The SVT protection cover will be designed to safely transport the SVT from the Experimental Equipment Lab to Hall B.

With the SVT in its final position in the CLAS12 detector, all the modules will be re-tested with the services that will be used to operate the SVT during data-taking.

13.3 Final Commissioning

After installation in Hall B, the SVT will be tested to identify problems that may have occurred during installation of the detector. A series of runs will be performed with and without the beam and with and without the magnetic field, four configurations in all.

For each of these configurations, the tests for the module performance will be repeated. Tests at later stages will be aimed at finding problems with data acquisition and services, such as the power supplies and cables, and ensuring that no common mode noise was added to the system due to improper grounding/shielding.

13.4 Safety

All activities will be analyzed in accordance with the Jefferson Lab ES&H Manual to identify hazards associated with the work and safety requirements. Personnel involved in an activity and in the vicinity will be briefed on all potential hazards involved with the activities. All activities are considered low risk, common, and routine in nature and are all fully covered by the ES&H Manual.

All activities will be coordinated by written procedures that are reviewed by the safety staff. Administrative procedures will be in place to prevent accidental shocks from power supplies. Workers will receive training prior to performing any activity on the detectors. Safety is an integral part of all activities.

14 Collaboration

At present, the SVT collaboration consists of the following institutions:
Moscow State University, Moscow, Russia
State Scientific Center of the Russian Federation-Institute for Theoretical and Expermental Physics, Moscow, Russia
University of New Hampshire, Durham, NH, USA
Fermilab, Batavia, IL, USA
Institut de Physique Theoretique CEA/Saclay, Gif-sur-Yvette, France

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