8086 and Memory Interfacing

Memory organization

- In the design of all computers, semiconductor memories are used as primary storage for data and code
- They are connected directly to the CPU and they are the memory the CPU asks for information (code or data)
- Among the most widely used are RAM and ROM
- The physical address space, or memory map, of a microprocessor refers to the range of addresses of memory location that can accessed by the microprocessor. The size of the address space depends on the number of address lines of the microprocessor.
- At least two memory devices are required in a microprocessor system: one for the ROM and one for the RAM.

Memory Capacity

- The number of bits/bytes that a semiconductor memory chip can store is called its chip capacity

Memory organization

A memory device or memory chip must have four types of lines or connections: **Address, Data, Enable and Control.**

Address Lines:

- The input lines that select a memory location within the memory device.
- Decoders are used, inside the memory chip, to select a specific location
- The number of address pins on a memory chip specifies the number of memory locations.

If '**n**' specifies the number of address lines, then

Number of memory location = 2^n

Memory organization

Data Lines:

- The data pins are typically bi-directional in read-write memories.
- The number of data pins is related to the size of the memory location .
  For example, an 8-bit wide (byte-wide) memory device has **8** data pins
- The number of data lines (m-bits) determines the size of each location in the memory.

Memory Capacity = 2^n x m

Memory organization

Enable Lines:

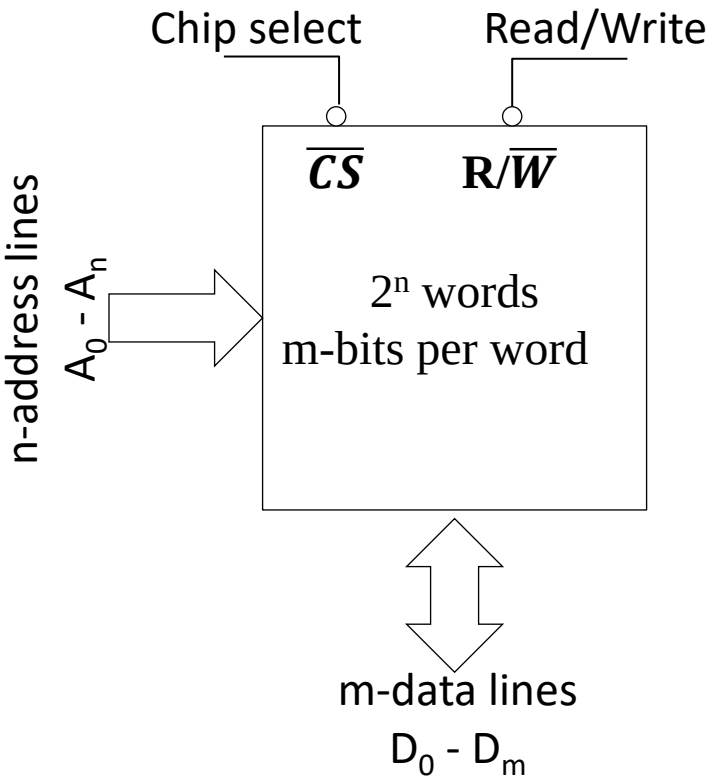
- All memory devices have at least one **Chip Select ($\overline{CS}$)** or **Chip Enable ($\overline{CE}$)** input, used to select or enable the memory device.
  - If a device is not selected or enabled then no data can be read from, or written into it.
  - The $\overline{CS}$ or $\overline{CE}$ input is usually controlled by the microprocessor through the higher address lines via an **address decoding circuit**.

Memory organization

Control Lines:

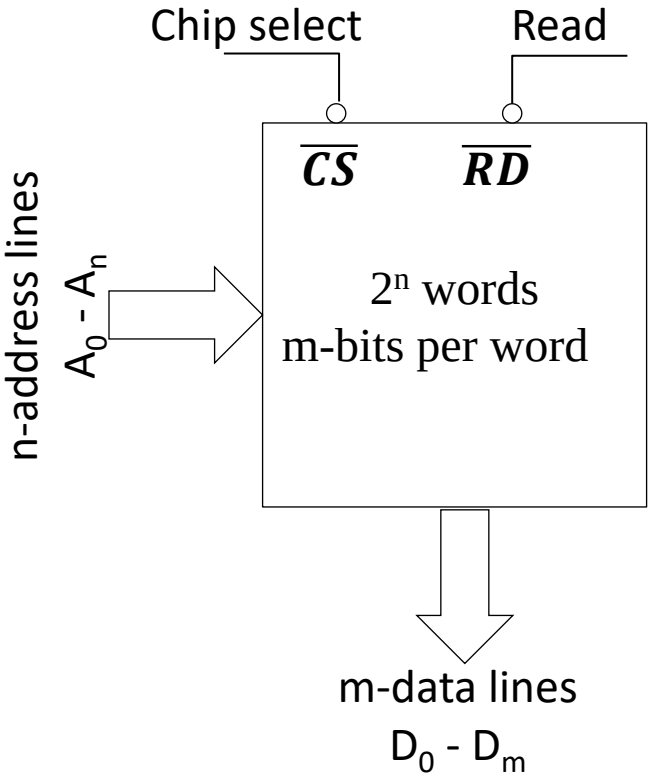
- RAM chips have two control input signals that specify the type of memory operation: the **Read ($\overline{RD}$)**and the **Write ($\overline{WR}$)** signals.
  - Some RAM chips have a common **Read /Write (R/$\overline{W}$)** signal.
- ROM chips can perform only memory read operations, thus there is no need for a Write **($\overline{WR}$)** signal.
  - In most real ROM devices the Read signal is called the **Output Enable ($\overline{OE}$)** signal.

Memory organization

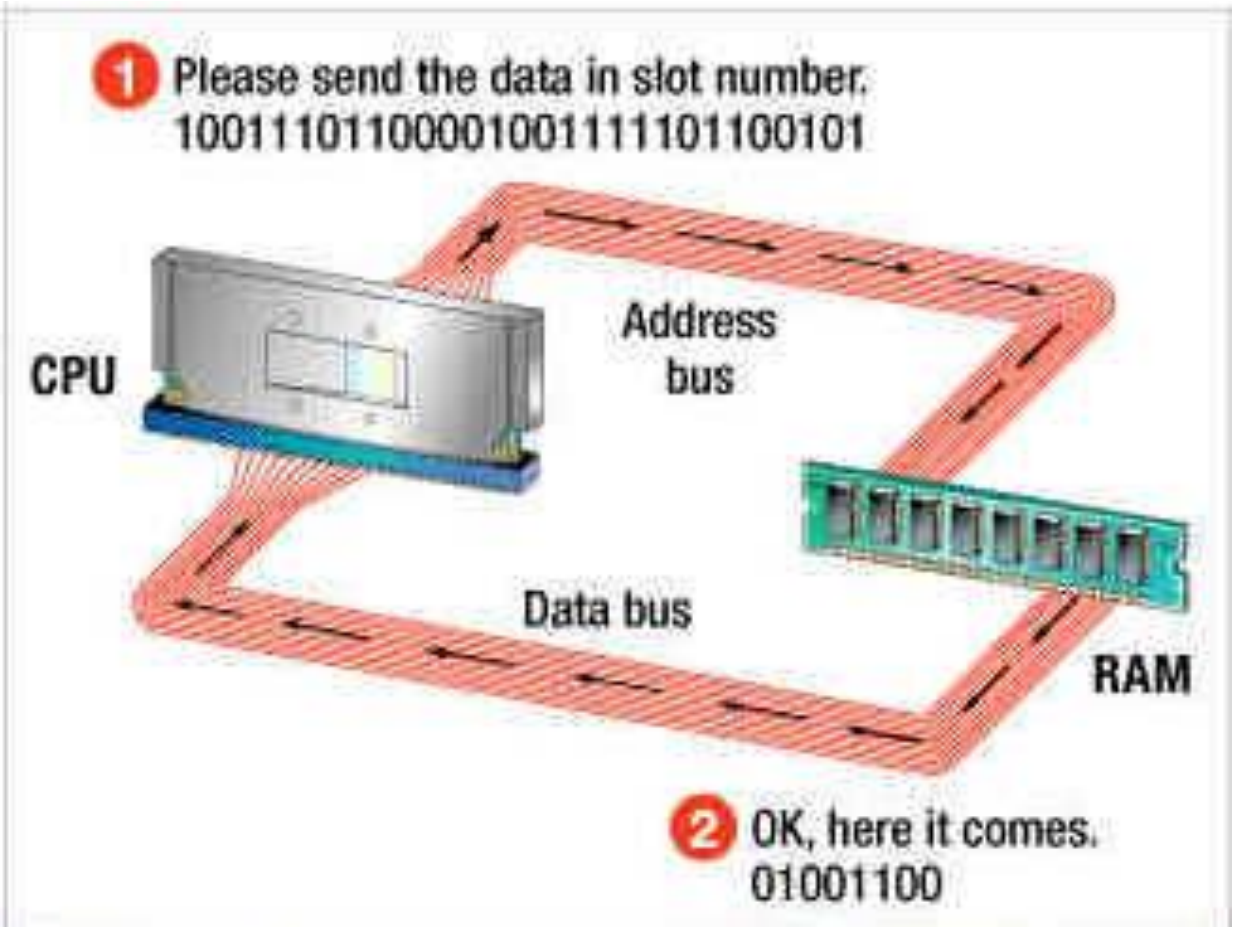


RAM Memory Chip

Memory organization



ROM Memory Chip


1 Please send the data in slot number.
10011101100001001111101100101
CPU
Address bus
Data bus
RAM
2 OK, here it comes.
01001100

Memory organization

Memory address		Memory contents
Binary	Decimal	
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	.	.
	.	.
	.	.
	.	.
	.	.
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

Memory organization

A RAM should be able to:

- Store many words, one per address
- Read the word that was saved at a particular address
- Change the word that's saved at a particular address

	Prefix	Base 2	Base 10
K	Kilo	$2^{10} = 1{,}024$	$10^{3} = 1{,}000$
M	Mega	$2^{20} = 1{,}048{,}576$	$10^{6} = 1{,}000{,}000$
G	Giga	$2^{30} = 1{,}073{,}741{,}824$	$10^{9} = 1{,}000{,}000{,}000$

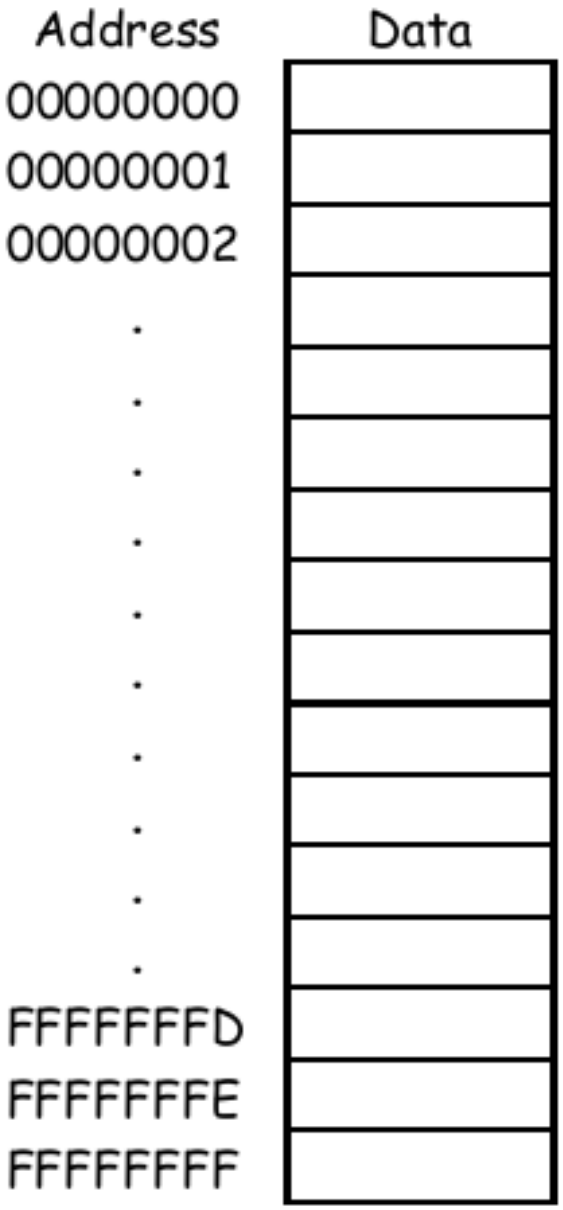
Memory organization

Memory capacity

- The number of bits that a semiconductor memory chip can store is called its memory capacity.

kapasite	sembol		deger
1 bit	Bit	=	0 1
1 byte	Byte	=	8 bit
1 Kilobyte	KB	=	1024 bytes
1 Megabyte	MB	=	1024 KB
1 Gigabyte	GB	=	1024 MB
1 Terabyte	TB	=	1024 GB

- The address serves as an array index.
- Each address refers to one word of data.



1. Calculate total addressable memory in a RAM chip when there is a 16-bit data bus and a 32-bit address bus.

2. Calculate total addressable memory in a ROM chip when there is a 32-bit data bus and a 16-bit address bus.

1. Calculate total addressable memory when there is a 16-bit data bus and a 32-bit address bus.

   $2^{32} \times 2 = 4GB \times 2 = 8GB$

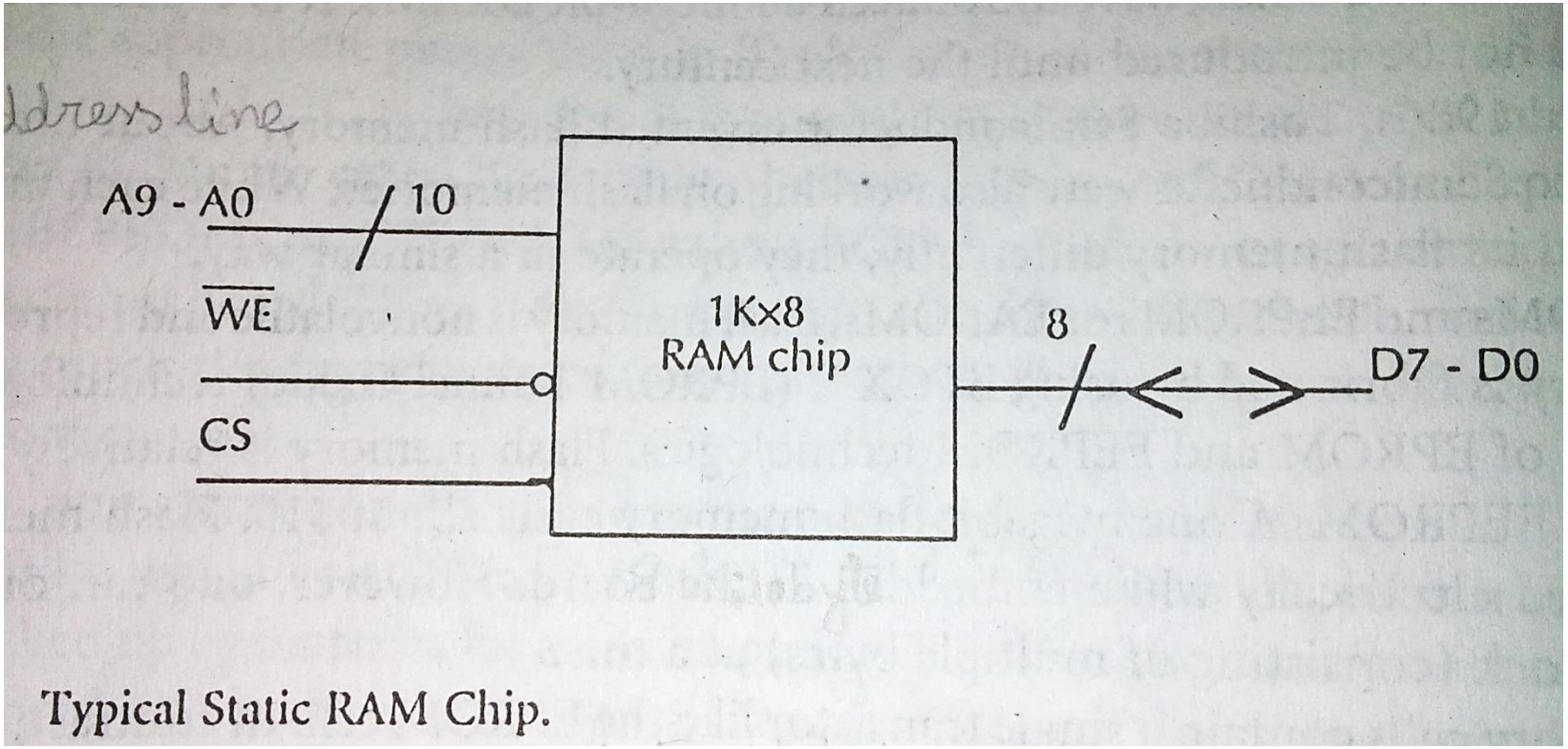
2. Calculate total addressable memory when there is a 32-bit data bus and a 16-bit address bus.

   $2^{16} \times 4 = 64K \times 4 = 256K$

Operation of RAM chip

- RAM is also called volatile memory because they will not retain data without power
- The main difference between ROM and RAM is that RAM is written under normal operation, whereas ROM is programmed outside the computer and normally is only read.

Typical RAM chip



Typical Static RAM Chip.

Operation of RAM chip

CS	WE’	MODE	Status of D7 – D0	Power
L	X	Not selected	High Impedance (as if it is disconnected)	Standby
H	L	Write	Acts as input bus	Active
H	H	Read	Acts as output bus	Active

a. When CS input is LOW, the chip is not selected. Because, D7-D0 is in high impedance state. The memory chip is disabled and reduces it’s power requirement. This feature reduces around 86% power.

High impedance circuit are low current, high voltage

Operation of RAM chip

CS	WE’	MODE	Status of D7 – D0	Power
L	X	Not selected	High Impedance	Standby
H	L	Write	Acts as input bus	Active
H	H	Read	Acts as output bus	Active

b. When CS=HIGH, WE’=LOW then data on lines D7-D0 are written into word, addressed by A9-A0.

c. When CS=HIGH, WE’=HIGH then contents of the memory word whose address is specified by the address line A9-A0 will appear on data lines D7-D0.

The number of bits that a CPU/memory chip can process at one time.

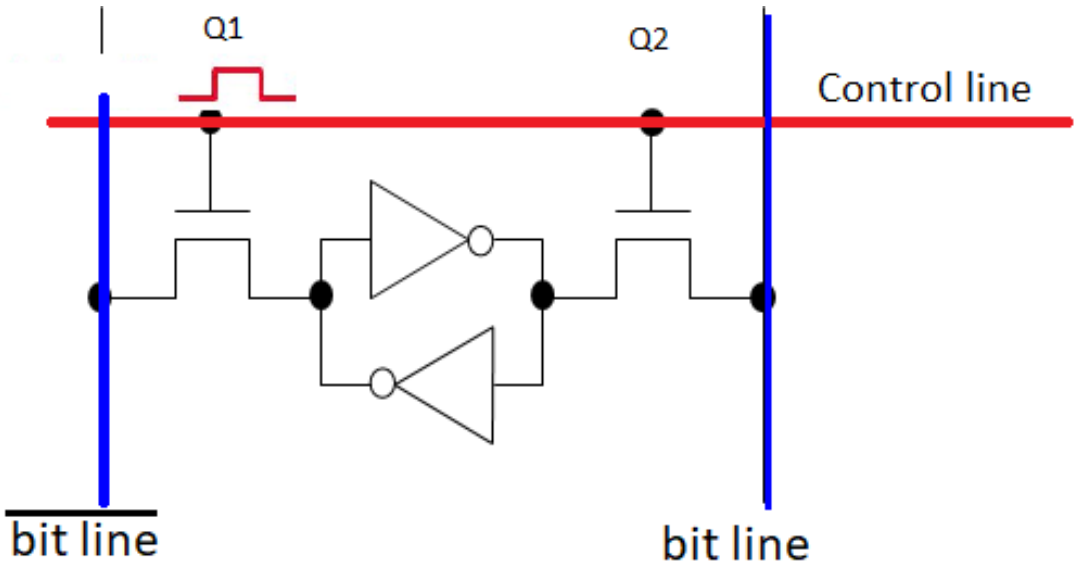
Types of RAM Devices

- Static RAM
- Dynamic RAM

Static RAM (SRAM) Devices

- Static RAM memory devices retain data for as long as DC power is applied.
- Because no special action is required to retain data, these devices are called static memory.

Data is written into the cell by applying the data and its complement at the bitline and $\overline{\text{bitline}}$ inputs respectively, with Q1 and Q2 in the ON condition.



SRAM Cell

Static RAM (SRAM) Devices

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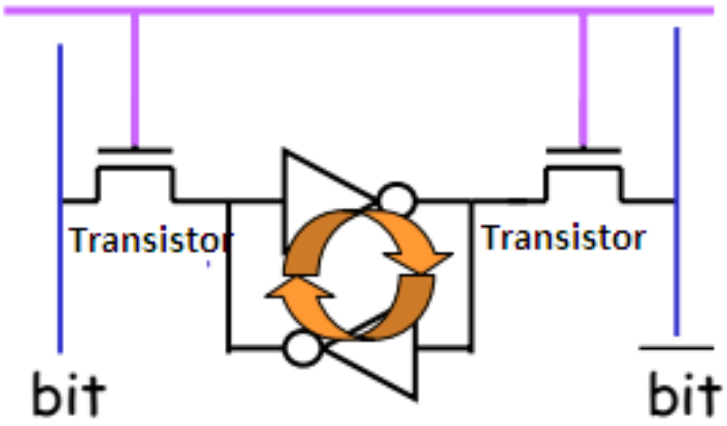
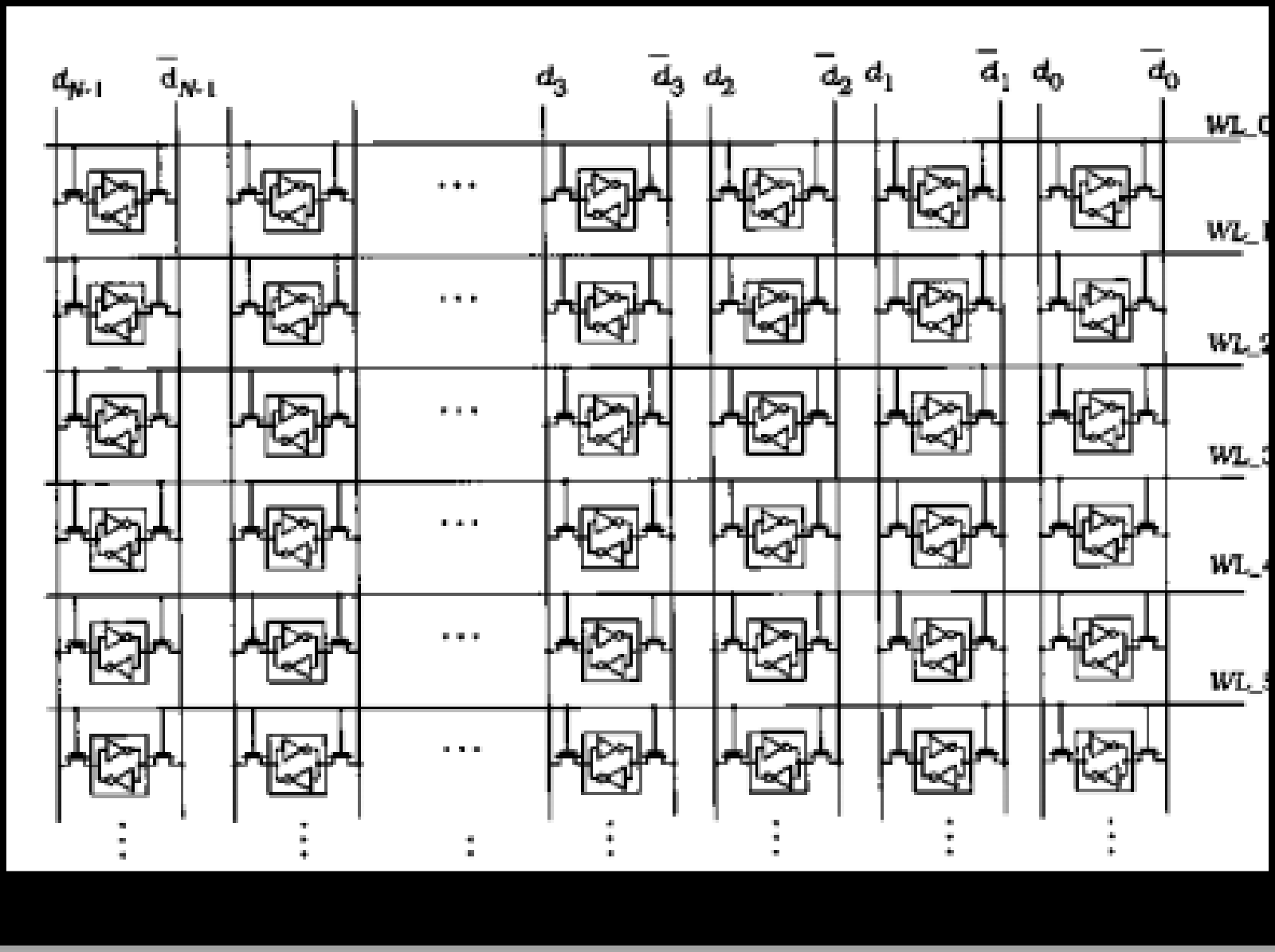


SRAM Cell


d_{N-1}
$\overline{d}_{N-1}$
d_3
$\overline{d}_3$
d_2
$\overline{d}_2$
d_1
$\overline{d}_1$
d_0
$\overline{d}_0$
WL_0
WL_1
WL_2
WL_3
WL_4
WL_5

DRAM Memory

- Inside a dynamic RAM chip, each memory cell holds one bit of information and is made up of two parts: a transistor and a capacitor.
- The capacitor holds the bit of information -- a 0 or a 1. The transistor acts as a switch that lets the control circuitry on the memory chip read the capacitor or change its state.
- For dynamic memory to work, either the CPU or the memory controller has to come along and recharge all of the capacitors holding a 1 before they discharge. To do this, the memory controller reads the memory and then writes it right back. This refresh operation happens automatically thousands of times per second.

DRAM & SRAM Memory

- This refresh operation is where dynamic RAM gets its name. Dynamic RAM has to be dynamically refreshed all of the time or it forgets what it is holding. The downside of all of this refreshing is that it takes time and slows down the memory.
- Static RAM uses a completely different technology. In static RAM, a form of flip-flop holds each bit of memory. A flip-flop for a memory cell takes 4 or 6 transistors along with some wiring, but never has to be refreshed. This makes static RAM significantly faster than dynamic RAM. However, because it has more parts, a static memory cell takes a lot more space on a chip than a dynamic memory cell. Therefore it holds less memory per chip, and that makes static RAM a lot more expensive.

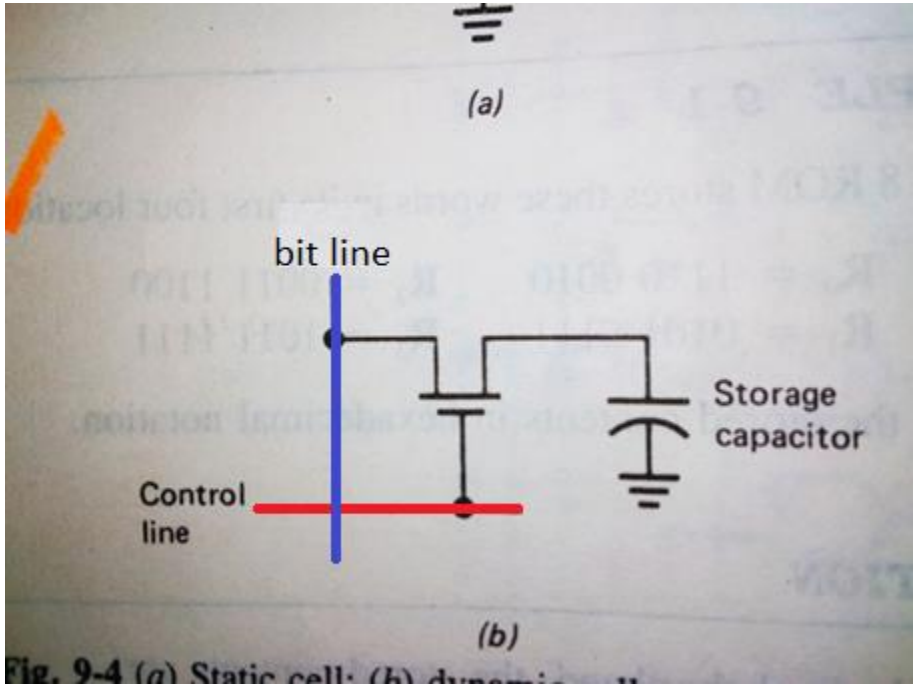
DRAM & SRAM Memory

- Static RAM is fast and expensive, and dynamic RAM is less expensive and slower. Therefore static RAM is used to create the CPU's speed-sensitive cache memory, while dynamic RAM forms the larger system RAM space.

Dynamic RAM (DRAM) Memory

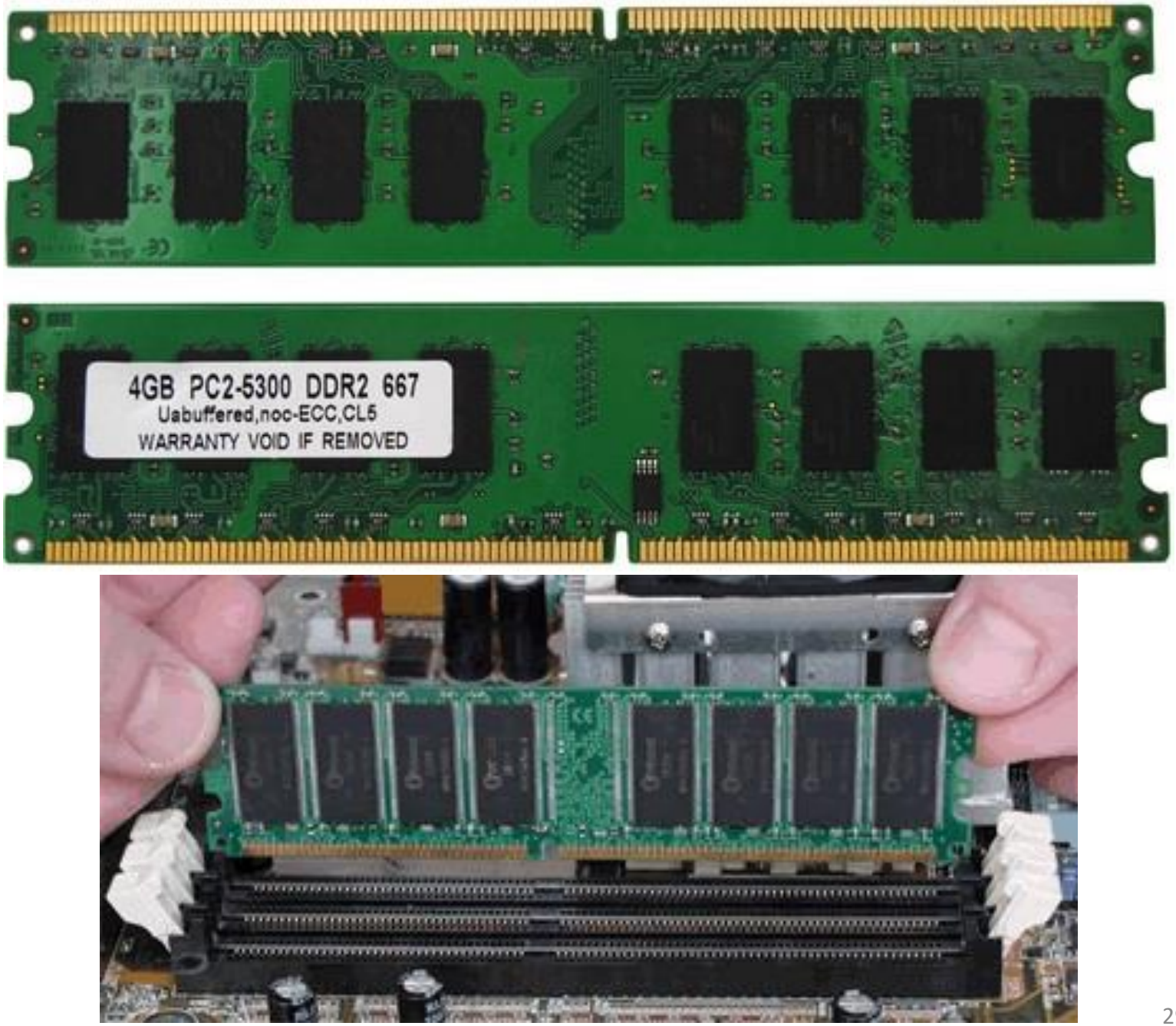
- DRAM is essentially the same as SRAM, except that it retains data for only 2 or 4 ms on an integrated capacitor.
- After 2 or 4 ms, the contents of the DRAM must be completely rewritten (refreshed) because the capacitors, which store a logic 1 or logic 0, lose their charges.

DRAM Cell



Difference between SRAM VS DRAM

SRAM	DRAM
SRAM uses flipflops.	DRAM uses capacitors.
Stores data till power is supplied.	Stores data only for few seconds even when power is supplied.
Does not refresh the memory cell.	Continuous refreshing is required to retain data.
Data access is faster.	Data access is slower.
Consume less power.	Consume more power.
Less memory per chip because bit density is low compared to DRAM. Therefore, Cost per bit is high.	More memory per chip. Since only a single transistor and a capacitor are employed to store a bit. Therefore, Cost per bit is low.


4GB PC2-5300 DDR2 667
Uabuffered,noc-ECC,CL5
WARRANTY VOID IF REMOVED

Memory Decoding

- In general, all the memory locations are not implemented.
- All the address are not used by the memory devices to select particular memory locations.
- The unused lines are used to decode to generate chip select signals.
- Basically, two techniques are used to decode the address
    1. Linear or Partial decoding
    2. Absolute or Full decoding

Memory Decoding

Linear decoding/Partial Decoding

- All the address lines are not used to generate chip select, basically used in small systems
- Individual high order address lines are used to decode the chip select for the memory chips using less hardware
- Disadvantages: Each memory location has more than one address called memory foldback.

Check Rafiquzzaman book

Memory Decoding

Draw the diagram of 8-bit microprocessor with 16 bit address bus and 8 bit data bus interfaced with 6KB RAM using linear decoding method. Each RAM chip has 10 bit address bus and 8 bit data bus. Also provide the corresponding address map (starting address and end address) for each RAM chip

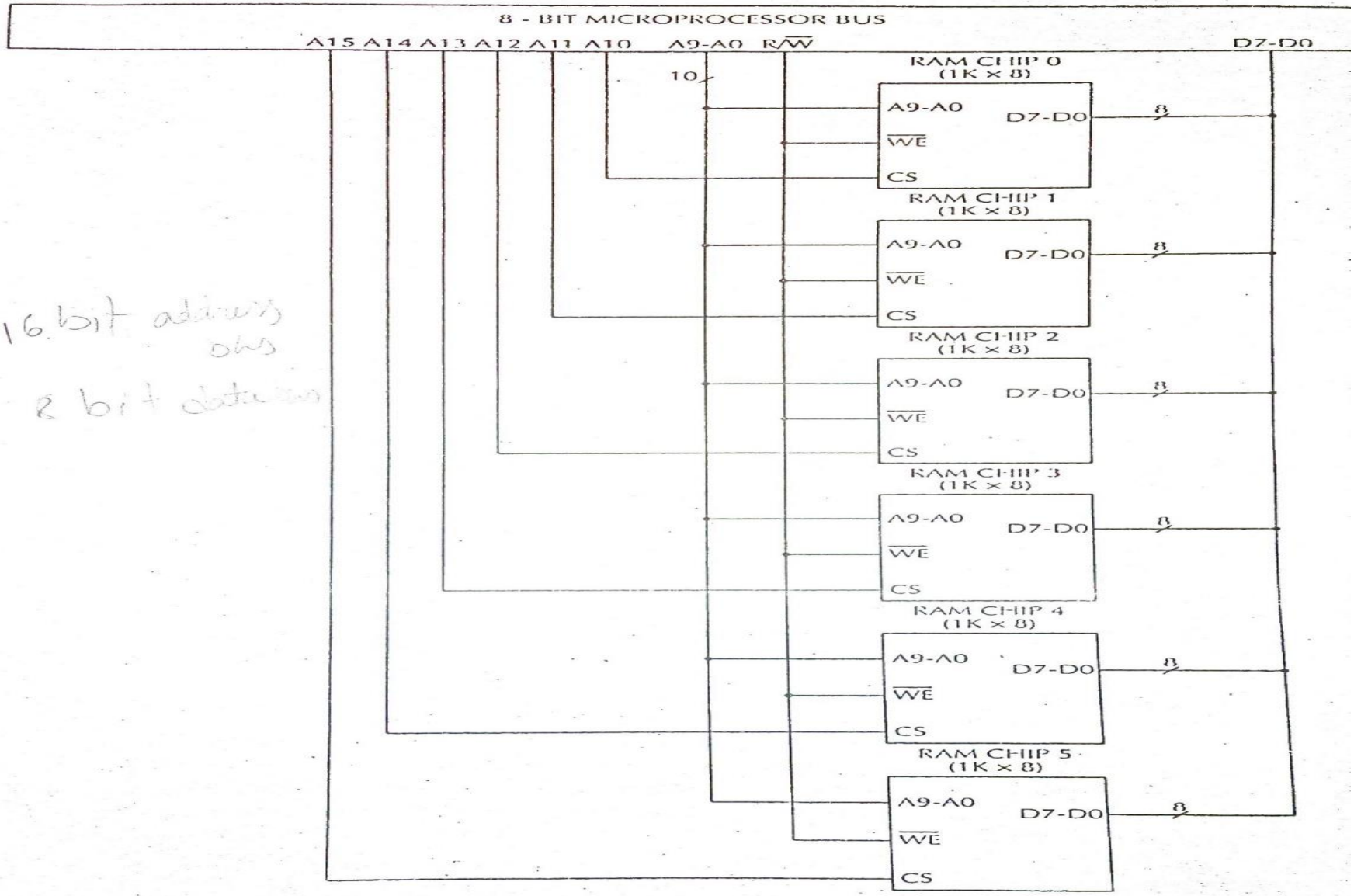


FIGURE 1.5 An 8-bit microprocessor interfaced to a 6K RAM system using the linear select decoding technique.

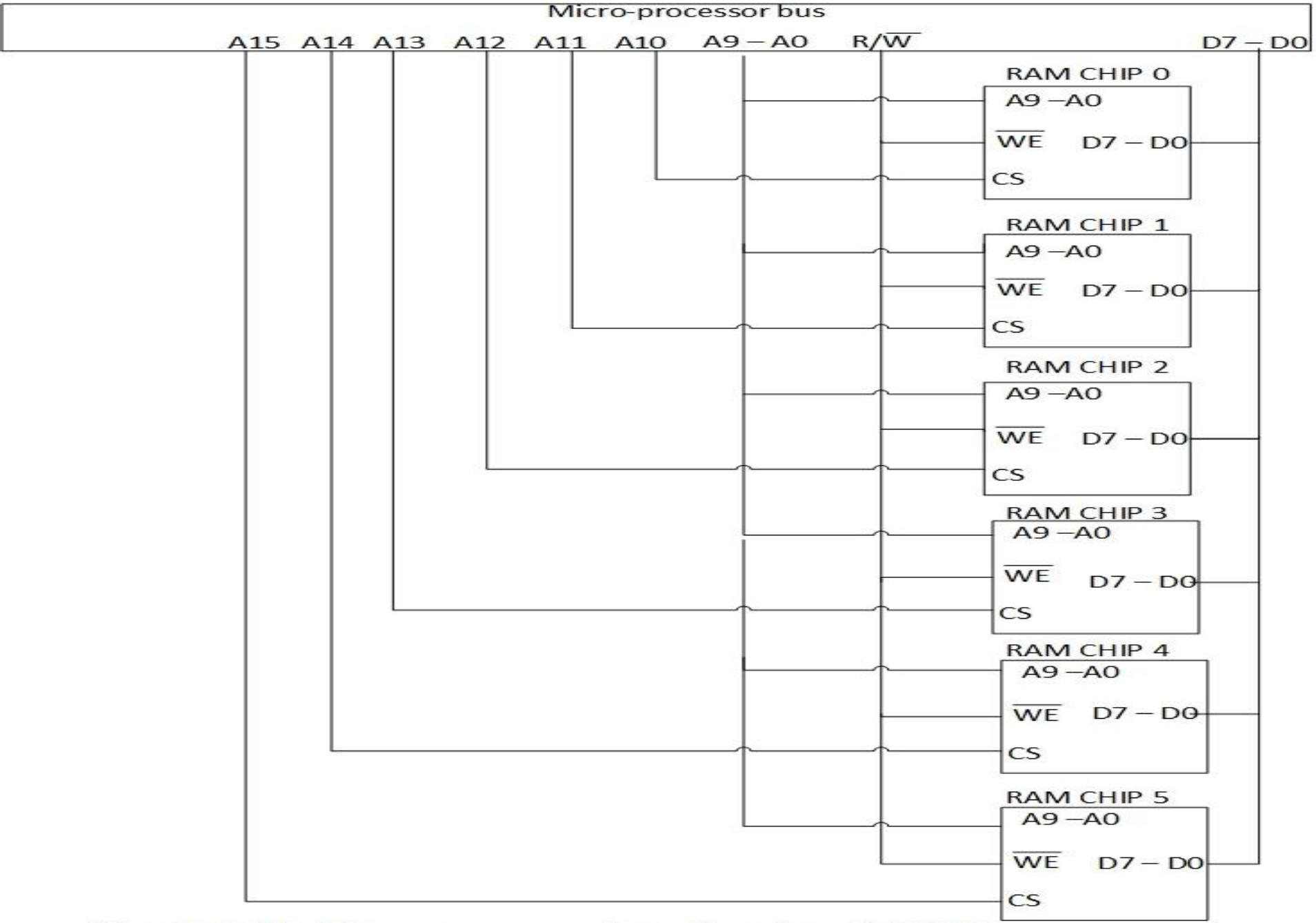


Fig. An 8-bit Micro-processor interfaced to 6k RAM system using Linear decoding

Address map

Binary Address Pattern A15 A14 A13 A12 A11 A10 A9 A7 A6 A5 A4 A3 A2 A1 A0	Device Selected	Address Assignment in Hex
0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 . . . . 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1	RAM CHIP 0	0400 to 07FF
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 . . . . 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1	RAM CHIP 1	0800 to 0BFF
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 . . . . 0 0 0 1 0 0 1 1 1 1 1 1 1 1 1	RAM CHIP 2	1000 to 13FF
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 . . . . 0 0 1 0 0 0 1 1 1 1 1 1 1 1 1	RAM CHIP 3	2000 to 23FF
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 . . . . 0 1 0 0 0 0 1 1 1 1 1 1 1 1 1	RAM CHIP 4	4000 to 43FF
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 . . . . 1 0 0 0 0 0 1 1 1 1 1 1 1 1 1	RAM CHIP 5	8000 to 83FF

Drawback

- For 8-bit microprocessor with 16 bit address bus and 8 bit data bus, we have 64KB of RAM memory space. However, we can interface with 6KB of RAM memory space where each RAM chip has 10 bit address bus and 8 bit data bus. This means that this idea wastes address space.
- The address map is not contiguous, rather, it is sparsely distributed.
- Address line A10 and A11 connected with RAM chip select (CS) of RAM chip 0 and 1. If both A10 and A11 are high at the same time then a bus conflict occurs. This can be avoided by proper programming to select desired memory chip.

Drawback

- If all unused address lines are not utilized as chip select then total memory size is reduced. It is called memory foldback and it wastes memory space. For example, if A15 is don't care in design then memory size is reduced from 6KB to 5 KB.

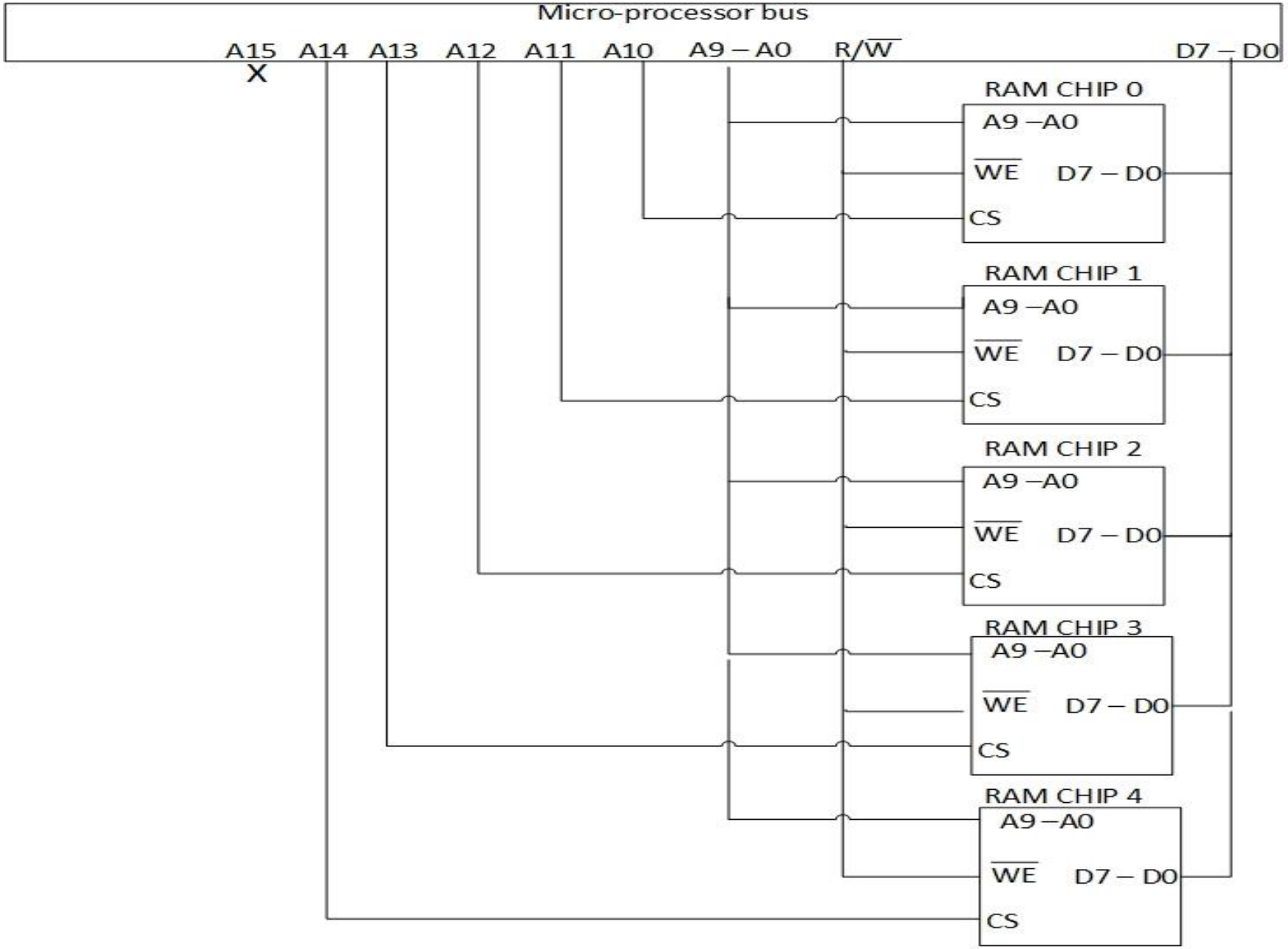


Fig. An 8-bit Micro-processor interfaced to 5k RAM system using Linear decoding

Memory Decoding

Full Decoding

- All of the higher address lines are decoded to select memory chip, and the chip is selected only for the specified logic levels on these high order address lines.
- Each memory location has unique address
- Disadvantages: it needs more hardware for decoding

Memory Decoding

Full Decoding

Draw the diagram of an 8-bit microprocessor with 16 bit address bus and 8 bit data bus interfaced to 4KB RAM system using the full decoding method. Each RAM chip has 10 bit address bus and 8 bit data bus. Provide the corresponding address map (starting address and end address) for each RAM chip.

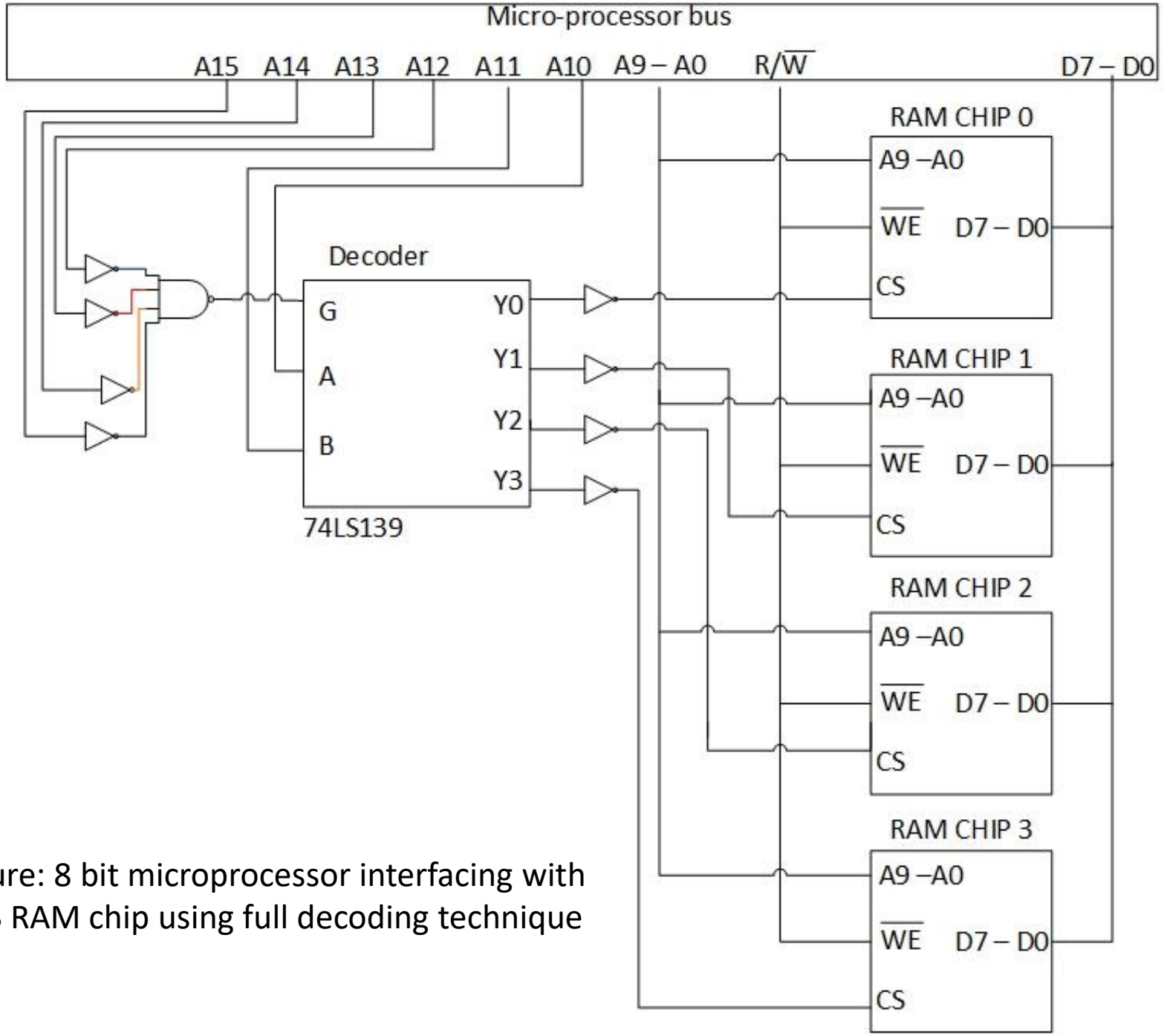
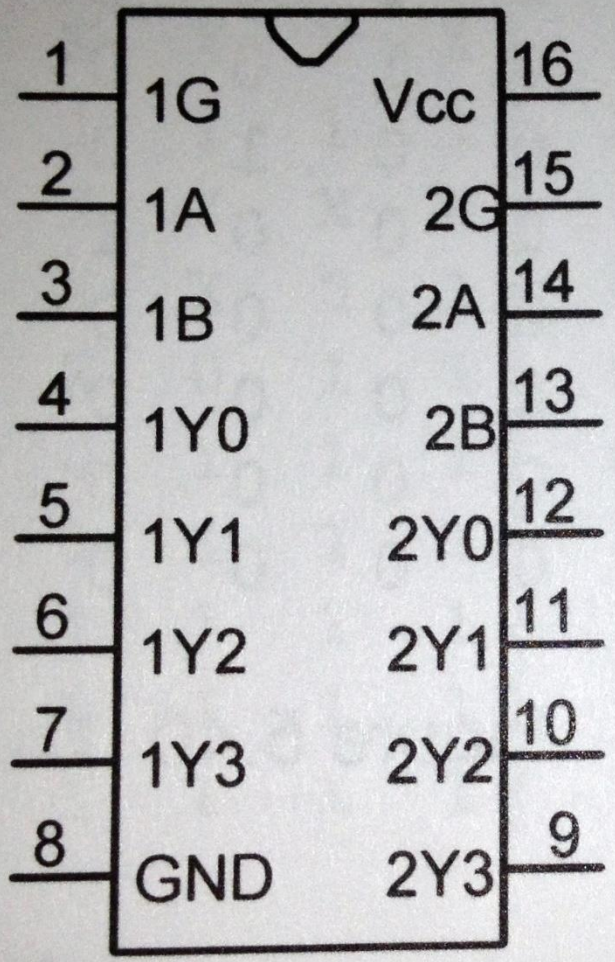


Figure: 8 bit microprocessor interfacing with 4KB RAM chip using full decoding technique

Truth table for 74LS39

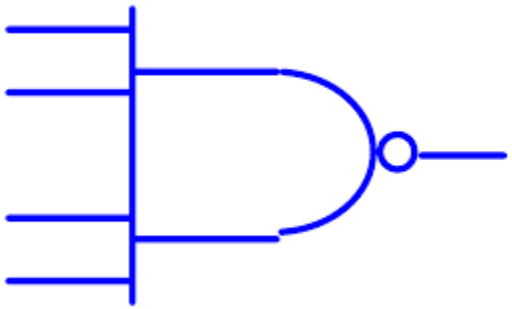


74LS139

G	B	A	Y0	Y1	Y2	Y3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

X = don't care

Truth table for NAND gate

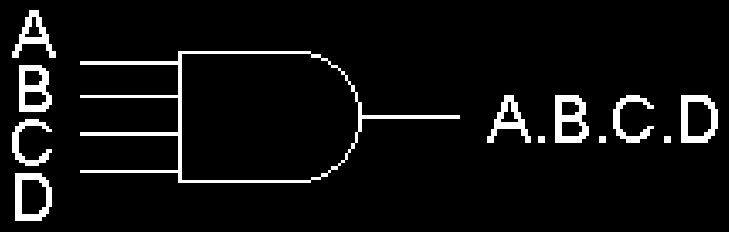


A	B	C	D	A.B.C.D
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Address map

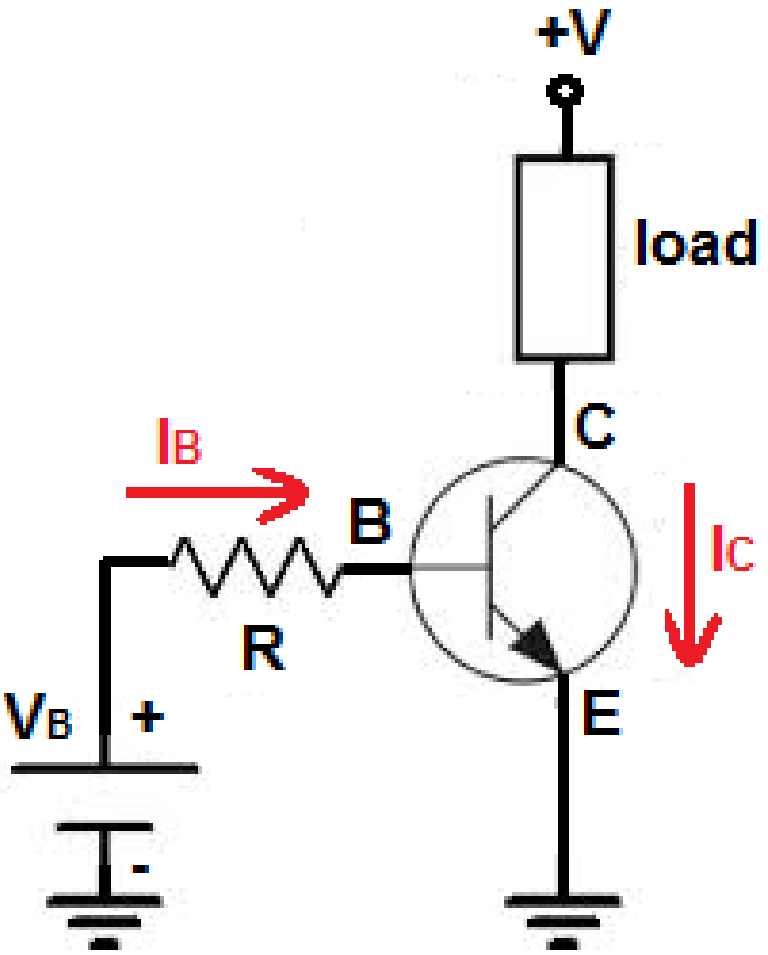
Binary Address Pattern A15 A14 A13 A12 A11 A10 A9 A7 A6 A5 A4 A3 A2 A1 A0	Device Selected	Address Assignment in Hex
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 . . . . 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1	RAM CHIP 0	0000 to 03FF
0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 . . . . 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1	RAM CHIP 1	0400 to 07FF
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 . . . . 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1	RAM CHIP 2	0800 to 0BFF
0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 . . . . 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1	RAM CHIP 3	0C00 to 0FFF

Truth table for AND gate



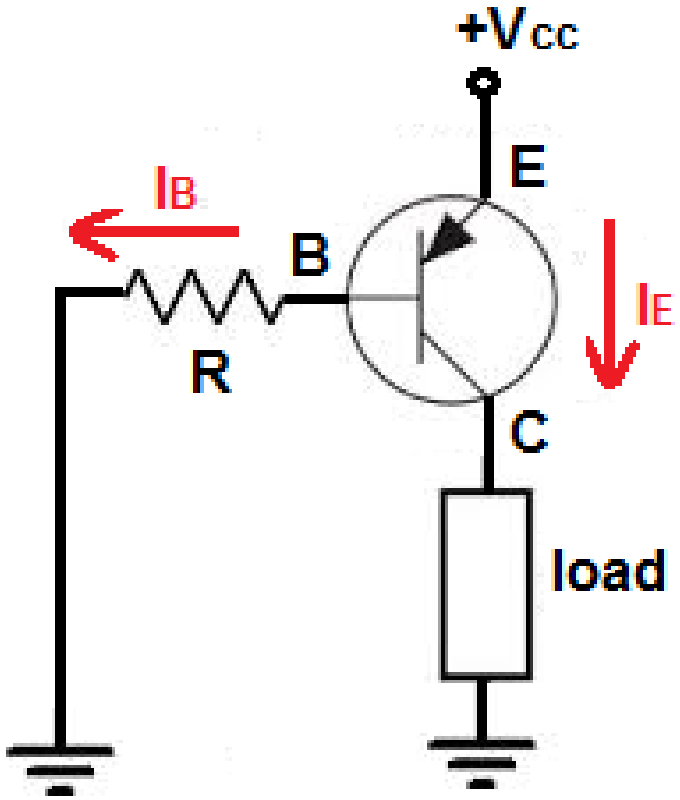
4 Input AND gate				
A	B	C	D	A.B.C.D
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Reference



In an NPN transistor, positive voltage is given to the collector terminal and current flows from the collector to the emitter, given there is sufficient base current

Reference



In a PNP transistor, positive voltage is given to the emitter terminal and current flows from the emitter to the collector, given there is sufficient negative current flow from the base