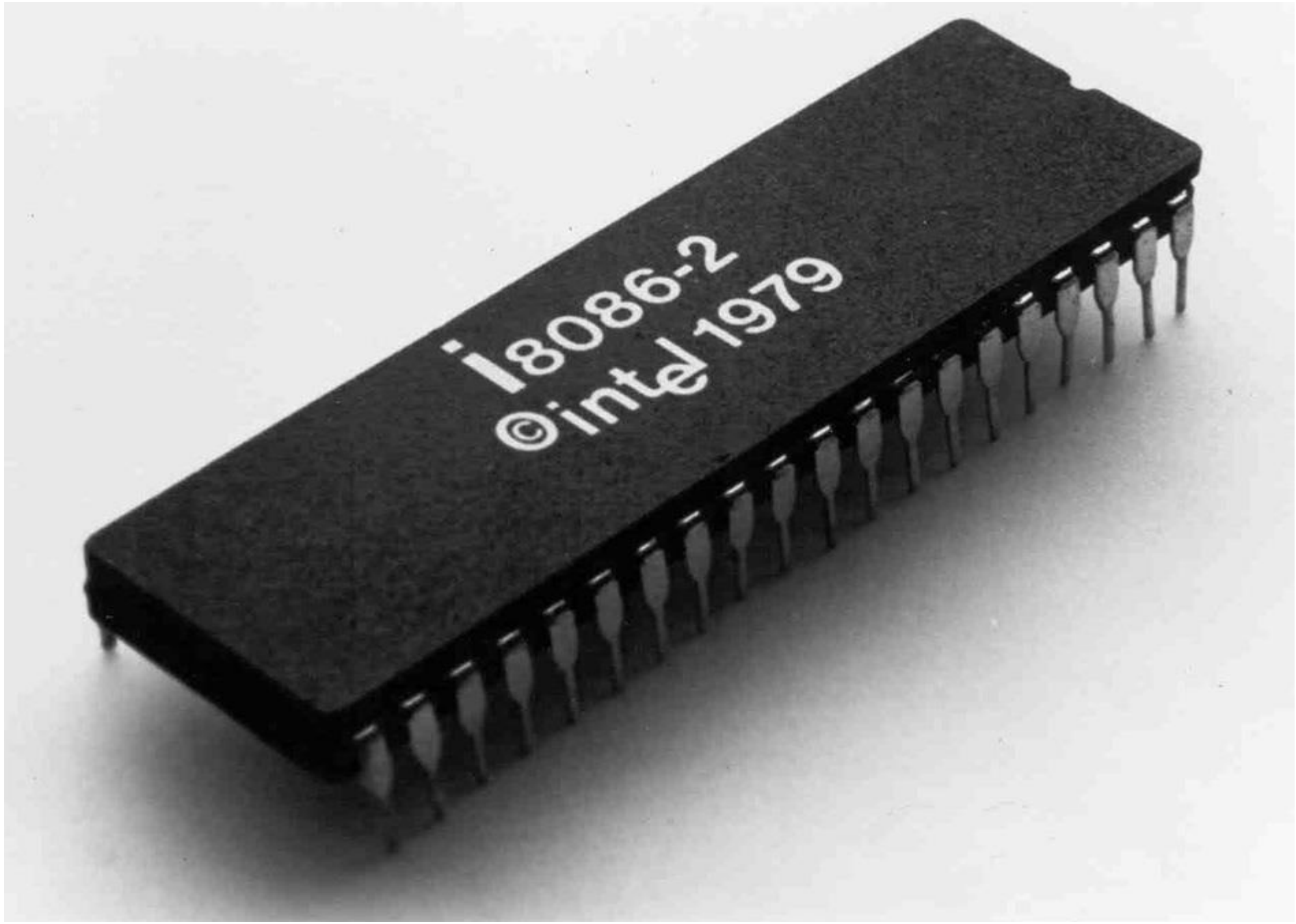
Introduction to 8086 Microprocessor (part 4)

The Intel Microprocessors 8th Edition by Barry B Brey
Section 9-1 Pin-Outs and the Pin Functions page 305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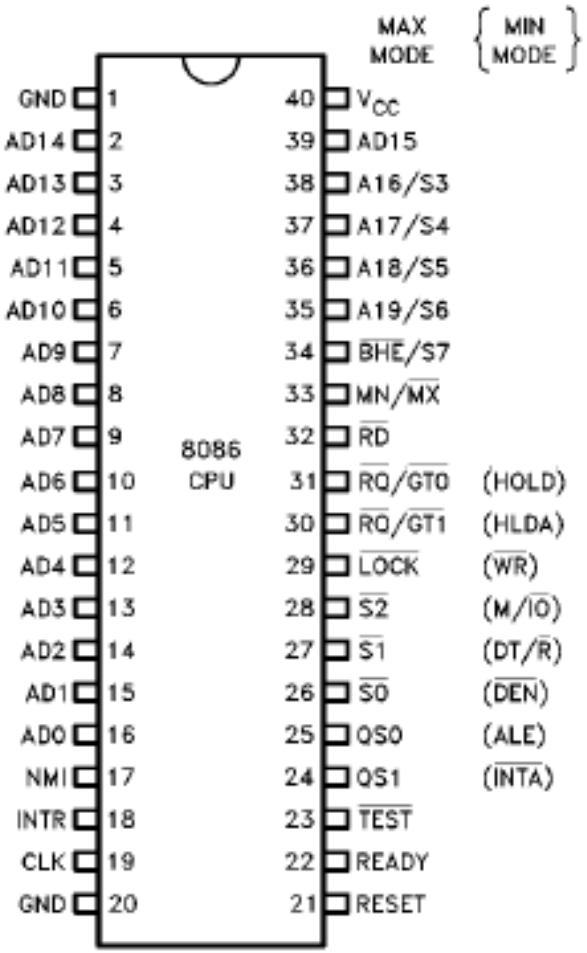
8086 Pin Diagram



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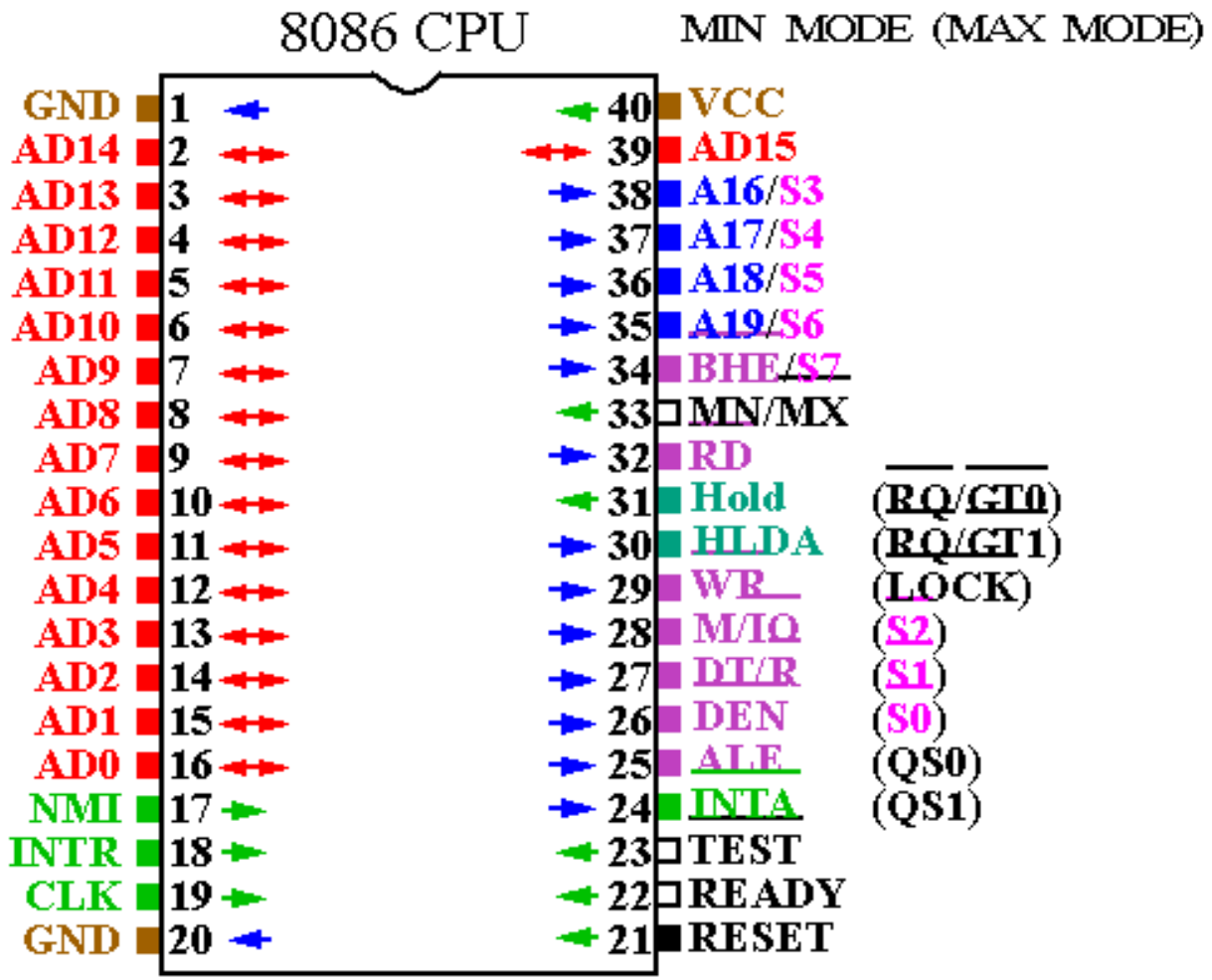


Pin Description

- AD0-AD15: Multiplexed Address/Data Bus
- RD': Low while reading from memory or port
- WR' : Low while writing to memory or port
- ALE : Address latch enable shows 8086 data bus contains address information. This address can be a memory or I/O device
- M/IO' : High during Memory operations.

  Low during I/O Port operations.
- RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution.

Pin Description

- CLK : The clock pin provides the basic timing signal to the microprocessor
- VCC: This power supply input provides a +5.0 V ±10 % signal to the microprocessor.
- GND: The ground connection is the return for the power supply. Note that the 8086 microprocessors have two pins labeled GND—both must be connected to ground for proper operation.

Pin Description

- INTR-Interrupt Request : Interrupt requests used to request a hardware interrupt.
- INTA-Interrupt Acknowledgement : It becomes active after the current instruction has completed execution.
- NMI : The non-maskable interrupt is similar to INTR except that the NMI interrupt does not check to see whether the IF flag bit is a logic 1.

Pin Description

- HOLD : The hold input requests a direct memory access (DMA). If the HOLD signal is a logic 1, the microprocessor release the buses for external use. If the HOLD pin is a logic 0, the microprocessor executes software normally.

- HLDA : Hold acknowledge indicates that the 8086 has entered the hold state

- MN/MX’
  In Minimum mode, the 8086 processor works in a single processor environment.
  Maximum mode is designed to be used when a co-processor exists in the system.

If minimum mode is selected, the MN/MX’ pin must be connected directly to +5.0 V.

Pin Description

- DT/R’ : The data transmit/receive signal shows that the microprocessor data bus is transmitting (DT/R’) or receiving (DT/R’) data. This signal is used to enable external data bus buffers.
- DEN’: Data bus enable activates external data bus buffers.
- BHE’/S7: The bus high enable pin is 0 used to enable the most-significant data bus bits (D15–D8) and 1 to enable data bus bits (D7–D0) during a read or a write operation. The state of S7 is always a logic 1.
- READY: The READY input is controlled to insert wait states into the timing of the microprocessor. If the READY pin is placed at a logic 0 level, the micro-processor enters into wait states and remains idle. If the READY pin is placed at a logic 1 level, it has no effect on the operation of the microprocessor.

Pin Description

- A19/S6–A16/S3 : The address/status bus bits are multiplexed to provide address signals A19–A16 and also status bits S6–S3.

✓During the first clock period of a bus cycle, the entire 20-bit address is available on these lines. During all other clock cycles for memory and I/O operations, AD15-AD0 contains the 16-bit data, and S3, S4, S5, and S6 become status lines.

✓After the first clock cycle of an instruction execution, the A17/S4 and A16/S3 pins specify which segment register generates the segment portion of the 8086 address. Thus, by decoding these lines and using the decoder selects the memory chips.

✓S5 reflects the contents of the IF flag. S6 is always held at 0 and indicates that an 8086 is controlling the system bus.

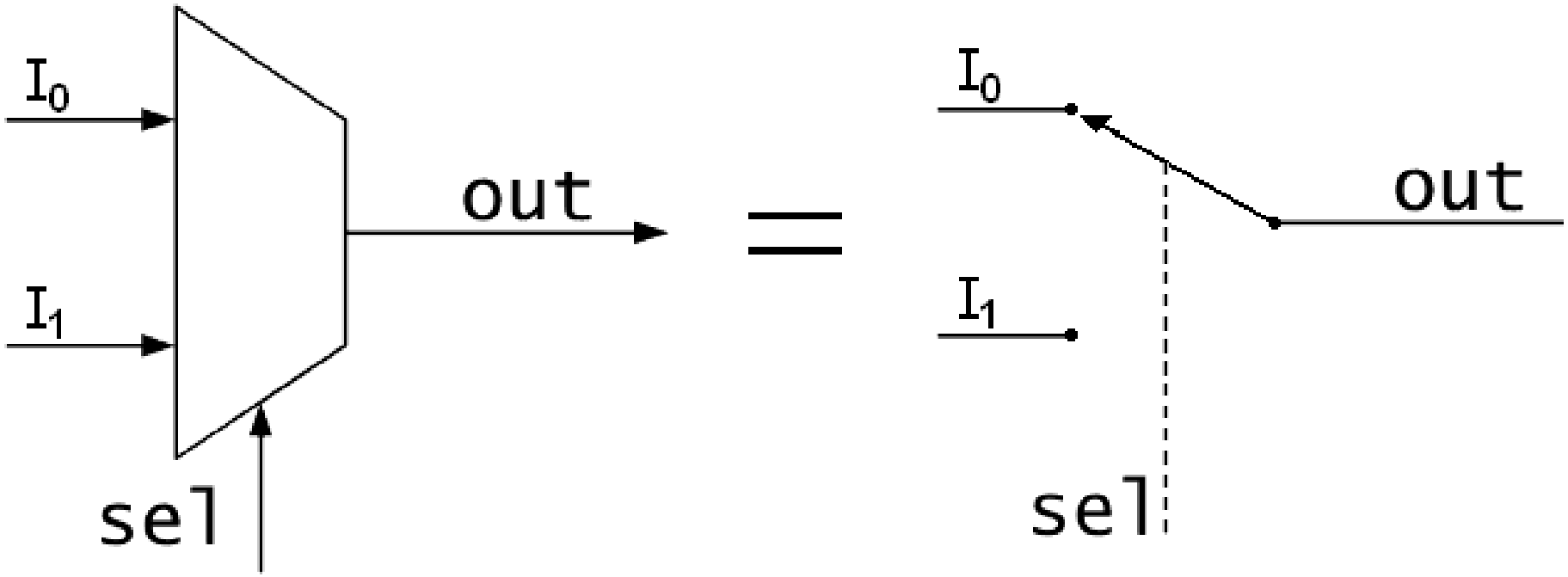
Pin Description

S3 and S4 lines are decoded as follows:

A17/S4	A16/S3	Function
0	0	Extra segment access
0	1	Stack segment access
1	0	Code segment access
1	1	Data segment access

Reference (1)

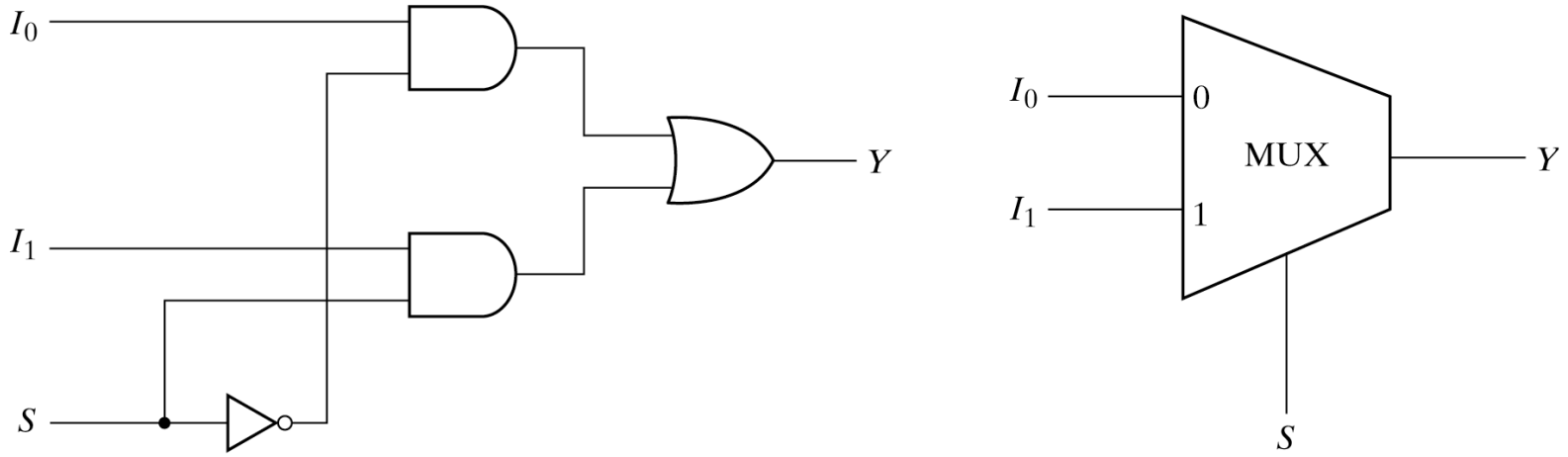
The address/data bus on the 8086 is multiplexed (shared) to reduce the number of pins required for the 8086/8088 microprocessor integrated circuit. Unfortunately, this burdens the hardware designer with the task of extracting or demultiplexing information from these multiplexed pins.



Reference (2): Multiplexer (Data Selector)

- Multiplexing means transmitting a large number of information units over a smaller number of channels or lines.
- A digital multiplexer is a circuit that selects binary information from one of many input lines and directs it to a single output lines.
- The selection of a particular input line is controlled by a set of selection lines.
  - Have 2^n input lines and n selection lines whose bit combinations determine which input is selected.

Reference (3): Multiplexer



(a) Logic diagram

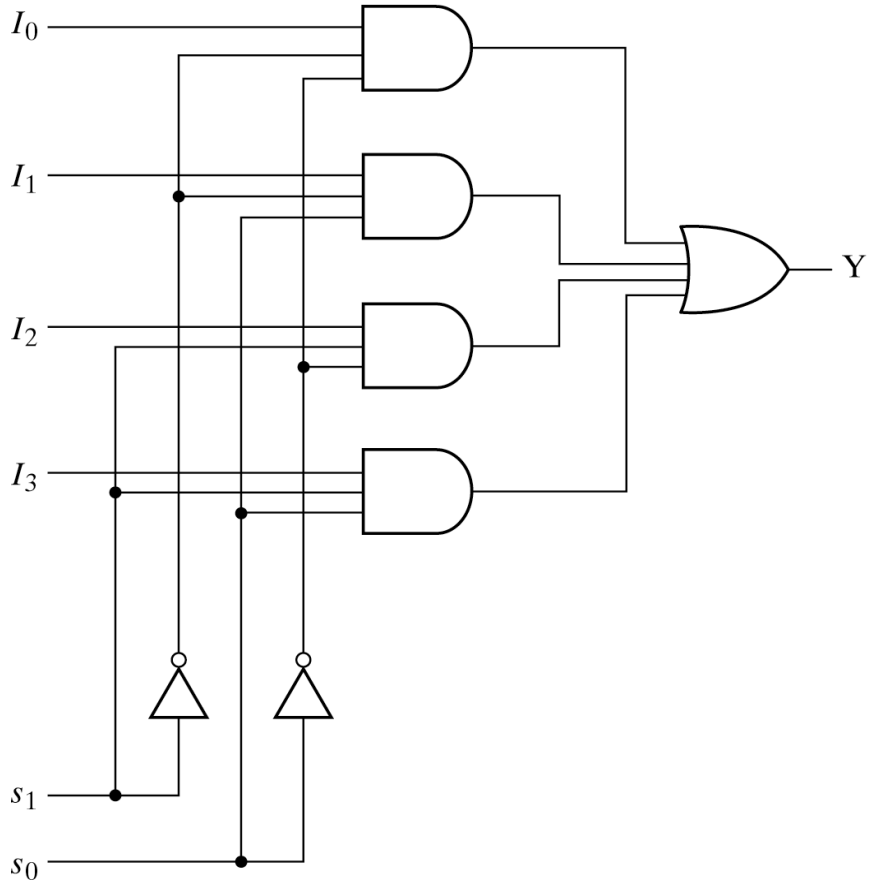
(b) Block diagram

Fig. 4-24 2-to-1-Line Multiplexer

Reference (4) : 4-to-1-Line Multiplexer

- The combinations of S_0 and S_1 control each AND gates
- Part of the multiplexer resembles a decoder
  - Selection lines s_1 and s_0 are decoded to select a particular AND gate.
- To construct a multiplexer:
  - Start with an n-to-2^n decoder
  - Add 2^n input lines, one to each AND gate
  - The outputs of the AND gates are applied to a single OR gate.

Reference (5) : 4-to-1-Line Multiplexer



(a) Logic diagram

s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

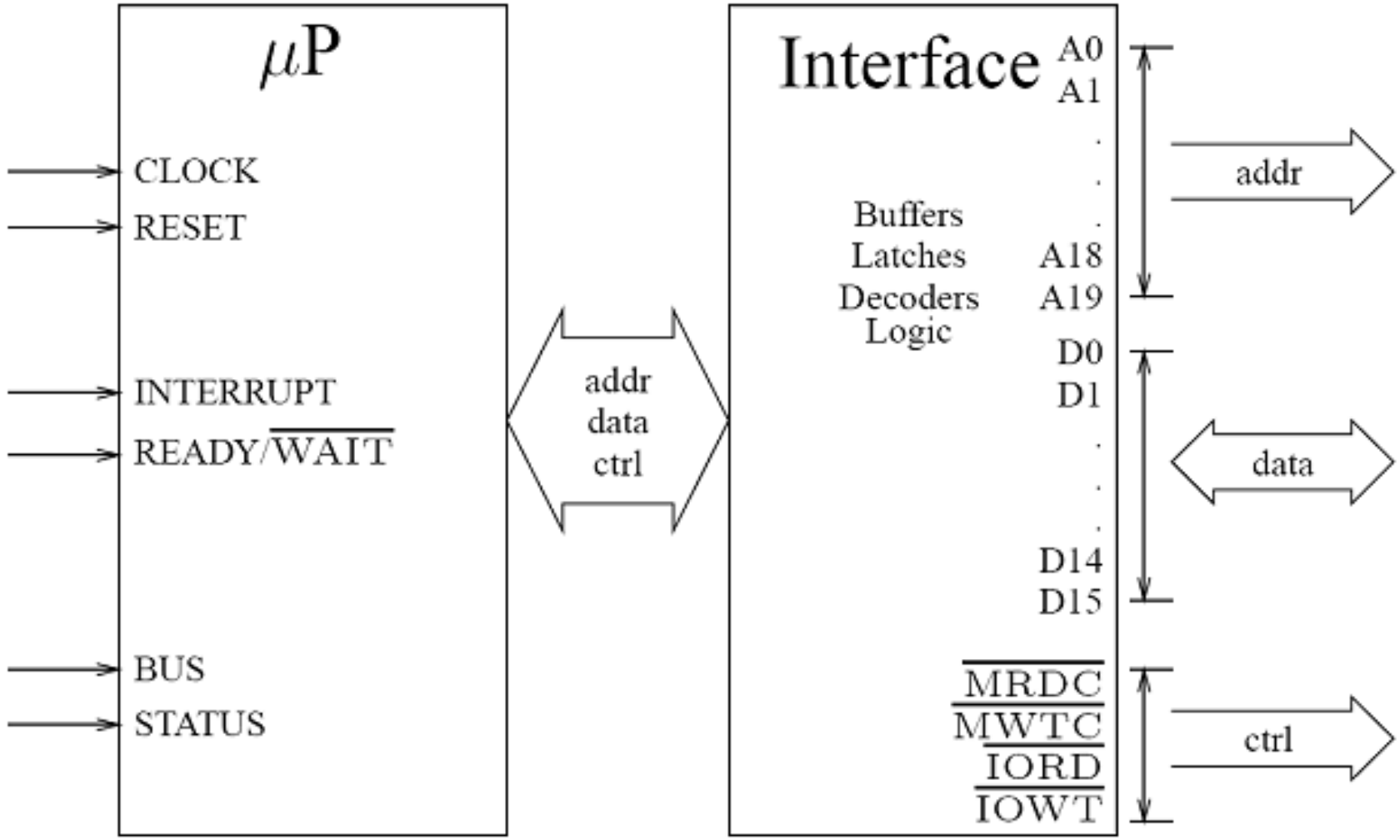
Fig. 4-25 4-to-1-Line Multiplexer

- The function table lists the input-to-output path for each possible bit combination of the selection lines.

Reference (6): Multiplexer

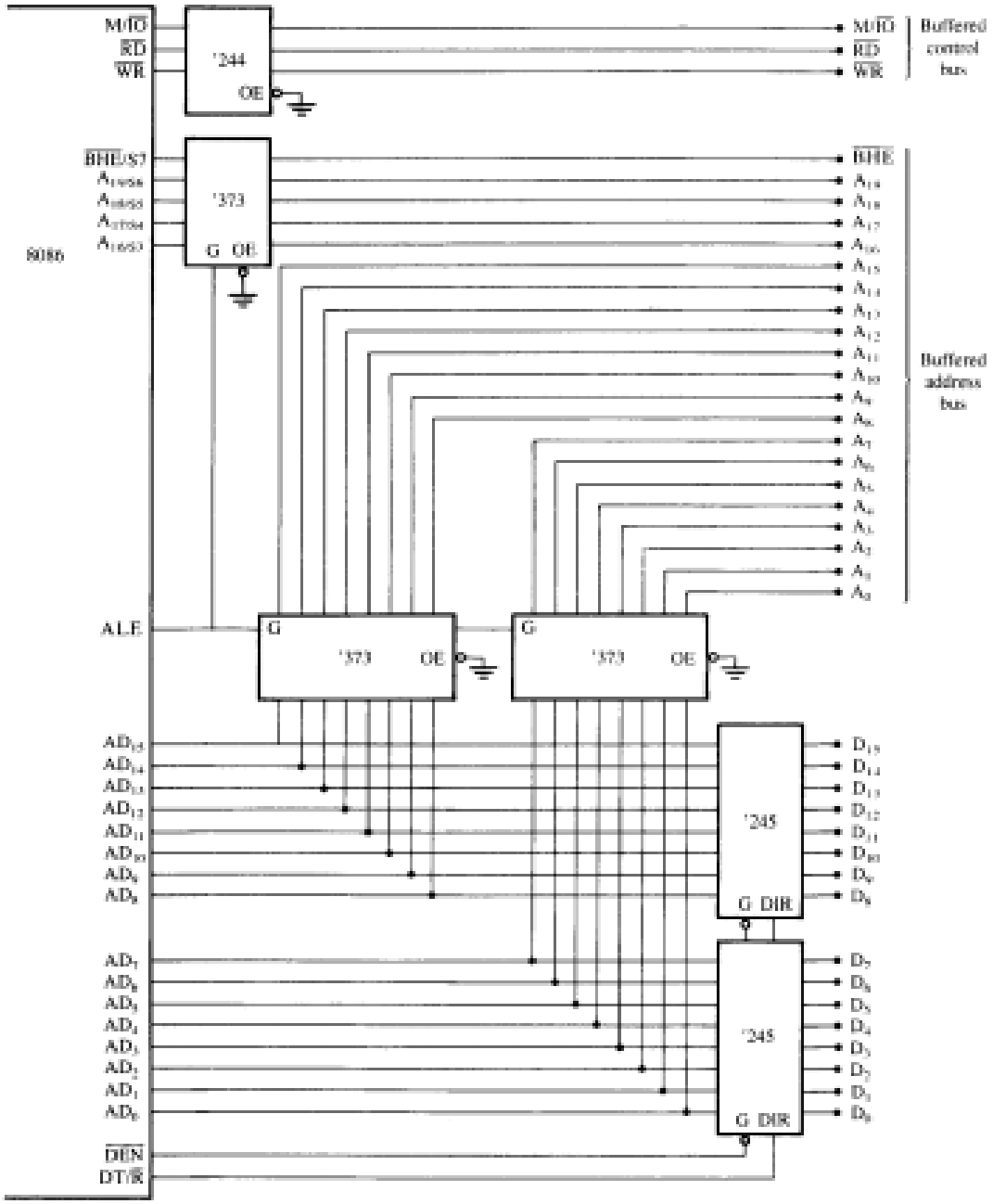
- The size of a multiplexer is specified by the number 2^n of its input lines and the single output line.
  - It is then implied that it also contains n selection lines.
- As in decoders, multiplexer ICs may have an enable input to control the operation of the unit.

Reference (7)



Abstract diagram showing data flow in/out of μP

BUS Buffering and Latching



Reference (8)

The 8086 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8086-based systems

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Reference (9)

A buffer allows a signal to drive more inputs than it would by itself, or provides input protection / amplification. For the 8086, it's used in the output sense, allowing internal signals to be made robust to drive external devices