Programming SAP-1 part 2

SAP1 Malvino.pdf

- The instruction format of SAP-1 Computer is

  (XXXX) (XXXX)

- the first four bits make the opcode while the last four bits make the operand(address).
- SAP-1 instruction set consists of following instructions

Mnemonic	Operation	OPCODE
LDA	Load addressed memory contents into accumulator	0000
ADD	Add addressed memory contents to accumulator	0001
SUB	Subtract addressed memory contents from accumulator	0010
OUT	Load accumulator data into output register	1110
HLT	Stop processing	1111

Exercise 1

- Q: Translate the program into SAP1 machine language.
- Program:

Address	Instruction
0H	LDA 9H
1H	ADD AH
2H	ADD BH
3H	SUB CH
4H	OUT
5H	HLT

Answer:

- Machine language:

Address	Instruction
0000	0000 1001
0001	0001 1010
0010	0001 1011
0011	0010 1100
0100	1110 XXXX
0101	1111 XXXX

Exercise 2

- Q: Write down the program (assembly language and machine language) to get the result in SAP1 for the following arithmetical expression.

16 + 20 + 24 -32 (decimal)

Answer:

- Assembly language:

Address	Contents
0H	LDA 9H
1H	ADD AH
2H	ADD BH
3H	SUB CH
4H	OUT
5H	HLT
6H	XX
7H	XX
8H	XX
9H	10H
AH	14H
BH	18H
CH	20H

Answer:

- Machine language:

Address	Contents
0000	0000 1001
0001	0001 1010
0010	0001 1011
0011	0010 1100
0100	1110 XXXX
0101	1111 XXXX
0110	XXXX XXXX
0111	XXXX XXXX
1000	XXXX XXXX
1001	0001 0000
1010	0001 0100
1011	0001 1000
1100	0010 0000

The program is stored in the low-memory. And data is stored in the high-memory.

Machine cycle and Instruction cycle

SAP1 has six T-states (three fetch and three execute cycles) reserved for each instruction. Not all instructions require all the six T-states for execution. The unused T- state is marked as No Operation (NOP) cycle. Each T-state is called a machine cycle for SAP1. A ring counter is used to generate a T-state at every falling edge of clock pulse. The ring counter output is reset after the 6th T-state.

FETCH CYCLE – T1, T2, T3 machine cycle

EXECUTE CYCLE - T4, T5, T6 machine cycle

Ring counter

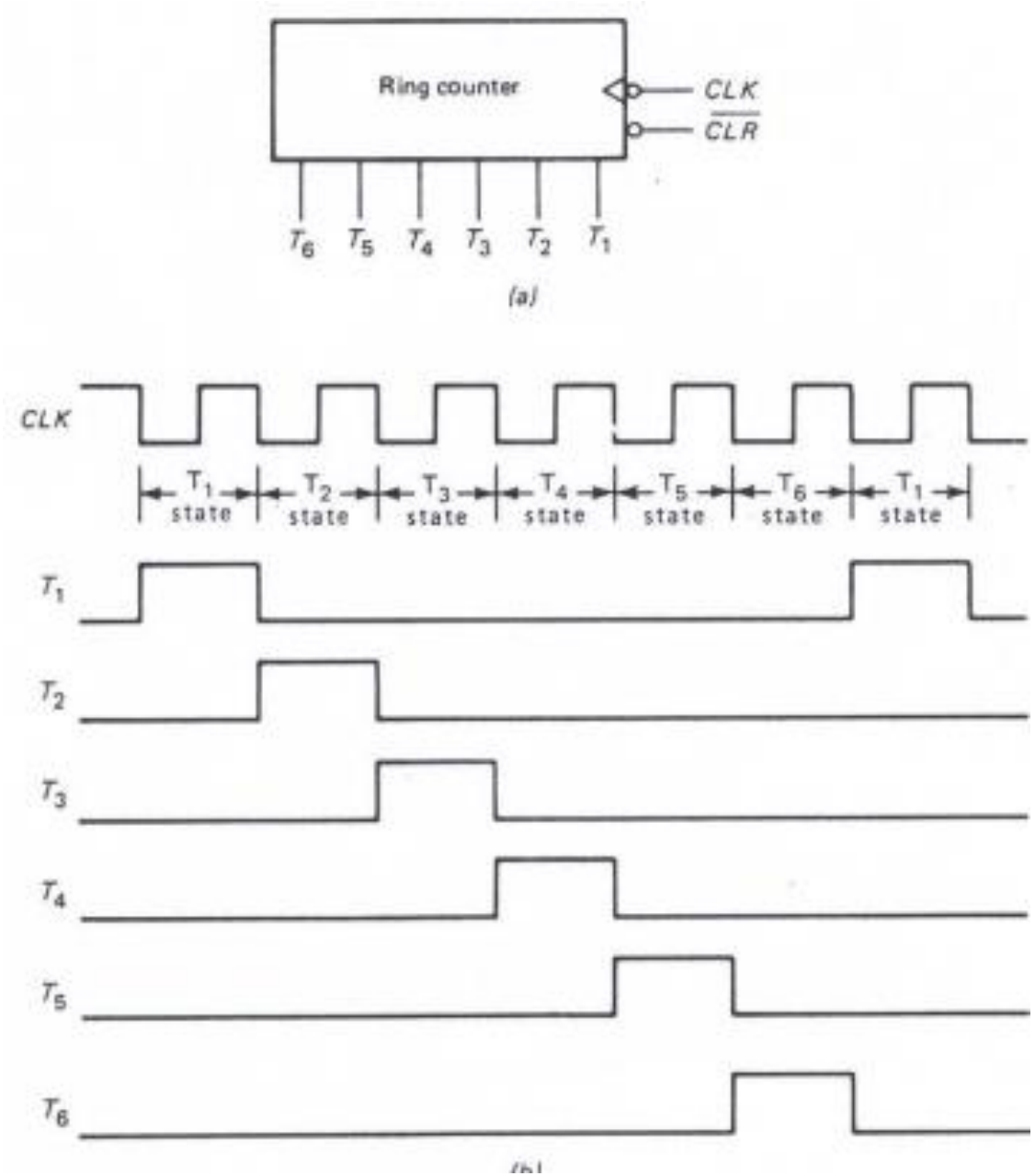


Figure: a. Ring counter symbol
b. Clock and timing signals

Ring counter

Ring Counter

Earlier, we discussed the SAP-1 ring counter (see Fig. 8-16 for the schematic diagram). Figure 10-2*a* symbolizes the ring counter, which has an output of

$$\mathbf{T} = T_6T_5T_4T_3T_2T_1$$

At the beginning of a computer run, the ring word is

$$\mathbf{T} = 000001$$

Successive clock pulses produce ring words of

$$\mathbf{T} = 000010$$
$$\mathbf{T} = 000100$$
$$\mathbf{T} = 001000$$
$$\mathbf{T} = 010000$$
$$\mathbf{T} = 100000$$

Then, the ring counter resets to 000001, and the cycle repeats. Each ring word represents one *T* state.

Machine cycle and Instruction cycle

SAP1 has six T-states (three fetch and three execute cycles) reserved for each instruction. Not all instructions require all the six T-states for execution. The unused T- state is marked as No Operation (NOP) cycle. Each T-state is called a machine cycle for SAP1. A ring counter is used to generate a T-state at every falling edge of clock pulse. The ring counter output is reset after the 6th T-state.

FETCH CYCLE

FETCH CYCLE – T1, T2, T3 machine cycle

T1 (address state),

T2 (Increment state),

T3 machine cycle (Memory state)

EXECUTE CYCLE

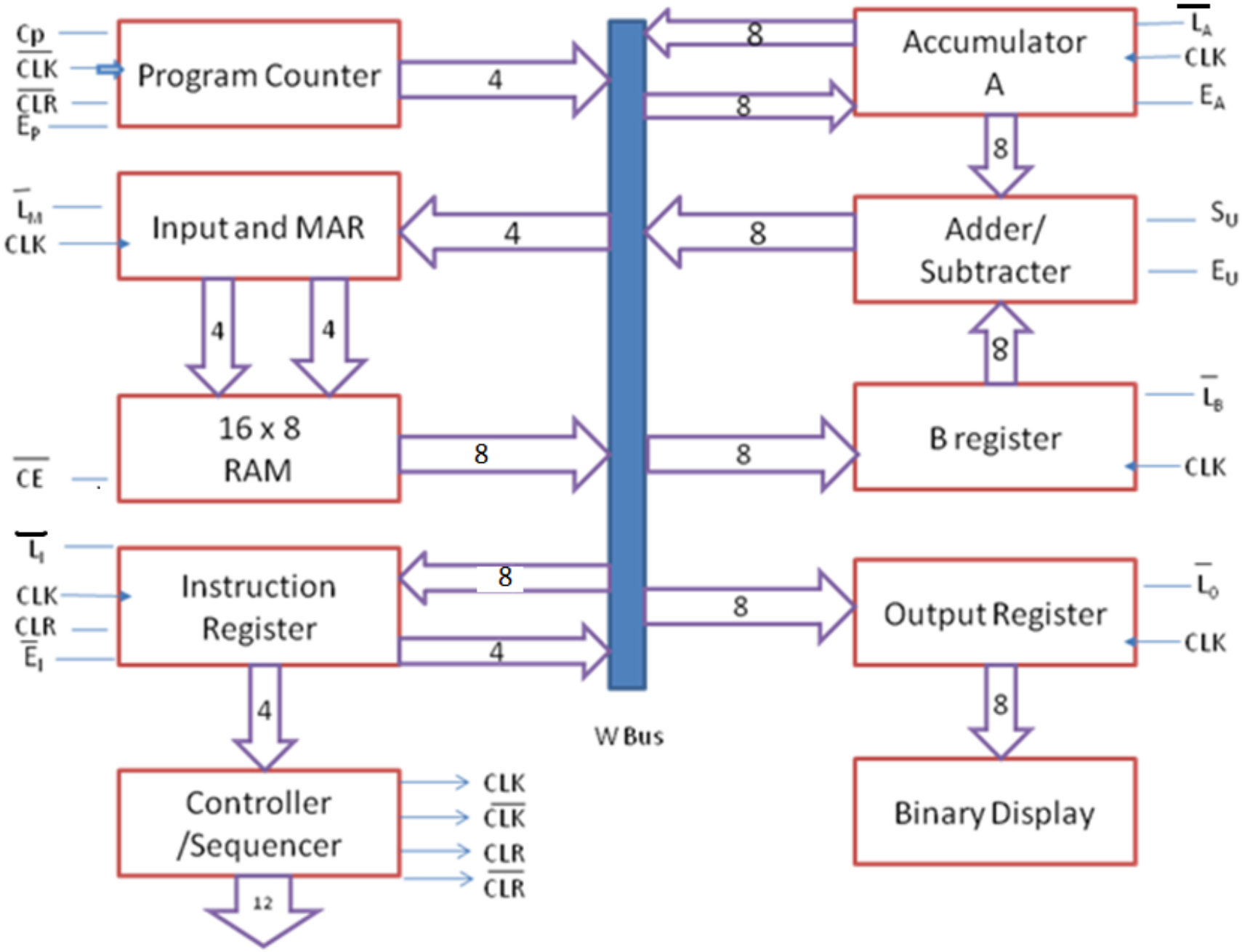
EXECUTE CYCLE - T4, T5, T6 machine cycle

The next three states (T4, T5, T6) are the execution cycle of SAP1. The register transfers during the execution cycle depend on the particular instruction being executed. For example, LDA 9H requiers different register transfer than ADD BH.

Instruction routine

- LDA routine
- ADD routine
- SUB routine
- OUT routine
- HLT routine

T1, T2, T3 machine cycle
is same for all instruction



Block diagram of Simple-As-Possible (SAP)-1 Architecture

$$CON = C_P\, E_P\, L'_M\, CE' \quad L'_I\, E'_I\, L'_A\, E_A \quad S_U\, E_U\, L'_B\, L'_O$$