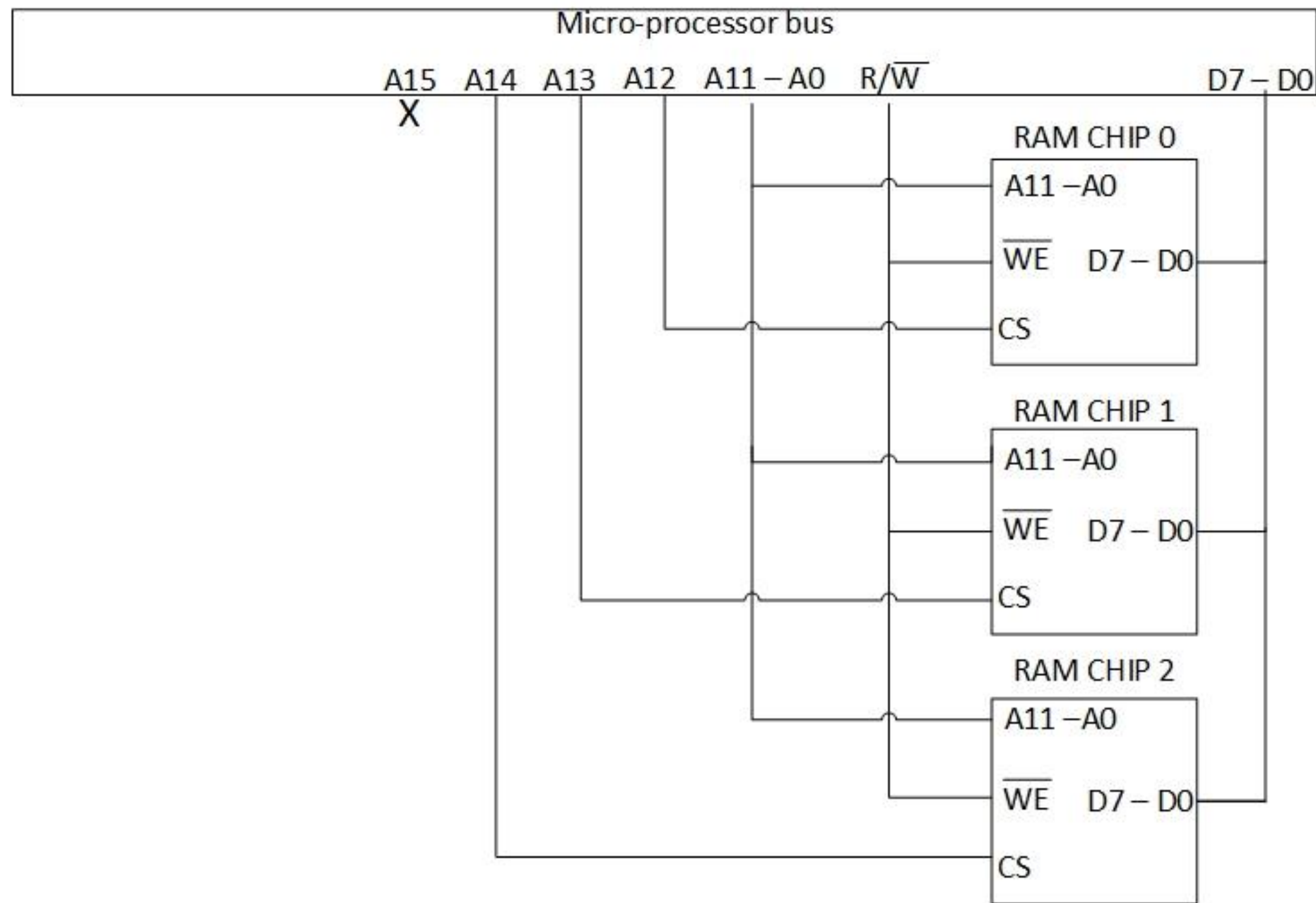# 8086 and Memory Interfacing Part 2

Draw the diagram of 8-bit microprocessor with 16 bit address bus interfaced with 9KB RAM using linear decoding method. Each RAM chip has 12 bit address bus and 8 bit data bus. Also provide the corresponding address map for each RAM chip.

Micro-processor bus

A15 A14 A13 A12 A11 − A0 R/W̄   D7 − D0

X

RAM CHIP 0

A11 − A0

W̄Ē   D7 − D0

CS

RAM CHIP 1

A11 − A0

W̄Ē   D7 − D0

CS

RAM CHIP 2

A11 − A0

W̄Ē   D7 − D0

CS

Address A15-A14-A13-A12-A11-A10-A9-A8-A7-A6-A5-A4-A3-A2-A1-A0	RAM CHIP
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	Ram chip 0
0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	Ram chip 1
0 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1	
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Ram chip 2
0 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1	

Draw the diagram of 8-bit microprocessor with 16 bit address bus interfaced with 7KB RAM using the full decoding technique. Each RAM chip has 10 bit address bus and 8 bit data bus. Also provide the corresponding address map for each RAM chip.