

# Introduction to 8086 Microprocessor (part 1)

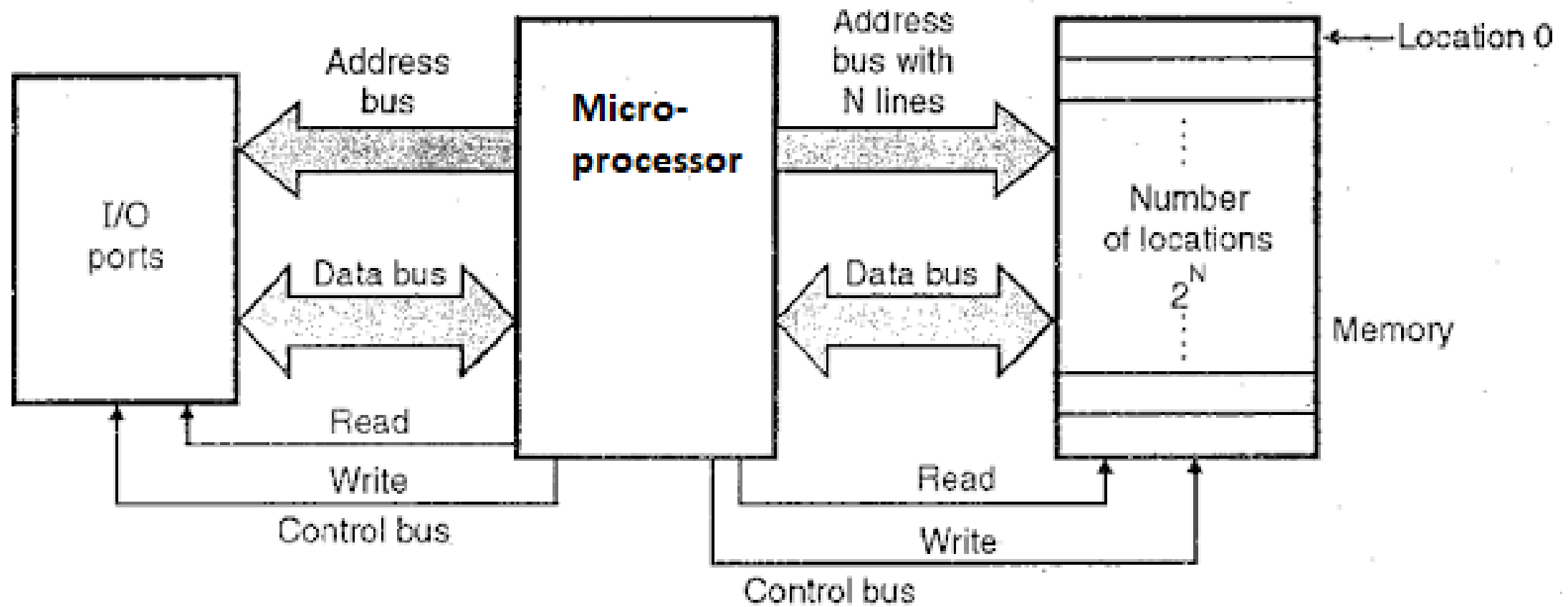
Microprocessors and microcomputer-based system design

Mohamad Rafiquzzaman

>Chapter 3 section 3.1, 3.2, 3.3

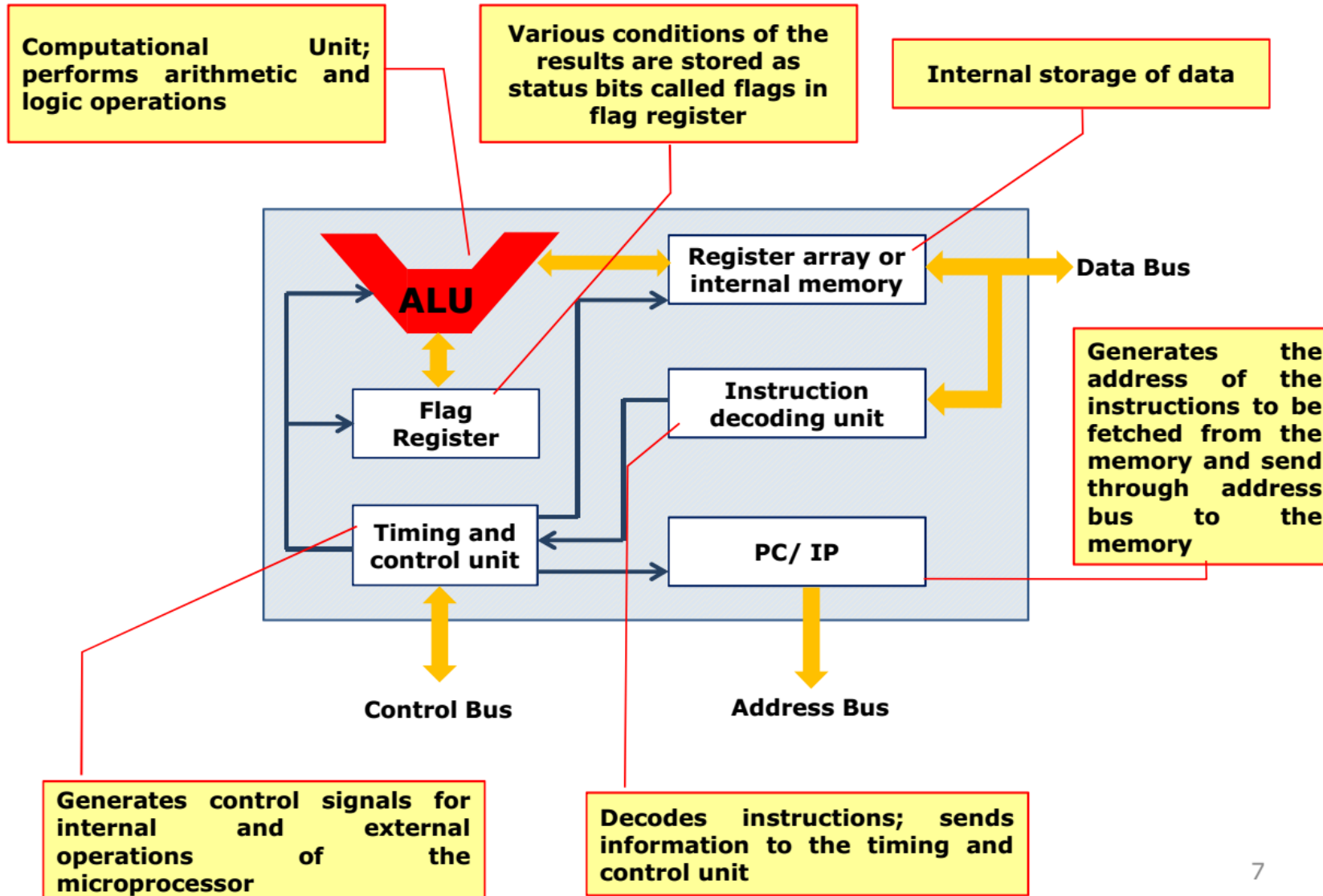
Assembly language programming Ytha Yu

> Chapter 3 section 3.2



Micro-processor interfacing with memory device (ROM/RAM) and I/O device (keyboard/printer)

## Functional blocks inside micro-processor



# Microprocessors Family

8085 : 8-bit micro-processor

## 8086 Family:

8086: First 16-bit processor

80186: 16-bit 8086 with peripheral devices

80286: Advanced version of 8086 used for multitasking.

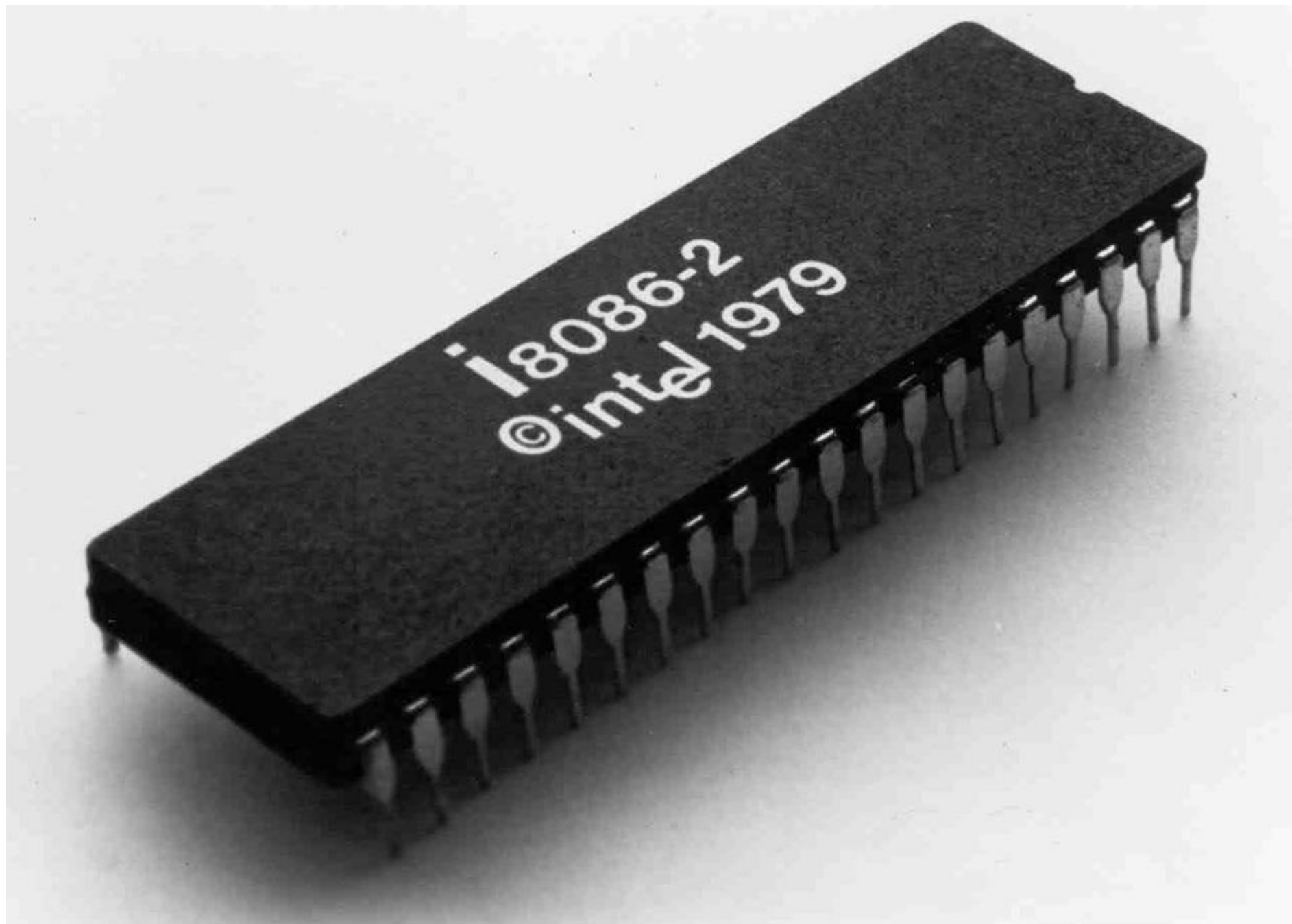
80386: 32-bit processor architecture

80486: 32-bit processor architecture with floating point processor(80387) integrated into the chip.

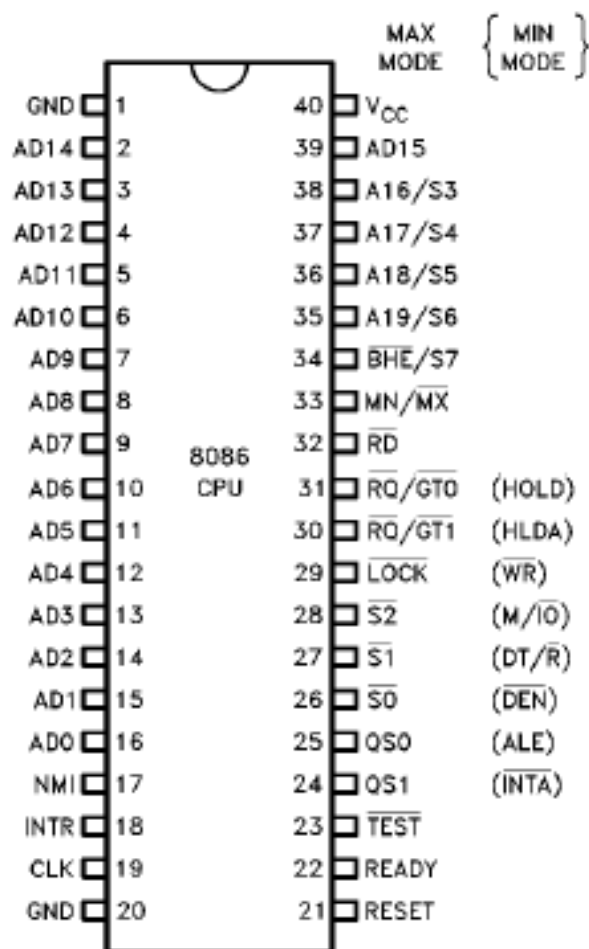
## 8088 Family:

8088: Same as 8086 but 8-bit databus.

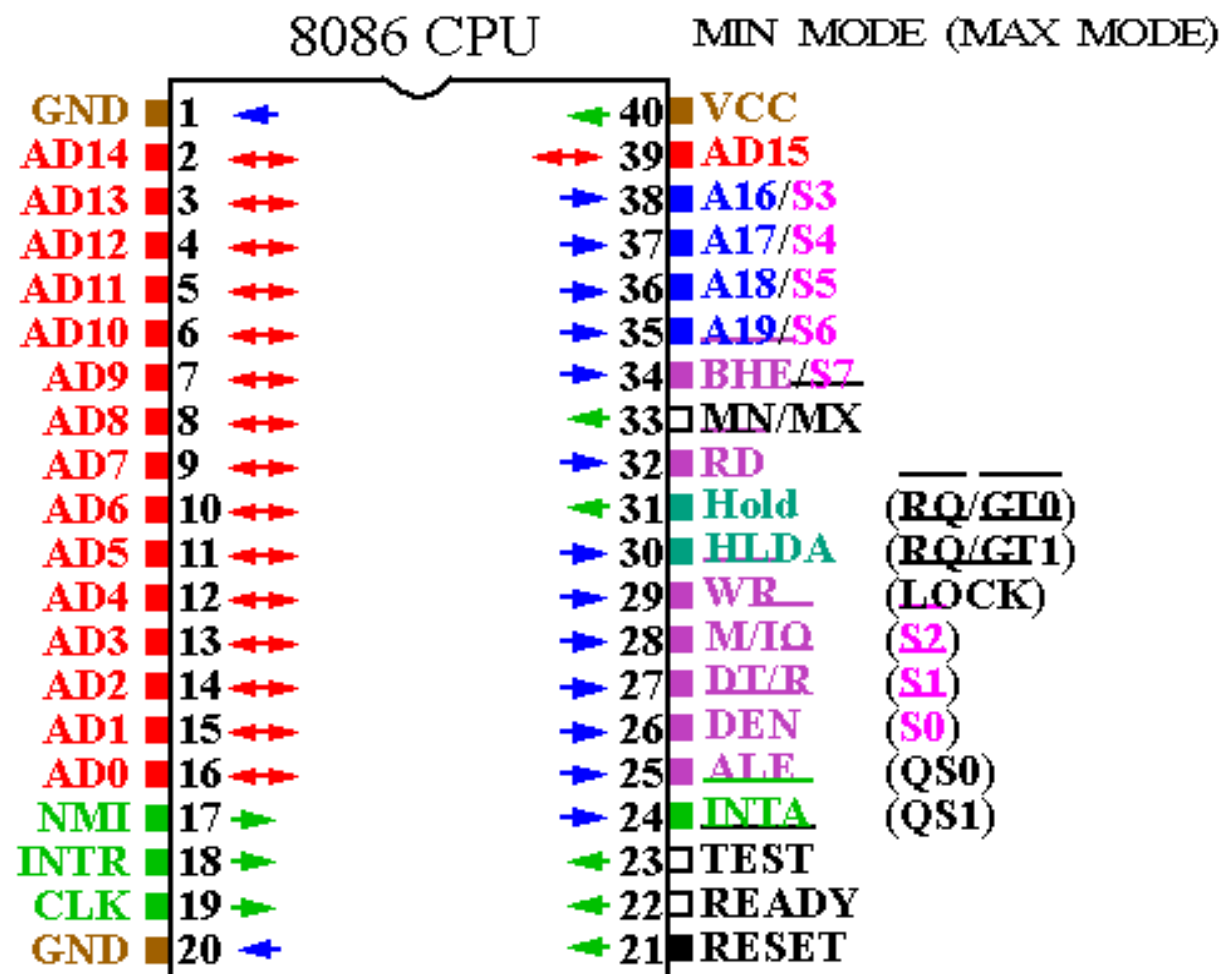
80188: 8088 with peripheral devices.



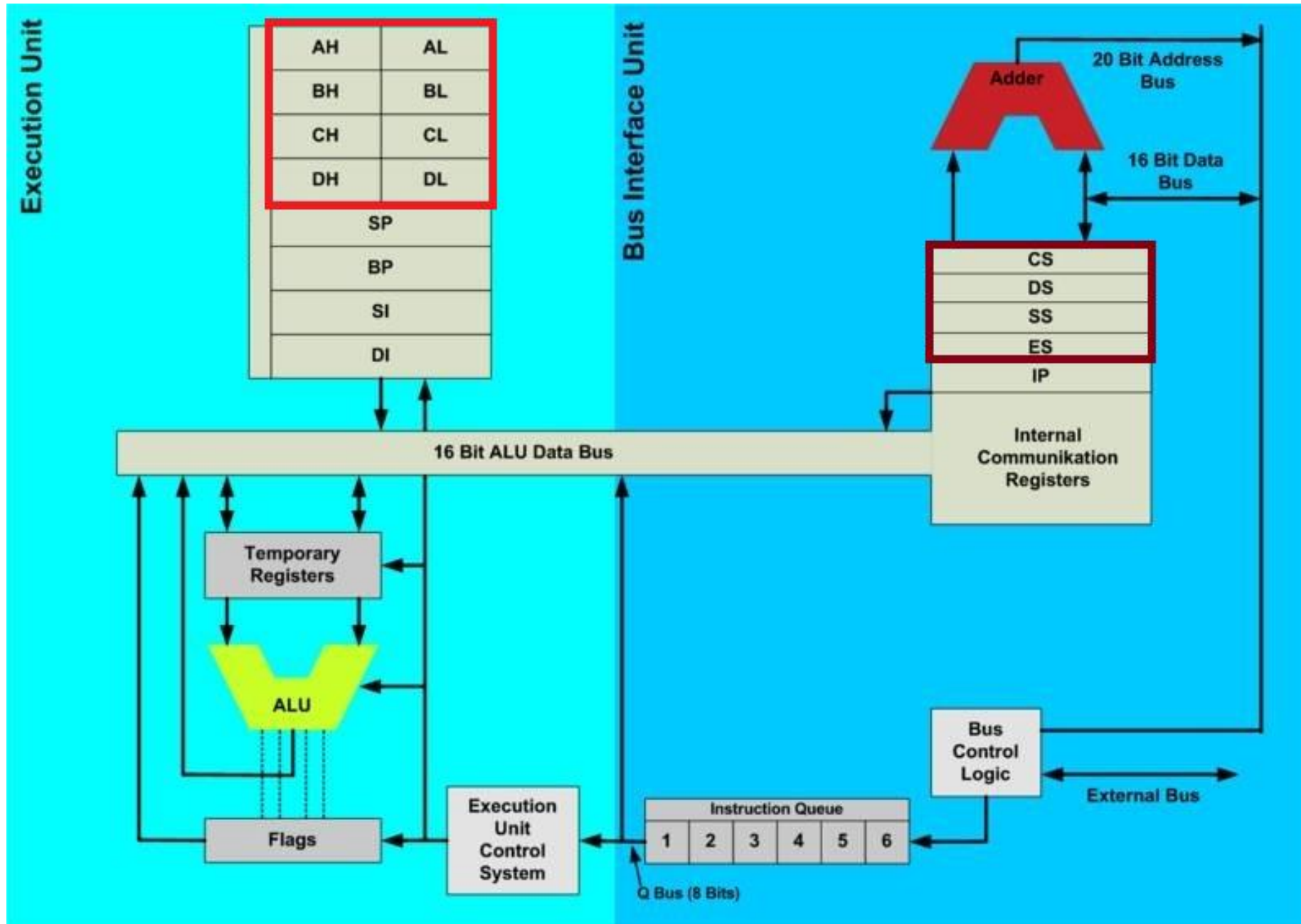
# 8086 Pin Diagram



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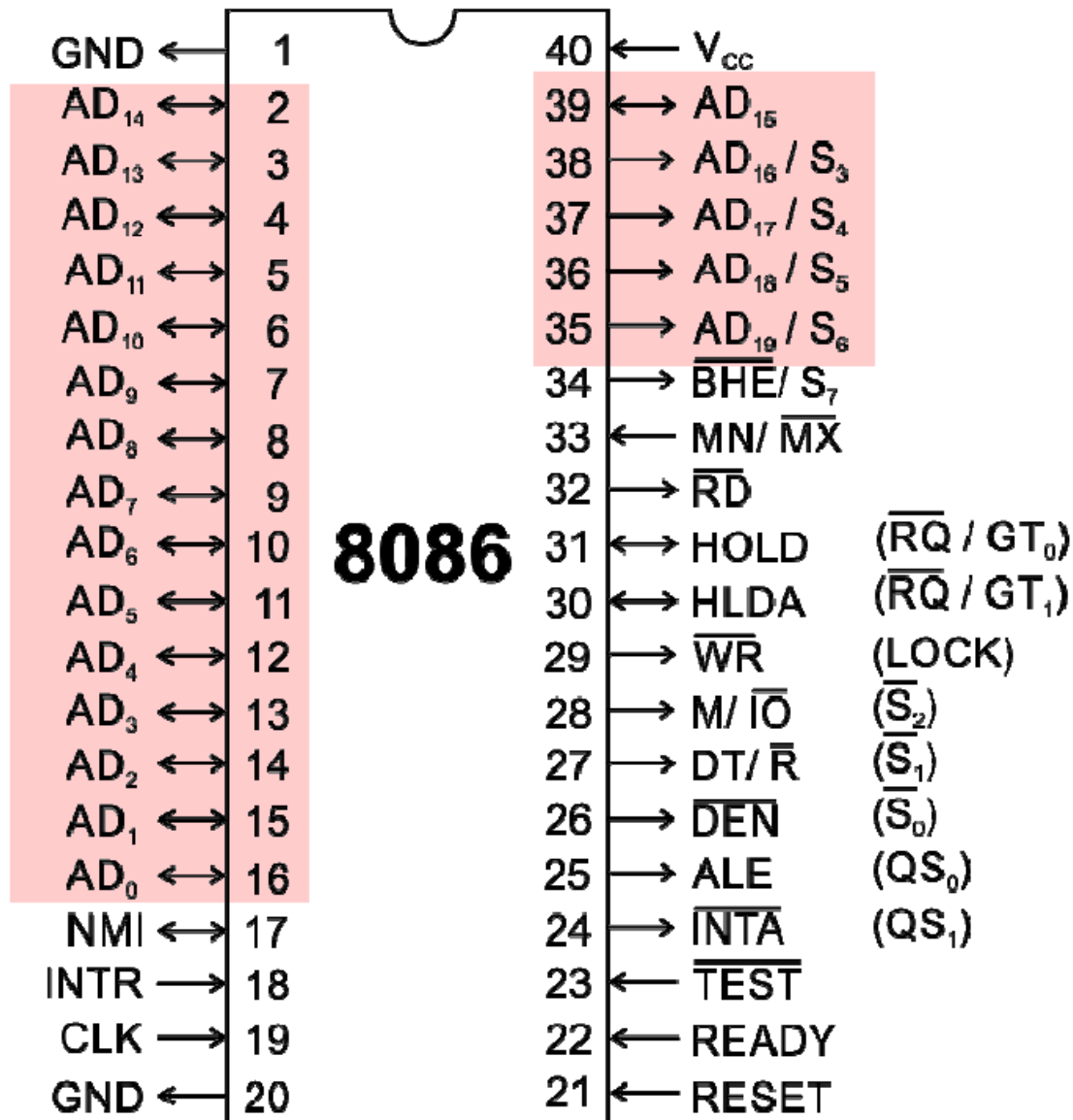
# 8086 Internal Architecture



# 8086 Features

- Operating Clock rates are 5, 8, 10 MHz.
- 16-bit Arithmetic Logic Unit
- 16-bit data bus
- 20-bit address bus





## AD<sub>0</sub>-AD<sub>15</sub> (Bidirectional)

### Address/Data bus

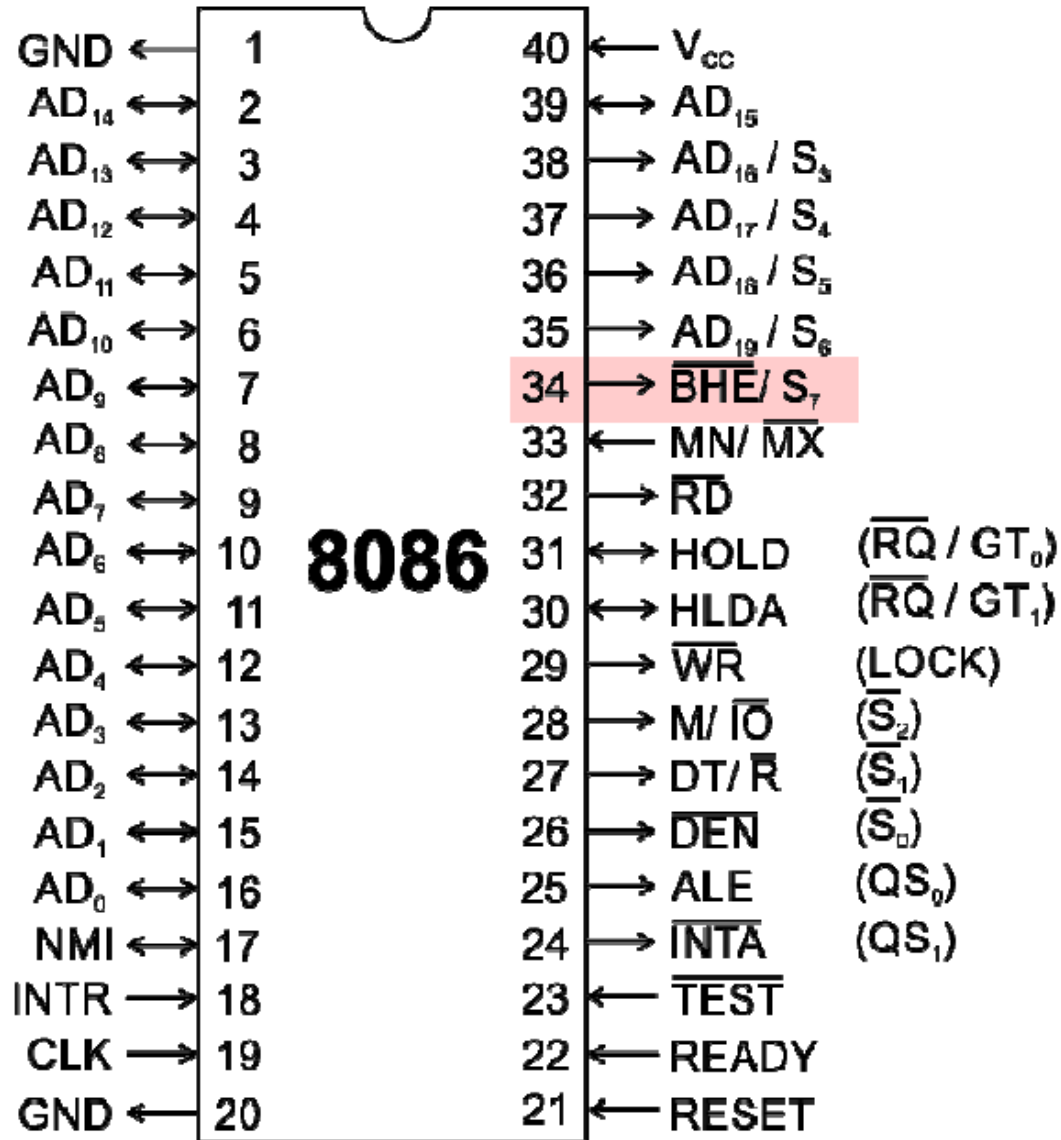
Low order address bus; these are multiplexed with data.

When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A<sub>0</sub>-A<sub>15</sub>.

When data are transmitted over AD lines the symbol D is used in place of AD, for example D<sub>0</sub>-D<sub>7</sub>, D<sub>8</sub>-D<sub>15</sub> or D<sub>0</sub>-D<sub>15</sub>.

### A<sub>16</sub>/S<sub>3</sub>, A<sub>17</sub>/S<sub>4</sub>, A<sub>18</sub>/S<sub>5</sub>, A<sub>19</sub>/S<sub>6</sub>

High order address bus. These are multiplexed with status signals



## BHE (Active Low)/S<sub>7</sub> (Output)

### Bus High Enable/Status

It is used to enable data onto the most significant half of data bus, D<sub>8</sub>-D<sub>15</sub>. 8-bit device connected to upper half of the data bus use BHE (Active Low) signal. It is multiplexed with status signal S<sub>7</sub>.

## MN/ MX

### MINIMUM / MAXIMUM

This pin signal indicates what mode the processor is to operate in.

## RD (Read) (Active Low)

The signal is used for read operation.  
It is an output signal.  
It is active when low.

# Intel 8086 known as 16 bit microprocessor

The bit size of a processor is normally defined by its ALU width, which equates to its main working register width. (e.g.: AX, BX, CX, DX).

8086 processor is capable to process the 16 bit data together. It means a data with 16 bit can be processed and can be sent to processor in single oscillation.

# Memory capacity/size

Address 20 bit

000000000000000000000000

000000000000000000000001

000000000000000000000010

000000000000000000000011

000000000000000000000100

Data 8 bit

1st data

2nd data

3rd data

4th data

5th data

Memory

Data bus 16 bit

## 8086 capacity/size

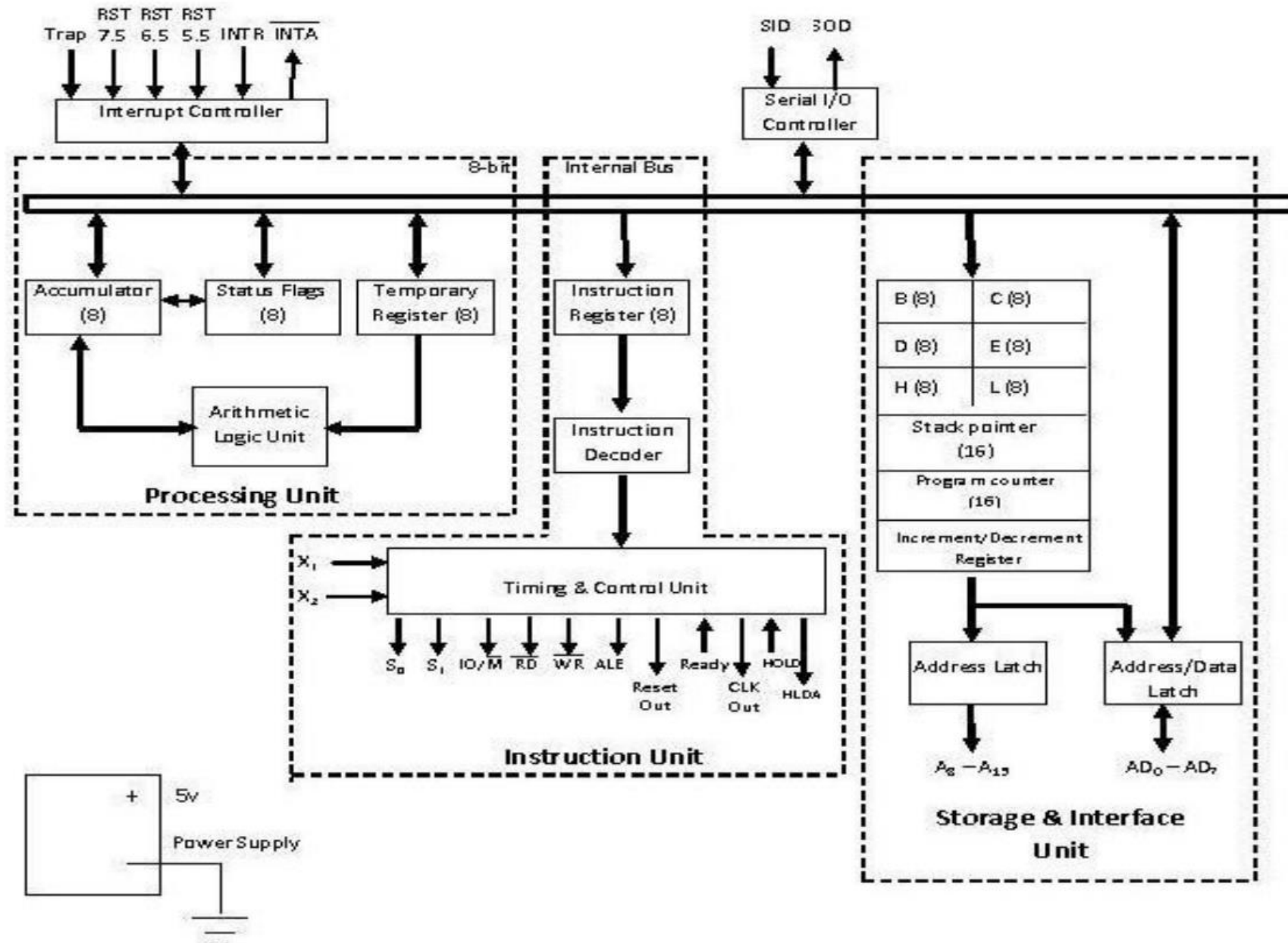
- Memory addressing capacity depends upon number of address lines in CPU
- **Set** of all possible addresses that can be generated by CPU is called **address space**. CPU can directly address all the addresses of its **address space**.
- Eg: 8086 intel microprocessor has 20 address lines and can address 1MB of memory directly using 20 bit address bus.
- Thus 1MB is the address space of INTEL 8086 microprocessor. This is also its memory size or capacity.

## 8086 capacity/size

- $2^{20} = 1048576$  no. of memory locations
- Each memory location has 8 bit data size
- Total memory size:  $1048576 * 8 \text{ bit} = 8388608 \text{ bit} = 1048576 \text{ byte} = 1024 \text{ Kbyte} = 1 \text{ Mbyte}$

## Difference between micro-processor 8085 and 8086

Parameter	8085	8086
Size	It is an 8 bit processor	It is 16 bit processor
Address bus	Address bus is 16 bits	Address bus is 20 bits
Data bus	Data bus is 8 bit.	Data bus is 16 bit
Memory	It can access upto $2^{16}$ = 65,536 bytes ( 64KB)	It can access upto $2^{20}$ = 1,048,576 bytes(1MB)
Instruction Queue	It does not have an instruction queue	It has 6 byte instruction queue
Pipelining	It does not support pipelining	It support pipelining architecture
I/Os	It Can address $2^8$ = 256 I/O locations	It can address $2^{16}$ = 65,536 I/O locations
Multiprocessing support	It does not have multiprocessing support	It supports multiprocessing. It has compatibility with further processors like 80386



Intel 8085  
internal  
architecture