8086 Bus Timing & Wait state

The Intel Microprocessors 8th Edition by Barry B Brey
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General Bus Operation

- The 8086 has a combined address and data bus commonly referred as a time multiplexed address and data bus. The main reason behind multiplexing address and data over the same pins is the maximum utilization of processor pins and it facilitates the use of 40 pin standard DIP (Dual in-line package).

- Basically, all the processor bus cycles consist of at least four clock cycles. These are referred to as T1, T2, T3, T4. The address is transmitted by the processor during T1. It is present on the bus only for one clock cycle.

Machine Cycles

- A machine (bus) cycle consists of at least four clock cycles, called T states.
- A specific, defined action occurs during each T state (labeled T1 – T4)
  - **T1**: Address is output
  - **T2**: Bus cycle type (Mem/IO, read/write)
  - **T3**: Data is supplied / Data is received
  - **T4**: Data latched by CPU, control signals removed

BUS Timing (Write/Read)

- *During T_1 :*

➢The address is placed on the Address/Data bus.

➢Control signals ALE and DT/ R’ specify memory or I/O, latch the address onto the address bus and set the direction of data transfer on data bus.

- During T_2 :

➢8086 issues the RD’ or WR’ signal, DEN’ .

➢DEN’ enables the memory or I/O device to receive the data for writes and the 8086 to receive the data for reads.

Bus timing

- During T_3 :

➢This cycle is provided to allow memory to access data.

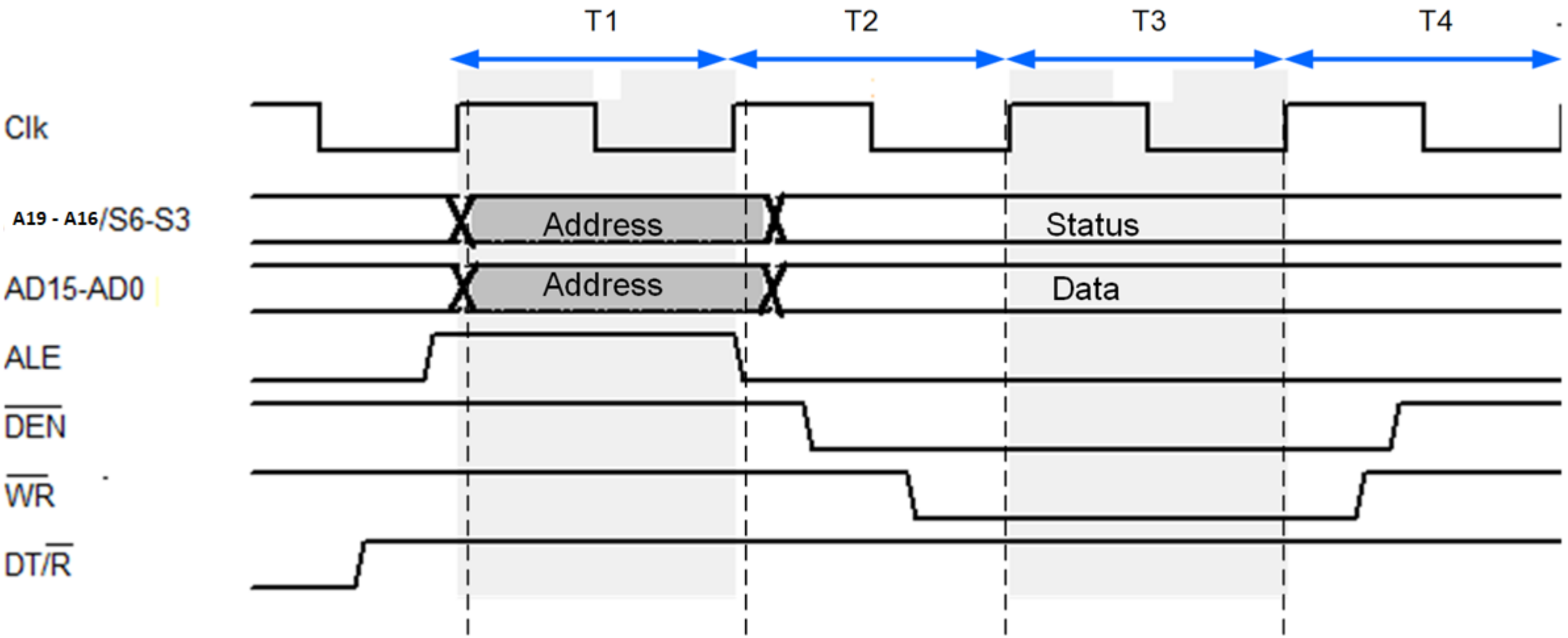
➢READY is sampled at the end of T_2 .

  - If low, T_3 becomes a wait state.

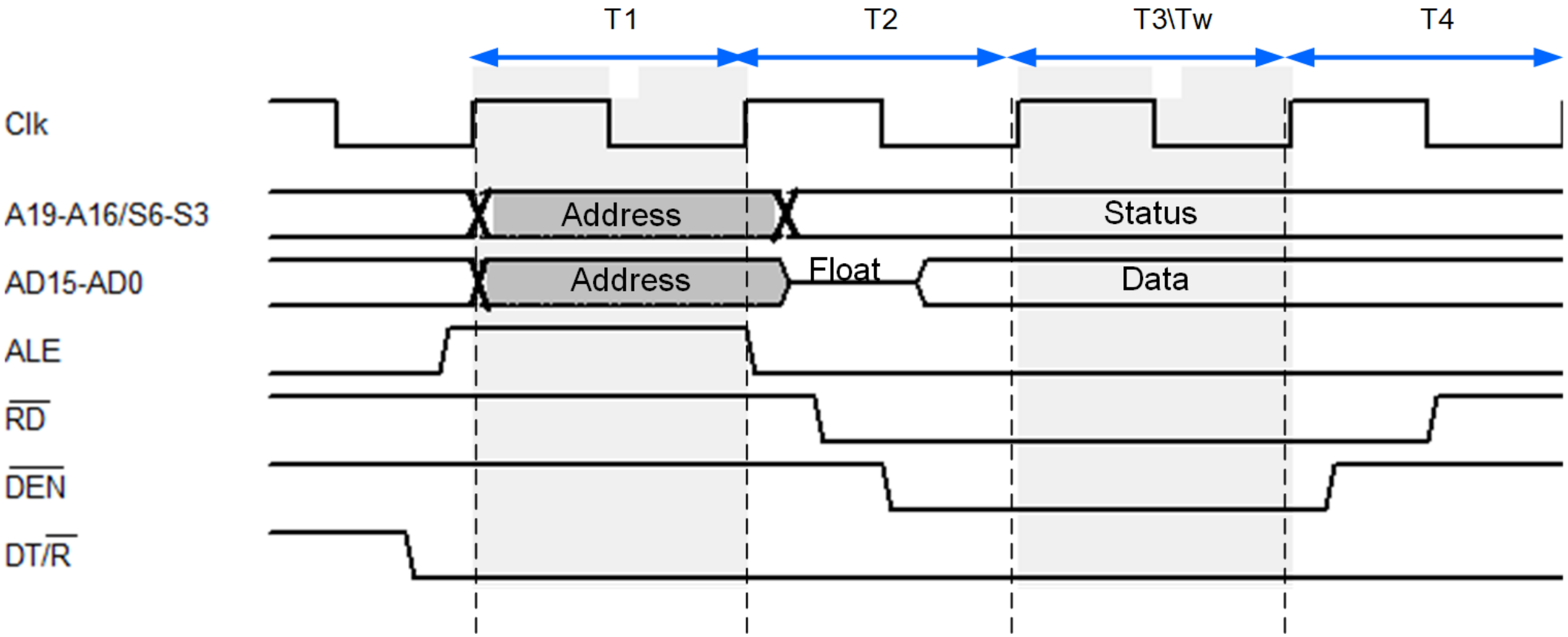
- During T_4 :

➢All bus signals are deactivated, in preparation for next bus cycle.

➢Data is sampled for reads, writes occur for writes.



Bus timing for Write operation



Bus timing for Read operation

Ready pin and Wait state

- The READY input causes wait states for slower memory and I/O components.
- A wait state is a situation in which a computer processor is waiting for the completion of some event before resuming activity. A program or process in a wait state is inactive for the duration of the wait state.
- When a computer processor works at a faster clock speed than the random access memory (RAM) that sends it instructions, it is set to go into a wait state for one or more clock cycles so that it is synchronized with RAM speed. In general, the more time a processor spends in wait states, the slower the performance of that processor.
- Wait states are a pure waste for a processor's performance. Modern designs try to eliminate or hide them using a variety of techniques: CPU caches, instruction pipelines, instruction prefetch , simultaneous multithreading and others.

8086 Ready pin

The READY input is controlled to insert “Wait states” into the timing of the microprocessor. If the READY pin is placed at a logic 0 level, the micro-processor enters into wait states and remains idle. When it is high (logic 1), it indicates that the device is ready to transfer data.