# Simple-As-Possible (SAP-1) part 1

SAP1 Malvino.pdf

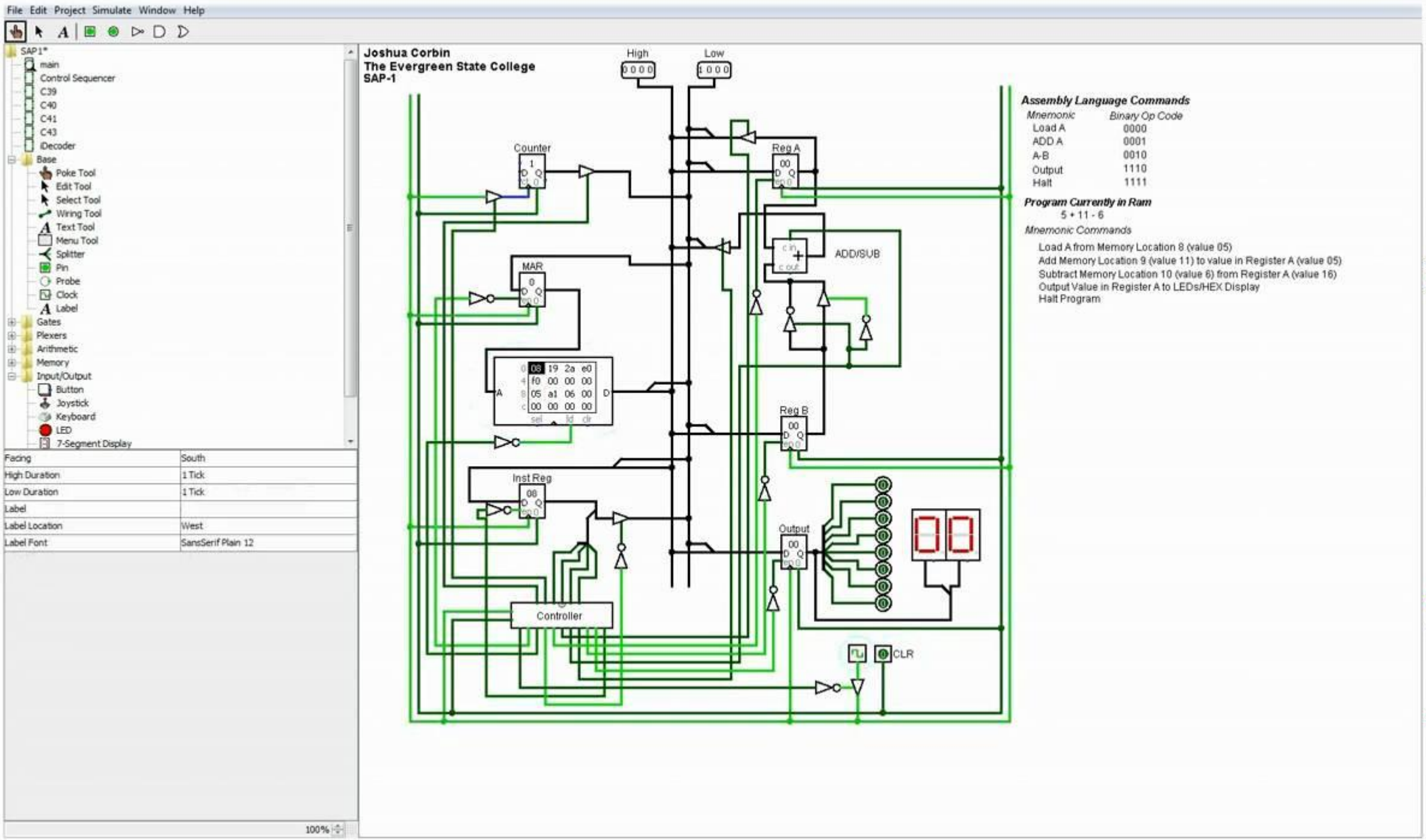
# SAP-1

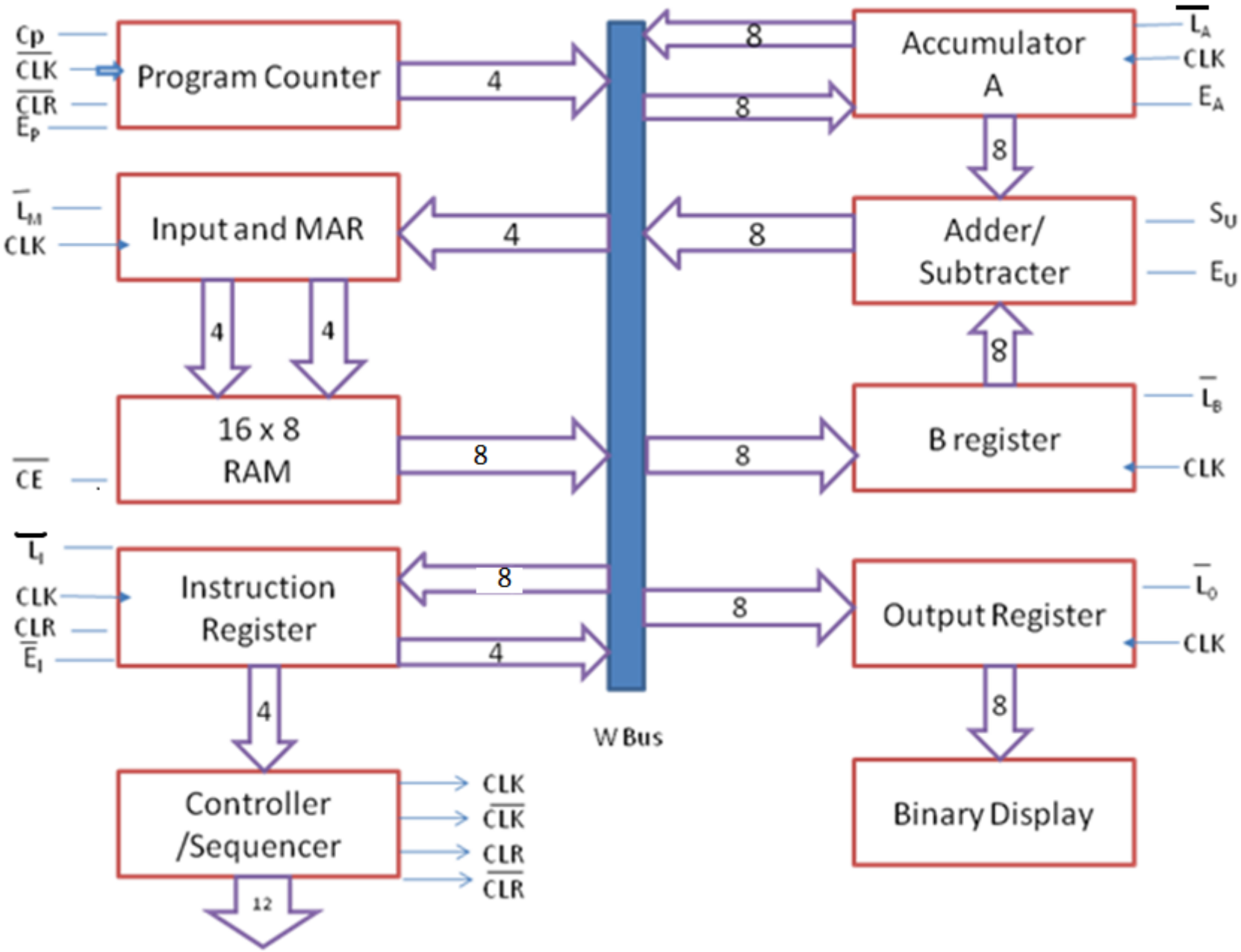
- The Simple-As-Possible (SAP)-1 computer is a very basic model of a microprocessor explained.
- The SAP-1 design contains the basic necessities for a functional Microprocessor.
- Its primary purpose is to develop a basic understanding of how a microprocessor works, interacts with memory and other parts of the system like input and output.
- The instruction set is very limited and is simple.
- SAP is Simple-As-Possible Computer. The type of computer is specially designed for the academic purpose and nothing has to do with the commercial use.

# SAP-1

- The architecture is 8 bits and comprises of 16 X 8 memory. 16 memory location with 8 bits in each location. All instructions (5 only) get stored in this memory. It means SAP cannot store program having more than 16 instructions.
- SAP can only perform addition and subtraction and no logical operation. These arithmetic operations are performed by an adder/subtractor unit.


Calculator
MC3
MC2
MC1
ASAP-3
Almost
Simple As Possible
Computer


File Edit Project Simulate Window Help
SAP1*
main
Control Sequencer
C39
C40
C41
C43
iDecoder
Base
Poke Tool
Edit Tool
Select Tool
Wiring Tool
Text Tool
Menu Tool
Splitter
Pin
Probe
Clock
Label
Gates
Plexers
Arithmetic
Memory
Input/Output
Button
Joystick
Keyboard
LED
7-Segment Display
Facing South
High Duration 1 Tick
Low Duration 1 Tick
Label
Label Location West
Label Font SansSerif Plain 12
100%
Joshua Corbin
The Evergreen State College
SAP-1
High
Low
Counter
Reg A
ADD/SUB
MAR
Reg B
Inst Reg
Output
Controller
CLR
Assembly Language Commands
Mnemonic Binary Op Code
Load A 0000
ADD A 0001
A-B 0010
Output 1110
Halt 1111
Program Currently in Ram
5 + 11 - 6
Mnemonic Commands
Load A from Memory Location 8 (value 05)
Add Memory Location 9 (value 11) to value in Register A (value 05)
Subtract Memory Location 10 (value 6) from Register A (value 16)
Output Value in Register A to LEDs/HEX Display
Halt Program




Block diagram of Simple-As-Possible (SAP)-1 Architecture

$$CON = C_P\, E_P\, L'_M\, CE' \quad L'_I\, E'_I\, L'_A\, E_A \quad S_U\, E_U\, L'_B\, L'_O$$

# SAP-1 Architecture

1. Counter Program (Program Counter)
2. Register Input & Memory Address Register (MAR)
3. 16 x 8 RAM memory
4. Register Instructions
5. Control Sequencer (Control Sequencer)
6. Accumulator A
7. Adder / Substractor
8. Register B
9. Output Register
10. Binary display

# SAP-1 Architecture : 1. Program Counter


Function

It’s job is to send to the memory the address of the next instruction to be executed and fetched.

- Control Line on Program Counter (PC):

- Ep: Transfer value from PC to Bus W
- Cp: Controls increment PC: PC ← PC + 1

# SAP-1 Architecture : 1. Program Counter

## Process

1) The PC is reset to 0000 before each computer run

2) When the computer run begins, the PC sends address 0000 to the MAR.

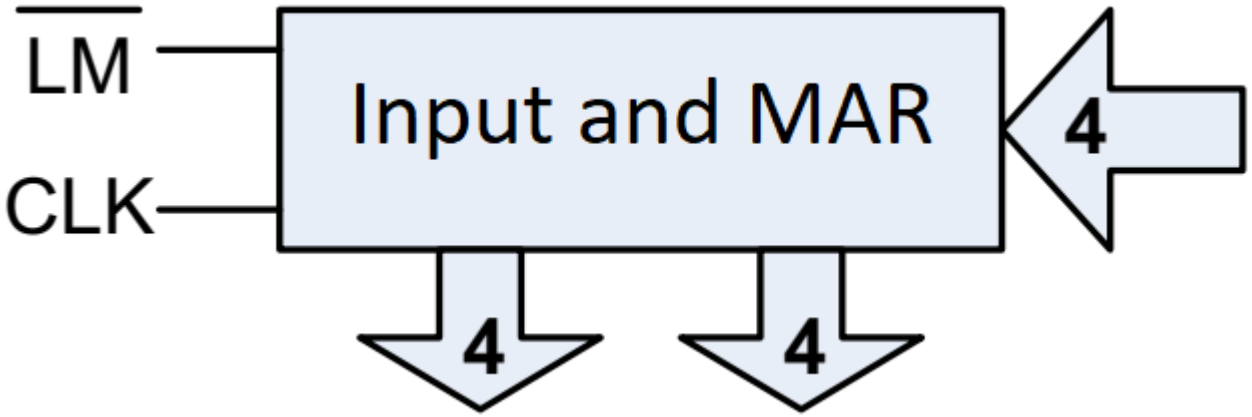
3) The pc is then incremented to get 0001.

MAR ⟵ PC
PC ⟵ PC + 1

4) After the first instruction is fetched and executed, the PC sends address 0001 to the memory.

In this way, the PC is keeping track of the next instruction to be executed.

# SAP-1 Architecture : 2. Input and MAR (Memory Address Register)




Function

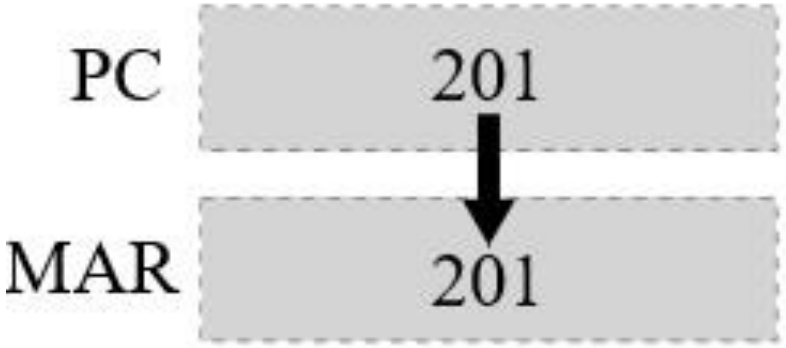
Its job is to hold (latched) the address of PC into Memory Address Register (MAR)

- Control Line on Input and MAR:

- $\overline{Lm}$: Retrieving data from bus W into MAR.

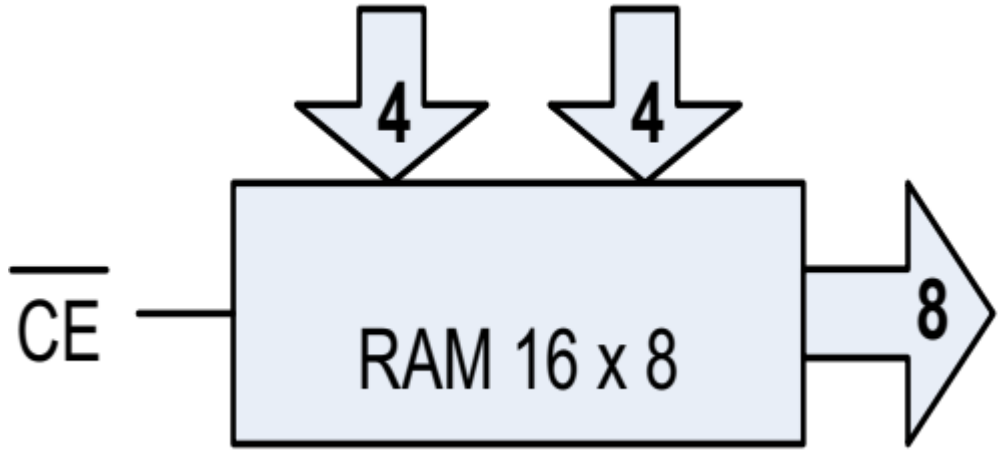
# SAP-1 Architecture : 2. Input and MAR (Memory Address Register)

**MAR <- [PC]**




| | |
|---|---|
| 201 | LOAD 206 |
| 202 | ADD #205 |
| 203 | STORE 205 |

# SAP-1 Architecture : 3. RAM




Function

The program code to be executed and data for SAP-1 computer is stored here.

- Control Line on RAM:

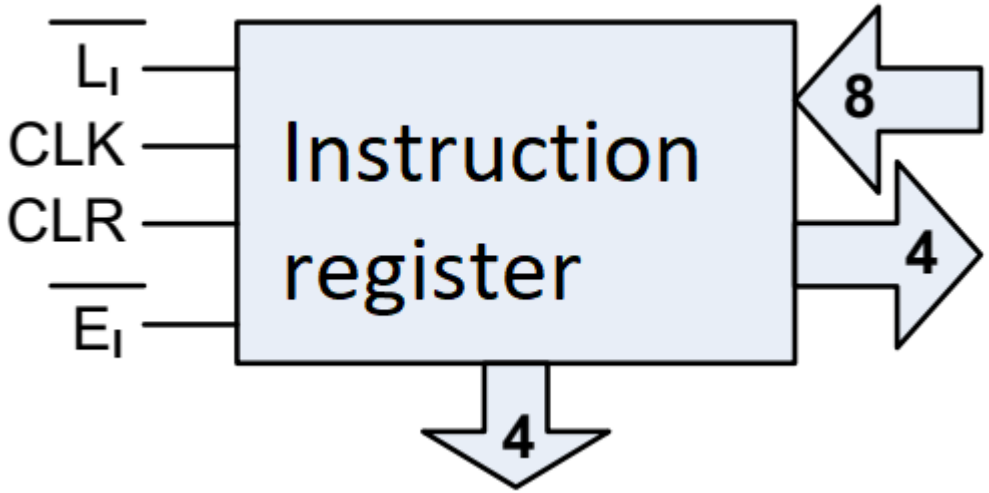
- $\overline{CE}$: Removing data 8 bit from memory to bus W.

# SAP-1 Architecture : 3. RAM

- Process

1) MAR applies 4-bit address to the RAM, where a real read operation is performed
2) Thus, the instruction or data word stored in RAM is placed on the W bus for use by some other part of the computer.

# SAP-1 Architecture : 4. Instruction register




Function

IR contains the instruction (composed of OPCODE+ADDRESS) to be executed by SAP1 computer.

❑ Control Line on Instruction register:

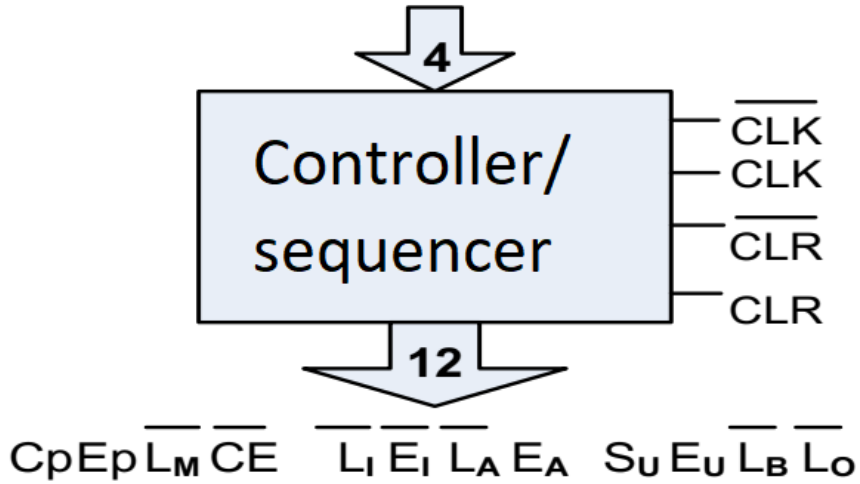
- $\overline{L1}$: Retrieve 8 bit data from bus W.
- $\overline{E1}$: Controls 4 bit data from IR to bus W.

# SAP-1 Architecture : 4. Instruction register

- Process

1) The contents of the IR are split into two nibbles.
2) The upper nibble is a two state output that goes directly to the block labelled ‘Controller-sequencer’.
3) The lower nibble is send to the W-bus.

# SAP-1 Architecture : 5. Controller/Sequences

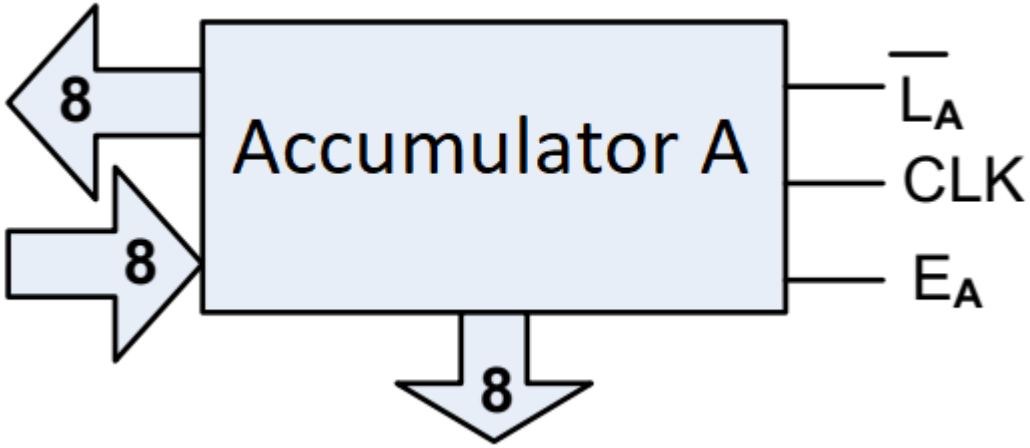



Function

- It generates the control signals for each block so that actions occur in desired sequence. CLK signal is used to synchronize the overall operation of the SAP1 computer.

- A 12-bit word comes out of the Controller-Sequencer block. This control word determines how the registers will react to the next positive CLK edge.

# SAP-1 Architecture : 6. Accumulator A



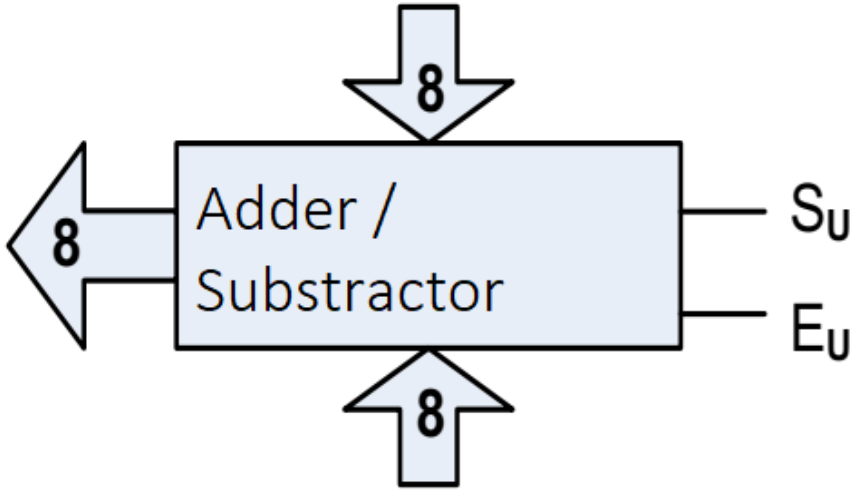

Function

- It is a 8-bit buffer register that stores intermediate results during a computer run.
- It is always one of the operands of ADD, SUB and OUT instructions.

❑ Control Line on Accumulator A:

- $\overline{La}$: Retrieve 8 bit data from bus W.
- Ea: Control the 8 bit data into bus W (The value appeared in the W bus)

# SAP-1 Architecture : 7. Adder / Substractor



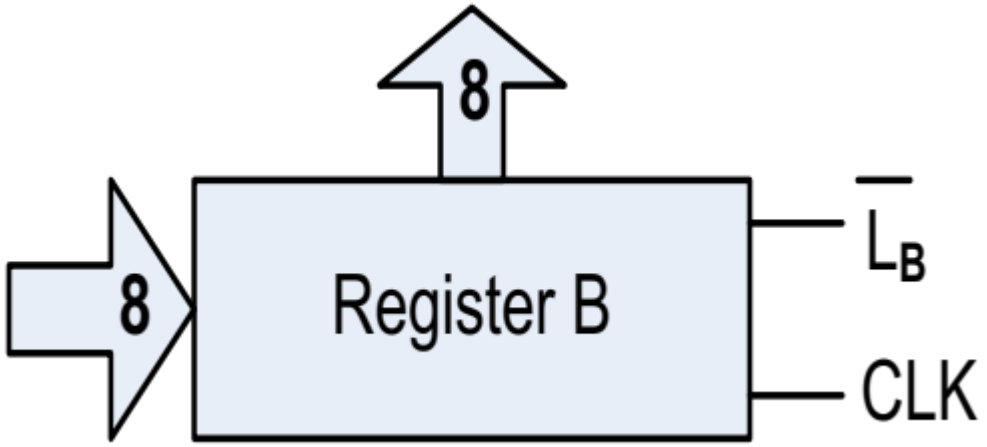

Function

- It is a 2's complement adder-subtractor.

❑ Control Line on Adder / Substractor:

- Su: Low signal (0) then addition operation, when signal high (1) then the operation substraction.
- Eu: Send data to bus W

# SAP-1 Architecture : 8. Register B



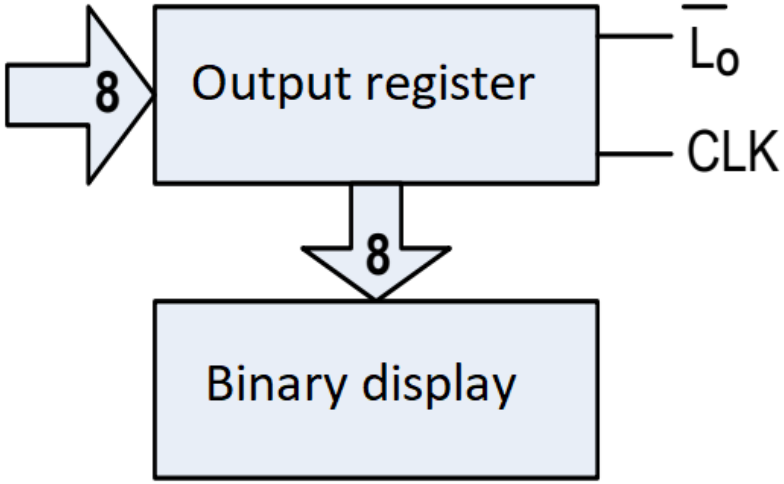

Function

- It is 8-bit buffer register which is primarily used to hold the other operand (one operand is always accumulator) of mathematical operations.

❑ Control Line on Register B:

- Lb: Retrieve data from bus W to register B

# SAP-1 Architecture : 9. Output Register



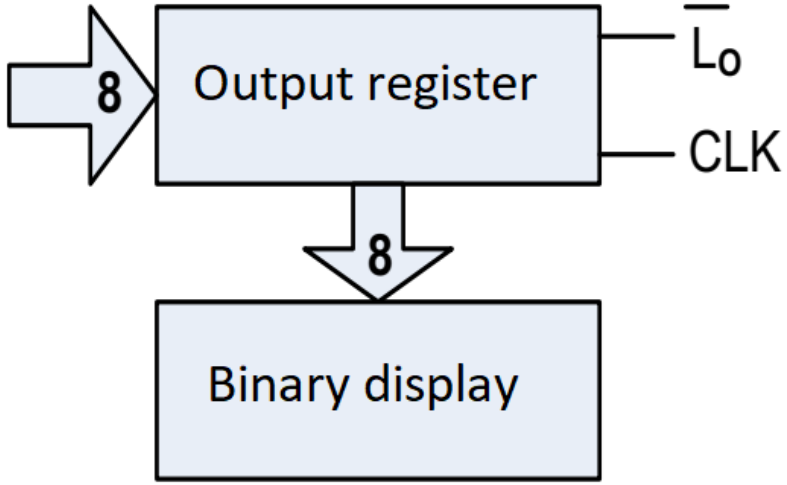

Function

- This registers hold the output of OUT instruction.

❑ Control Line on Output Register:

- Lo: Retrieve data 8 bits from bus W

# SAP-1 Architecture : 10. Binary display




Function

- It is a row of eight LEDs to show the contents of output register.
- Binary display unit is the output device for the SAP-1 microprocessor.

# SAP-1 Architecture : Exercise