CS202 · Computer Organization

Assignment 1

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Problem 1

(a)

$$\text{CPU time} = \frac{\#\text{instructions} \times \text{CPI}}{\text{clock rate}} \tag{1}$$

$$\#\text{instructions} = \frac{\text{CPU time} \times \text{clock rate}}{\text{CPI}} \tag{2}$$

To calculate the *instructions per second*, we let the CPU time as 1sec, substituting the CPI and clock rate then we will have:

$$\begin{cases} \text{IPS}_1 = \frac{1\text{s}\times 3\text{GHz}}{1.5} = 2 \times 10^9 \\ \text{IPS}_2 = \frac{1\text{s}\times 2.5\text{GHz}}{1.0} = 2.5 \times 10^9 \\ \text{IPS}_3 = \frac{1\text{s}\times 4\text{GHz}}{2.2} \approx 1.8 \times 10^9 \end{cases}$$

Therefore, *P2* has the highest performance expressed in instructions per second.

(b)

$$\#\text{cycles} = \text{CPU time} \times \text{clock rate} \tag{1}$$

$$\#\text{instruction} = \frac{\#\text{cycles}}{\text{CPI}} \tag{2}$$

	#cycles	#instruction
P1	3×10^{10}	2×10^{10}
P2	2.5×10^{10}	2.5×10^{10}
P3	4×10^{10}	1.8×10^{10}

(c) With an unchanged #instructions, we find that

$$\text{CPU time} \propto \frac{\text{CPI}}{\text{clock rate}}$$

a.k.a., $(1.2\ \text{CPI}_{\text{old}})/\ \text{clock rate}_{\text{new}} = 0.7(\ \text{CPI}_{\text{old}}\ /\ \text{clock rate}_{\text{old}})$, that is, the new clock rate is about *1.71* time of the old clock rate.

Problem 2

(*) As shown in **(b)**, the CPU time of P1 is $\frac{2.6\times 10^6}{2.5\text{GHz}} = 1.04\text{ms}$, while the CPU time of P2 is $\frac{2.0\times 10^6}{3\text{GHz}} \approx 0.67\text{ms}$. It's trivial that P2 is faster.

(a)

$$\mathrm{CPI}_{\mathrm{glob}} = \frac{\Sigma \mathrm{CPI}_{\mathrm{class}} \times \#\mathrm{inst}_{\mathrm{class}}}{\Sigma \#\mathrm{inst}_{\mathrm{class}}} = \Sigma \mathrm{CPI}_{\mathrm{class}} \times \%_{\mathrm{class}}$$
$$\mathrm{CPI}_{P1} = 1 \cdot 10\% + 2 \cdot 20\% + 3 \cdot 50\% + 3 \cdot 20\% = 2.6$$
$$\mathrm{CPI}_{P2} = 2 \cdot 10\% + 2 \cdot 20\% + 2 \cdot 50\% + 2 \cdot 20\% = 2$$

(b)

$$\#\mathrm{cycles} = \mathrm{CPI}_{\mathrm{glob}} \times \#\mathrm{instructions}$$
$$\#\mathrm{cycles}_{\mathrm{P1}} = 2.6 \times 10^6$$
$$\#\mathrm{cycles}_{\mathrm{P2}} = 2.0 \times 10^6$$

Problem 3

(a)

$$\mathrm{CPI} = \frac{\text{CPU time} \times \text{clock rate}}{\#\text{instructions}}$$
$$\mathrm{CPI}_A = \frac{1.1s \cdot 10^9 Hz}{10^9} = 1.1$$
$$\mathrm{CPI}_B = \frac{1.5s \cdot 10^9 Hz}{1.2 \cdot 10^9} = 1.25$$

(b)

$$\text{CPU time} \times \text{clock rate} = \mathrm{CPI} \times \#\text{instructions}$$
$$\frac{\text{clock rate}_1}{\text{clock rate}_2} = \frac{\mathrm{CPI}_1 \times \#\text{instructions}_1}{\mathrm{CPI}_2 \times \#\text{instructions}_2} = \frac{1.1}{1.5} \approx 0.73$$

Or say processor B is 1.36 time as fast as processor A.

(c)

$$\text{CPU time} \times \text{clock rate} = \mathrm{CPI} \times \#\text{instructions}$$

When we are considering "speed up" of compilers, we usually assume that the clock rate keeps the same.

$$\text{CPU time} \propto \mathrm{CPI} \times \#\text{instructions}$$
$$\text{speed}_{\text{new}}/\text{speed}_A = \text{CPU time}_A/\text{CPU time}_{\text{new}} = \frac{1.1 \cdot 10^9}{1.1 \cdot 6 \times 10^8} \approx 1.67$$
$$\text{speed}_{\text{new}}/\text{speed}_B = \text{CPU time}_B/\text{CPU time}_{\text{new}} = \frac{1.25 \cdot 1.2 \times 10^9}{1.1 \cdot 6 \times 10^8} \approx 2.27$$

Problem 4

(a)

$$P_{\text{dyn}} = \frac{1}{2} C V^2 f$$
$$C = \frac{2 P_{\text{dyn}}}{V^2 f}$$
$$C_{\text{Pentium}} = \frac{2 \cdot 90W}{(1.25V)^2 \cdot 3.6GHz} = 3.2 \times 10^{-8} F$$
$$C_{\text{Core i5}} = \frac{2 \cdot 40W}{(0.9V)^2 \cdot 3.4GHz} \approx 2.9 \times 10^{-8} F$$

(b)

Pentium 4 the percentage of the total dissipated power comprised by static power is $\frac{10W}{10W+90W} = 0.1 = 10\%$; the ratio of static power to dynamic power is 1 : 9.

Core i5 the percentage of the total dissipated power comprised by static power is $\frac{40W}{40W+30W} \approx 0.43 = 42.9\%$; the ratio of static power to dynamic power is 3 : 4.

(c)

$$P = P_{\text{dyn}} + P_{\text{stat}} = \frac{1}{2}CV^2 f + I_{\text{leak}}V$$
$$I_{\text{leak}} = P_{\text{stat}}/V$$

Pentium 4 Voltage should be reduced to about 1.18V, which is a 5.6% reduction.

$$\begin{aligned} I_{\text{leak}} &= \frac{10W}{1.25V} = 8A \\ 90W &= \frac{1}{2} \times 3.2 \cdot 10^{-8}F \times V_{\text{new}}^2 \times 3.6GHz + 8A \times V_{\text{new}} \\ V_{\text{new}} &\approx 1.18V \end{aligned}$$

Core i5 Voltage should be reduced to about 0.84V, which is a 6.7% reduction.

$$\begin{aligned} I_{\text{leak}} &= \frac{30W}{0.9V} \approx 33.34A \\ 63W &= \frac{1}{2} \times 2.9 \cdot 10^{-8}F \times V_{\text{new}}^2 \times 3.4GHz + 33.34A \times V_{\text{new}} \\ V_{\text{new}} &\approx 0.84V \end{aligned}$$