DIGITAL DESIGN

ASSIGNMENT 1

Deadline: *22:30, Wednesday 13 October 2021*

Lab sessions&Location:

1. **Lychee Garden 6, Room 409 (Wednesday 14:00-15:50 pm)**
2. **Lychee Garden 6, Room 404 (Thursday 10:10-12:10 am)**
3. **Teaching Building 2, Room 205 (Friday 10:10-12:10 am)**
4. **Lychee Garden 6, Room 402 (Friday 14:00~15:50 pm)**

Teaching Assistant:

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. What is the exact number of bytes in a system that contains (a) 16K bytes, (b) 32M bytes, and (c) 3.2G bytes?
2. What is the largest binary number that can be expressed with 12 bits? What are the equivalent decimal and hexadecimal numbers?
3. Convert the decimal number 248 to binary in two ways: (a) convert directly to binary; (b) convert first to hexadecimal and then from hexadecimal to binary. Which method is faster?
4. Find the 9's and the 10's complement code of the following **decimal** numbers.
   a. 25273036
   b. 64322610
5. (a) Find the 16's complement of C6BF.
   (b) Convert C6BF to binary.
   (c) Find the 2's complement of the result in (b).
   (d) Convert the answer in (c) to hexadecimal, compare with the answer in (a).
6. Do the following conversion problems:
   (a) Convert decimal 23.5625 to binary.
   (b) Calculate the binary equivalent of 5/3 out to eight places. Then convert from binary to decimal. How close is the result to 5/3?
   (c) Convert the binary result in (b) into hexadecimal. Then convert the result to decimal. Is the answer the same? Explain why.
7. The state of a 12-bit register is 100101110101. What is its content if it represents
   (a) Three decimal digits in BCD?
   (b) Three decimal digits in the excess-3 code?
   (c) Three decimal digits in the 8,4,-2,-1 code?
   (d) Three decimal digits in the 6311 code?

(e) A binary number?

8. We can perform logical operations on strings of bits by considering each pair of corresponding bits separately (called **bitwise operation**). Given two eight - bit strings A = 11011010 and B = 01001110, evaluate the eight - bit result after the following bitwise logical operations: (a) AND (b) OR (c) XOR (d) NOT A (e) NOT B (f) NAND (g) NOR. **(Please represent all the 7 results in hexadecimal)**

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 to design a simple logic circuit: Do the addition on two signed 2bit numbers, do the simulation and verify its function by simulation. You should submit the description of the operation steps, the Verilog design and test-bench, the waveform from the simulation, and the function verification results.

PREAMBLE

Before working on the coursework itself, you should master the following material. A separate tutorial document (on the Sakai site) has be provided to you which includes:

- Vivado: The Vivado software provides a complete design environment for system-on-a-programmable-chip (SOPC) design. Regardless of whether you use a personal computer or a Linux workstation, Vivado ensures easy design entry, fast processing, and straightforward device programming.
- Minisys Practice platform: a practice platform designed for Digital design, Principles of Computer Organization and many other courses. This platform include FPGA chip, storage chip and lots of Dial switches for input and lots of LEDs for output.

- Verilog : standardized as IEEE 1364, is a hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification(test-bench) of digital circuits at the Register-Transfer-Level of abstraction. It is also used in the verification of analog circuits and mixed-signal circuits, as well as in the design of genetic circuits. http://www.verilog.com/

EXERCISE SPECIFICATION

In practical part, you will focus on how to use Vivado to do the design, simulation, generate the bitstream file which is used to program the FPGA chip (a part of the Minisys practice platform), you will also learn some basic concepts of Verilog. The steps you need to follow are:

1. Create an empty vivado project, or open an exist vivado project.
2. Edit a design file (Verilog file) & add it to the project.
3. Edit a simulation file (Verilog file) & add it to the project.
4. Do the simulation with the simulation file(test-bench) to verify the function of the circuit design. If the function is not ok, modify the design and do the simulation, repeat the step until the function verification pass.
5. Edit a constraints file (to define the Specifications of pins and the binding info between pins and the designed ports) & add it to the project.
6. Do the synthesize.
7. Do the implementation.
8. Generate the bitstream file.
9. Connect the Vivado project to the board(FPGA chip inside) & turn on the board.
10. Program the device(FPGA chip) with the bitstream file.
11. Test the design on the board (the dial switch is used as input, the LEDs is used as output)

In task1 and task2 of assignment1, you should just focus on step 1~4.

TASK1:

Create a project named as UnsignedAddition, design the source code to implement following function: **get the addition of two input numbers, and output the sum**. The bit-width of the inputs and the output is determined by parameter. **Do the simulation and to verify the function of the circuit design while the bit-width of inputs is 1bit and 2bit respectively**.

Note

(1) Two input number here should be treated as unsigned number. For example, if the bit-width is 2, the value of $(11)_2$ is $(3)_{10}$, the value of $(10)_2$ is $(2)_{10}$.

(2) There should be two inputs and one output (the output is used to demonstrate the value of the sum of two inputs) //following module is just a simplified demo.

```
module UnsignedAddition(addend, augend, sum_led);
parameter WIDTH=1;
input [WIDTH-1: 0] addend;
Input [WIDTH-1: 0]    augend;
output [?: 0]    sum_led;
……
Endmodule
```

(3) The Simulation is asked to cover all the test cases, explain every test case according to the waveform with the corresponding arithmetic expression.

For example, from the waveform, the inputs are $(10)_2$ and $(11)_2$, the output is $(100)_2$. This is ok, because $2((10)_2) + 3((11)_2) = 5((101)_2)$

(4) Redundant simulation is asked to be avoid. If the needed simulation time is smaller than 1000ns(the default simulation time), the simulation should NOT last for 1000ns. For example, if there are 4 test-cases in total, each test-case last for 10ns, the simulation time should be 40ns instead of 1000ns.

TASK2:

1) Do the design using data flow and structured style respectively (While doing the design with structured style, It is optional to use primitive gate, encapsulated IP or Parametric module) to verify the following theorem (you can find the design on the lab3 and lab4 courseware as a reference):

Distributive law: a) **A(B + C) = AB + AC** b) **A + BC = (A + B)(A + C)**.

the bit-width of A,B and C is 1bit

2) Create a test bench, do the simulation to verify the function of the design.

3) Repeat step1) and step2) while the bit-width of A, B and C is 2bit to judge if Distributive law is true while A,B and C is multi bit-width.

NOTE:

1) Naming the file:
   a. For data flow design, the source file should be distributive1bit_df.v, distributive2bit_df.v
   b. For structured design, the source file should be distributive1bit_sd.v, distributive2bit_sd.v
2) All the design could share the same test bench file if possible.
3) **The Simulation is asked to cover all the test cases, while redundant simulation is asked to be avoid**. If the needed simulation time is smaller than 1000ns(the default simulation time), the simulation should NOT last for 1000ns. For example, if there are 4 test-cases in total, each test-case last for 10ns, the simulation time should be 40ns instead of 1000ns.

SUBMISSION

Submit your assignment report to the BlackBoard on *Corresponding site* (“Digital Logic Fall 2021(Lab)” by the deadline.(NOTE: There is ONLY 1 DDL on BlackBoard)

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 35%

Question 1	3
Question 2	3
Question 3	2
Question 4	4
Question 5	6=2+1+2+1
Question 6	5=1+2+2
Question 7	5
Question 8	7
Total	35 marks

Lab: 65%

Task 1: Design in Verilog, the truth-table while the bit-width of inputs is 1bit and 2bit respectively.	5*2 marks
Task 1: Test bench in Verilog, simulation result(waveform and description)	5*2 marks
Task 2: Design with data-flow style, design with structure-design style, the truth-table(for both 1bit bit-width and 2bit bit-width inputs)	5*3*2 marks
Task 2: Test bench in Verilog, simulation result(waveform and description)	5*2 marks
Problems and solutions	5 marks
Total	65 marks

The template for the report is provided in the next pages.

DIGITAL DESIGN

ASSIGNMENT REPORT

ASSIGNMENT ID : xxxx

Student Name: xxxx

Student ID: xxxx

PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog(provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*

- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*