VIA Labs, Inc.

Data Sheet

VL800
4-Port USB 3.0 Host Controller

April 25, 2010
Revision 0.81

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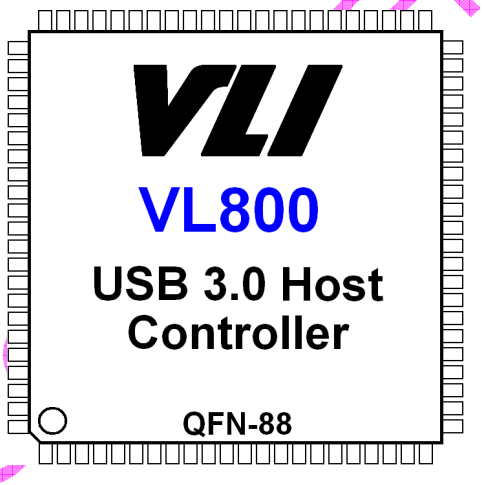

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Revision History

Rev	Date	Initial	Note
0.61	4/9/2010	TS	First release
0.62	4/12/2010	AL	1. Describe firmware upgrade feature 2. Describe battery charging feature
0.81	4/25/2010	TS	1. Updated Mechanical Specification. 2. Replaced Pinout Diagram 3. Modify pin list and pin definition for SPI interface.

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Product Features

VL800
4-Port USB 3.0 Host Controller

- **Compliant to Universal Serial Bus 3.0 Specification Revision 1.0**
  - Supports all transfer types: Control, Bulk, Stream, Interrupt, Isochronous
- **Compliant to Universal Serial Bus 2.0 Specification**
- **Compliant to eXtensible Host Controller Interface (xHCI) Specification Revision 0.96**
- **Support Legacy USB Function**
  - Four down-stream ports support SuperSpeed(SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS)
- **Support Battery Charging Specification**
  - Compliant to Battery Charging Specification Revision 1.1
  - Support for Battery Charging Specification Draft 2.0
- **Firmware Upgrade**
  - Support SPI interface for firmware upgrade (for Add-In card, etc.)
  - Option to integrate firmware in system BIOS (for motherboard)
- **Compliant with PCI Express Base Specification 2.0**
  - Supports ExpressCard Standard 2.0
- **In-house USB and PCIe PHY employs advanced CMOS process to reduce power consumption**
  - 3.3 V and 1.0 V power supply
  - USB 3.0 low power states support
- **Software**
  - Initial Driver Support for Windows 7, Vista, and XP
    - Bulk Only Transfer (BOT)
    - USB Attached SCSI Protocol (UASP)
  - Support various Linux kernels
- **Physical**
  - QFN 88L green package (10x10x0.85 mm)
- **Applications**
  - Motherboard
  - Notebook/Netbook
  - Express Card
  - Add-in Card
  - Embedded System

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VL800 System Overview

VIA Labs' VL800 is a single chip USB 3.0 Host controller which enables a PCI Express equipped platform to interface with USB Super-Speed (5 Gbps), High-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (1.5 Mbps) devices. The root hub consists of four downstream facing ports, allowing simultaneous operation of multiple peripheral devices. The VL800 has an x1 PCI Express 2.0 bus interface that is backwards compatible with PCI Express 1.0.

The VL800 complies with the Universal Serial Bus 3.0 Specification and Intel's eXtensible Host Controller Interface (xHCI), and is fully backward compatible with USB 2.0 and 1.1 specifications, ensuring seamless connectivity of legacy USB devices.

With well-planned pinout and advanced process, VL800 based devices enjoy easy layout and low working temperature in a compact footprint. Sideband signal pins are available for showing power enable, over current, and LED status. VL800 is available in QFN 88L green package (10x10x0.85 mm) to fit small form-factor designs.

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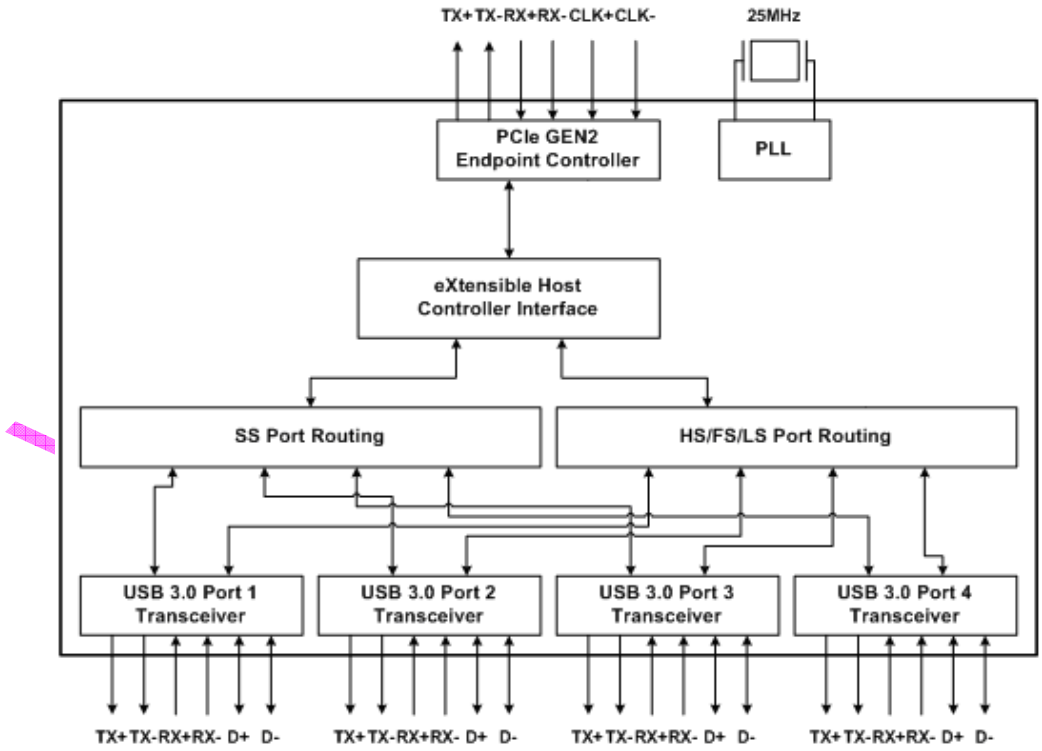

Figure 1 – VL800 Block Diagram

Pinout

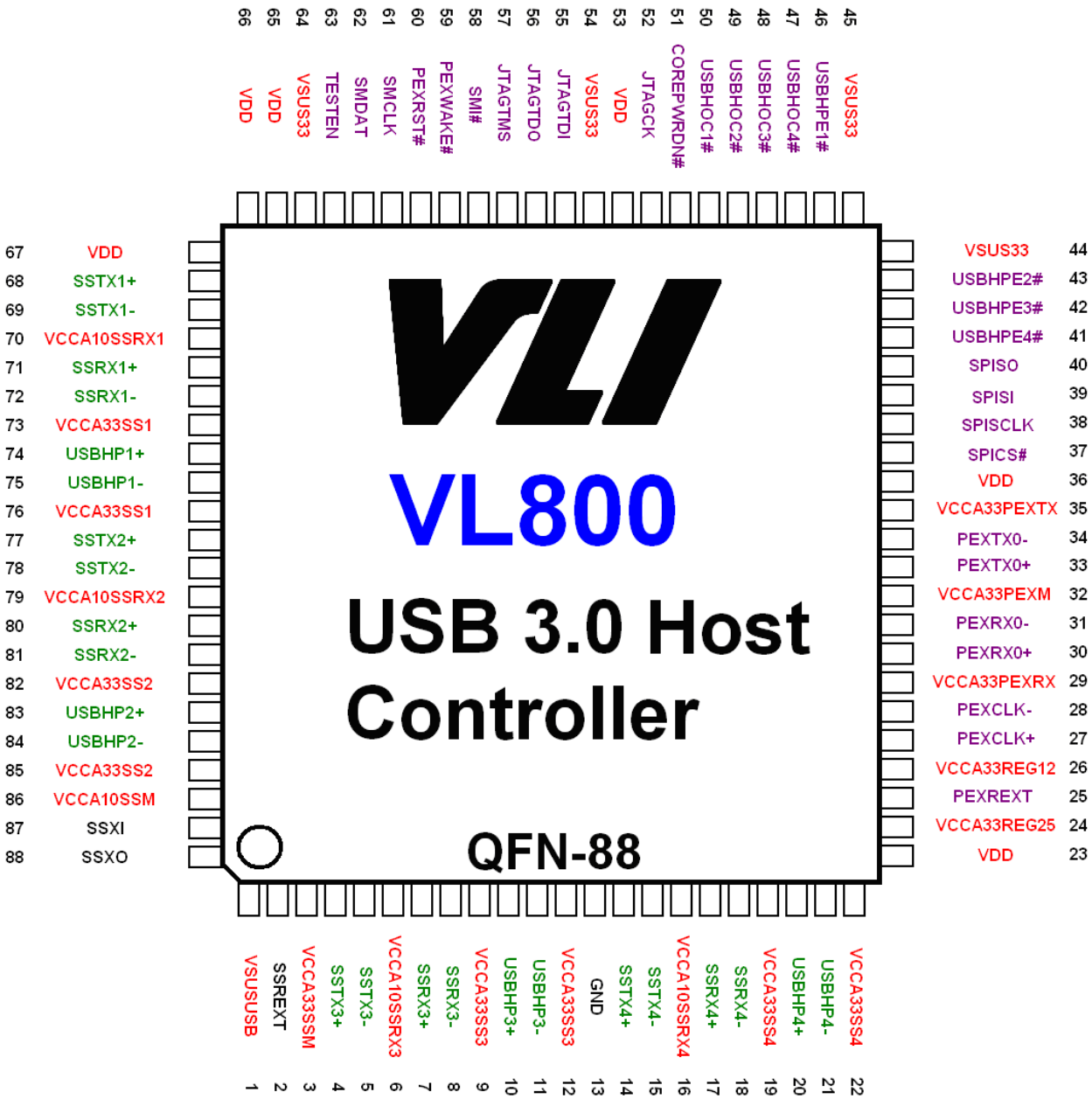

Figure 2 – VL800 Pin Diagram

Pin List

Table 1 – VL800 Pin List

Pin	Pin Name	Pin	Pin Name
1	VSUSUSB	45	VSUS33
2	SSREXT	46	USBHPE1#
3	VCCA33SSM	47	USBHOC4#
4	SSTX3+	48	USBHOC3#
5	SSTX3-	49	USBHOC2#
6	VCCA10SSRX3	50	USBHOC1#
7	SSRX3+	51	COREPWRDN#
8	SSRX3-	52	JTAGCK
9	VCCA33SS3	53	VDD
10	USBHP3+	54	VSUS33
11	USBHP3-	55	JTAGTDI
12	VCCA33SS3	56	JTAGTDO
13	GND	57	JTAGTMS
14	SSTX4+	58	SMI#
15	SSTX4-	59	PEXWAKE#
16	VCCA10SSRX4	60	PEXRST#
17	SSRX4+	61	SMCLK
18	SSRX4-	62	SMDAT
19	VCCA33SS4	63	TESTEN
20	USBHP4+	64	VSUS33
21	USBHP4-	65	VDD
22	VCCA33SS4	66	VDD
23	VDD	67	VDD
24	VCCA33REG25	68	SSTX1+
25	PEXREXT	69	SSTX1-
26	VCCA33REG12	70	VCCA10SSRX1
27	PEXCLK+	71	SSRX1+
28	PEXCLK-	72	SSRX1-
29	VCCA33PEXRX	73	VCCA33SS1
30	PEXRX0+	74	USBHP1+
31	PEXRX0-	75	USBHP1-
32	VCCA33PEXM	76	VCCA33SS1
33	PEXTX0+	77	SSTX2+
34	PEXTX0-	78	SSTX2-
35	VCCA33PEXTX	79	VCCA10SSRX2
36	VDD	80	SSRX2+
37	SPICS#	81	SSRX2-
38	SPISCLK	82	VCCA33SS2
39	SPISI	83	USBHP2+
40	SPISO	84	USBHP2-
41	USBHPE4#	85	VCCA33SS2
42	USBHPE3#	86	VCCA10SSM
43	USBHPE2#	87	SSXI
44	VSUS33	88	SSXO

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Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

USB 3.0 Root Hub Interface

Pin Name	Pin #	I/O	Signal Description
SSTX1+	68	O	USB 3.0 DP1 Port Differential Transmit Data +
SSTX1-	69	O	USB 3.0 DP1 Port Differential Transmit Data -
SSRX1+	71	I	USB 3.0 DP1 Port Differential Receive Data +
SSRX1-	72	I	USB 3.0 DP1 Port Differential Receive Data -
VCCA10SSRX1	70	PWR	Analog 1.0V
VCCA33SS1	73,76	PWR	Analog 3.3V
SSTX2+	77	O	USB 3.0 DP2 Port Differential Transmit Data +
SSTX2-	78	O	USB 3.0 DP2 Port Differential Transmit Data -
SSRX2+	80	I	USB 3.0 DP2 Port Differential Receive Data +
SSRX2-	81	I	USB 3.0 DP2 Port Differential Receive Data -
VCCA10SSRX2	79	PWR	Analog 1.0V
VCCA33SS2	82,85	PWR	Analog 3.3V
SSTX3+	4	O	USB 3.0 DP3 Port Differential Transmit Data +
SSTX3-	5	O	USB 3.0 DP3 Port Differential Transmit Data -
SSRX3+	7	I	USB 3.0 DP3 Port Differential Receive Data +
SSRX3-	8	I	USB 3.0 DP3 Port Differential Receive Data -
VCCA10SSRX3	6	PWR	Analog 1.0V
VCCA33SS3	9,12	PWR	Analog 3.3V
SSTX4+	14	O	USB 3.0 DP4 Port Differential Transmit Data +
SSTX4-	15	O	USB 3.0 DP4 Port Differential Transmit Data -
SSRX4+	17	I	USB 3.0 DP4 Port Differential Receive Data +
SSRX4-	18	I	USB 3.0 DP4 Port Differential Receive Data -
VCCA10SSRX4	16	PWR	Analog 1.0V
VCCA33SS4	19,22	PWR	Analog 3.3V
VCCA33SSM	3	PWR	USB 3.0 Master Block Analog 3.3V

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USB 2.0 Root Hub Interface

Pin Name	Pin #	I/O	Signal Description
USBHP1+	74	I/O	USB 2.0 DP1 Bus Data Plus (D+)
USBHP1-	75	I/O	USB 2.0 DP1 Bus Data Minus (D−)
USBHP2+	83	I/O	USB 2.0 DP2 Bus Data Plus (D+)
USBHP2-	84	I/O	USB 2.0 DP2 Bus Data Minus (D−)
USBHP3+	10	I/O	USB 2.0 DP3 Bus Data Plus (D+)
USBHP3-	11	I/O	USB 2.0 DP3 Bus Data Minus (D−)
USBHP4+	20	I/O	USB 2.0 DP4 Bus Data Plus (D+)
USBHP4-	21	I/O	USB 2.0 DP4 Bus Data Minus (D−)

PCI Express x1 Interface

Pin Name	Pin #	I/O	Signal Description
VCCA33PEXTX	35	PWR	Analog 3.3V
PEXTX0+	33	O	Transmitter Lane 0, Differential +
PEXTX0-	34	O	Transmitter Lane 0, Differential -
VCCA33PEXM	32	PWR	Analog 3.3V
PEXRX0+	30	I	Receiver Lane 0, Differential +
PEXRX0-	31	I	Receiver Lane 0, Differential -
VCCA33PEXRX	29	PWR	Analog 3.3V
PEXCLK+	27	I	Reference Clock, Differential +
PEXCLK-	28	I	Reference Clock, Differential -
PEXWAKE#	59	I	Link Reactivation
VCCA33REG25	24	PWR	Analog 3.3V
VCCA33REG12	26	PWR	Analog 3.3V

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	87	I	25M crystal input
SSXO	88	O	25M crystal output
VCCA10SSM	86	PWR	1.0V OSC VDDA
SSREXT	2	A_{BIAS}	Connect to reference resistor for SuperSpeed USB
PEXREXT	25	A_{BIAS}	Connect to reference resistor for PCIe

SPI Flash Interface

Pin Name	Pin #	I/O	Signal Description
SPICS#	37	O	SPI Chip Select
SPISCLK	38	O	SPI Serial Clock Input
SPISI	39	O	SPI Serial Data Input
SPISO	40	I	SPI Serial Data Output

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Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	63	I	Test Mode Enable Do not connect for normal operation. Internal pull down.
JTAGCK	52	I	Test Clock
JTAGTDI	55	I	Test Data In
JTAGTDO	56	O	Test Data Out
JTAGTMS	57	I	Test Mode Select
SMCLK	61	I	SMbus clock, Open Drain
SMDAT	62	I/O	SMbus data, Open Drain

Side Band signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBHPE1#	46	O	DP1 Power Enable
USBHPE2#	43	O	DP2 Power Enable
USBHPE3#	42	O	DP3 Power Enable
USBHPE4#	41	O	DP4 Power Enable
USBHOC1#	50	I	DP1 Over Current Indicator
USBHOC2#	49	I	DP2 Over Current Indicator
USBHOC3#	48	I	DP3 Over Current Indicator
USBHOC4#	47	I	DP4 Over Current Indicator
COREPWRDN#	51	O	Core power down
PEXRST#	60	I	System reset
SMI#	58	O	System Management Interrupt

Power and Ground

Pin Name	Pin #	I/O	Signal Description
GND	13	GND	Ground
VDD	23,36,53, 65,66,67,	PWR	1.0V Core power
VSUS33	44,45,54, 64	PWR	3.3V suspend power
VSUSUSB	1	PWR	1.0V suspend power

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Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
T_A	Ambient Temperature	0	70	°C	—
V_{Sus33}	3.3V Power Supply Voltage	-0.5	3.69	V	—
V_{DD}	Input Voltage	-0.5	1.1	V	—
V_{SUSUSB}	Input Voltage	-0.5	1.1	V	—
V_{ESD}	Electrostatic Discharge	—	2	kV	Human Body Model

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

DC Characteristics

Operating Conditions:
V_{DD} = 1.0 V±10%
V_{SUSUSB} = 1.0 V±10%
V_{SUS33} = 3.3V±10%
GND = 0V

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.50	0.8	V	—
V_{IH}	Input High Voltage	2.0	VCC+0.5	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=4.0mA
V_{OH}	Output High Voltage	2.4	—	V	IOH=-1.0mA
I_{IL}	Input Leakage Current	—	+/-10	µA	0<VIN<VCC
I_{OZ}	Tristate Leakage Current	—	+/-20	µA	0<VOUT<VCC

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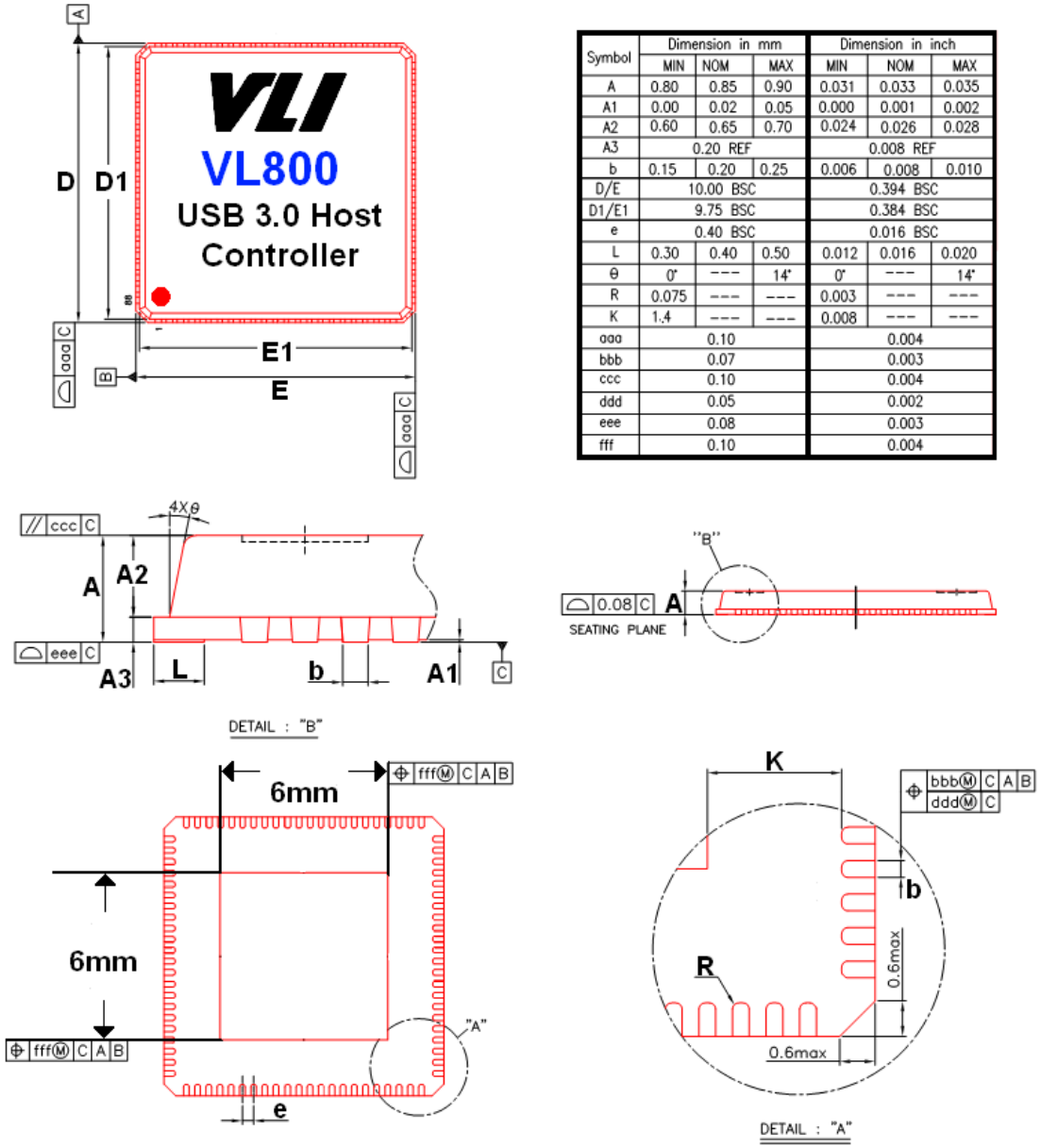
Package Mechanical Specifications

Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	10.00 BSC			0.394 BSC		
D1/E1	9.75 BSC			0.384 BSC		
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
K	1.4	---	---	0.008	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

Figure 3 – Mechanical Specification – QFN 88L 10x10x0.85 mm Package

Package Top Side Marking

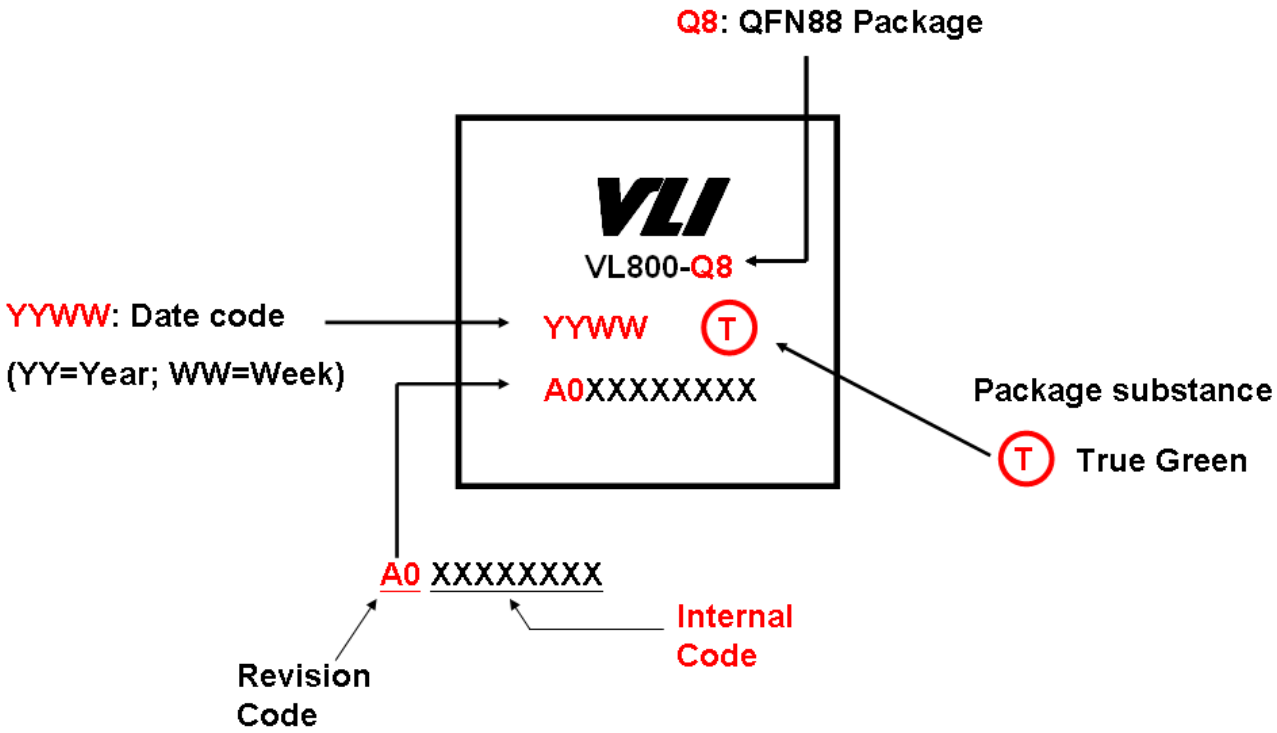


Figure 4 – Package Top Side Marking

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