SystemC & Behavior Coding

Assignment 6, 2025-11-27

Abstract

Remodel the Assignment 5 timer module with `SC_CTHREAD`.

Please read carefully. All outputs required are described in the text. Five (5) points will be taken for each bug, missing the required output and behavior.

The `SC_CTHREAD` timer module
Description

1. Remodel the Assignment 5 timer module with `SC_CTHREAD`, where `clock` pin is a positive-triggered clock port, and `start` pin is a synchronous active-high reset port.

sc_main
Description

1. Reuse the `main.cpp` implemented in Assignment 5.
2. Create a trace file named `RESULT.vcd`. And trace ports and the register `count` the same as in Assignment 5.

makefile
Description

A `makefile` must be provided with proper modifications to your environment.

Please submit the source code and `Makefile` only. Do not turn in the executable and waveform. Please try to utilize the code generator AI to generate the `timer` module. However, since GAI may not generate a correct `SC_CTHREAD` process, for this assignment, it may very well be much faster if you decide to code all by yourself.

Due date
3:00 PM, December 4, 2025

Score weight (towards the final grade)   5%