Alaska® 88E1510/88E1518/88E1512/ 88E1514 Datasheet

Integrated 10/100/1000 Mbps Energy Efficient Ethernet Transceiver

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CONFIDENTIAL

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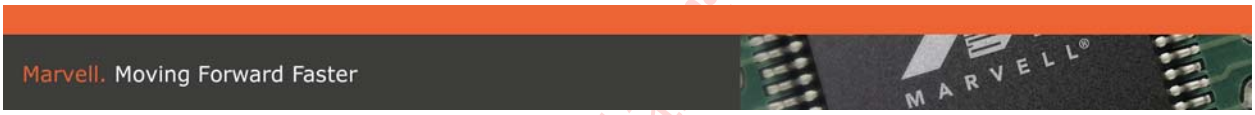


OVERVIEW

The Alaska® 88E1510/88E1518/88E1512/88E1514 device is a physical layer device containing a single 10/100/1000 Gigabit Ethernet transceiver. The transceiver implements the Ethernet physical layer portion of the 1000BASE-T, 100BASE-TX, and 10BASE-T standards. It is manufactured using standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 5 unshielded twisted pair.

The device supports the RGMII (Reduced pin count GMII) and SGMII for direct connection to a MAC/Switch port. The SGMII can also be used on media/line side to connect to SFP modules that support 1000BASE-X, 100BASE-FX and SGMII. It also supports Copper/Fiber Auto-media applications with RGMII as the MAC interface. SGMII operates at 1.25 Gbps over a single differential pair thus reducing power and number of I/Os used on the MAC interface.

The device integrates MDI interface termination resistors into the PHY. This resistor integration simplifies board layout and reduces board cost by reducing the number of external components. The new Marvell® calibrated resistor scheme will achieve and exceed the accuracy requirements of the IEEE 802.3 return loss specifications.

The device has an integrated switching voltage regulator to generate all required voltages. The device can run off a single 3.3V supply. The device supports 1.8V, 2.5V, and 3.3V LVCMOS I/O Standards.

The 88E1510/88E1518/88E1512/88E1514 device supports Synchronous Ethernet (SyncE) and Precise Timing Protocol (PTP) Time Stamping, which is based on IEEE1588 version 2 and IEEE802.1AS.

The 88E1510/88E1518/88E1512/88E1514 device supports IEEE 802.3az-2010 Energy Efficient Ethernet (EEE) and is IEEE 802.3az-2010 compliant.

The device incorporates the Marvell Advanced Virtual Cable Tester® (VCT™) feature, which uses Time Domain Reflectometry (TDR) technology for the remote identification of potential cable malfunctions, thus reducing equipment returns and service calls. Using VCT, the Alaska device detects and reports potential cabling issues such as pair swaps, pair polarity and excessive pair skew. The device will also detect cable opens, shorts or any impedance mismatch in the cable and reporting accurately within one meter the distance to the fault.

The device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The device achieves robust performance in noisy environments with very low power dissipation.

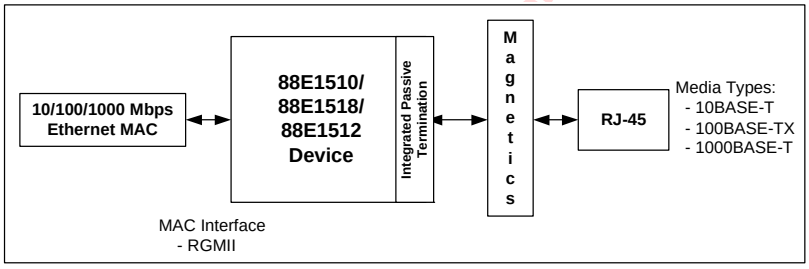
Features

- **10/100/1000BASE-T IEEE 802.3 compliant**
- **Multiple Operating Modes**
  - RGMII to Copper
  - SGMII to Copper (88E1512/88E1514 device only)
  - RGMII to Fiber/SGMII (88E1512 device only)
  - RGMII to Copper/Fiber/SGMII with Auto-Media Detect (88E1512 device only)
  - Copper to Fiber (1000BASE-X) (88E1512/88E1514)
- **Four RGMII timing modes including integrated delays - This eliminates the need for adding trace delays on the PCB**
- **Supports 1000BASE-X and 100BASE-FX on the Fiber interface along with SGMII**
- **Supports LVCMOS I/O Standards on the RGMII interface**
- **Supports Energy Efficient Ethernet (EEE) - IEEE 802.3az-2010 compliant**
  - EEE Buffering
  - Incorporates EEE buffering for seamless support of legacy MACs
- **Ultra Low Power**
- **Integrated MDI interface termination resistors that eliminate passive components**
- **Integrated Switching Voltage Regulators**

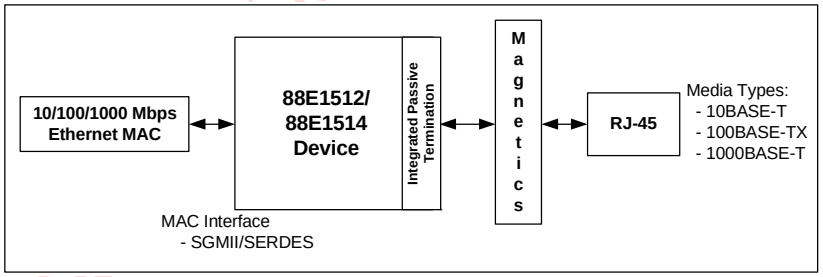
- **Supports Green Ethernet**
  - Active Power Save Mode
  - Energy Detect and Energy Detect+ low power modes
- **IEEE1588 version 2 Time Stamping**
- **Synchronous Ethernet (SyncE) Clock Recovery**
- **Three loopback modes for diagnostics**
- **"Downshift" mode for two-pair cable installations**
- **Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers**
- **Advanced digital baseline wander correction**
- **Automatic MDI/MDIX crossover at all speeds of operation**
- **Automatic polarity correction**
- **IEEE 802.3 compliant Auto-Negotiation**
- **Software programmable LED modes including LED testing**
- **MDC/XMDIO Management Interface**
- **CRC checker, packet counter**
- **Packet generation**
- **Wake on Lan (WOL) event detection**
- **Advanced Virtual Cable Tester® (VCT™)**
- **Auto-Calibration for MAC Interface outputs**
- **Temperature Sensor**
- **Supports single 3.3V supply when using internal switching regulator**
- **I/O pads can be supplied with 1.8V, 2.5V, or 3.3V**
- **Commercial grade, Industrial grade (88E1510 and 88E1512 only)**
- **48-Pin QFN 7 mm x 7 mm Green package with EPAD (88E1510 and 88E1518) and 56-Pin QFN 8 mm x 8 mm Green package with EPAD (88E1512/88E1514 device)**

Table 1: 88E1510/88E1518/88E1512/88E1514 Device Features

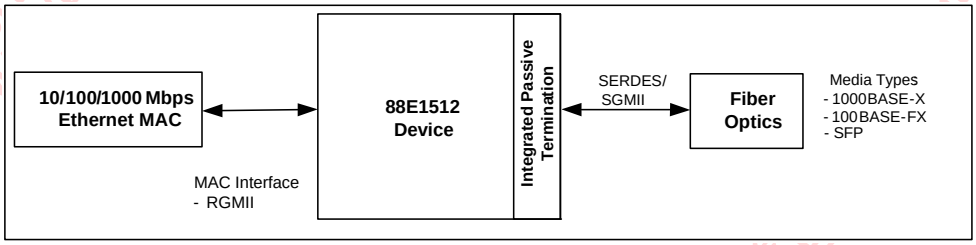
Features	88E1510	88E1518	88E1512	88E1514
RGMII to Copper	Yes	Yes	Yes	No
SGMII to Copper	No	No	Yes	Yes
RGMII to Fiber/SGMII	No	No	Yes	No
RGMII to Copper/Fiber/SGMII with Auto-Media Detect	No	No	Yes	No
Copper to Fiber	No	No	Yes	Yes
I/O Voltage (VDDO)	3.3V/2.5V	1.8V only	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V
IEEE 802.3az-2010 Energy Efficient Ethernet (EEE)	Yes	Yes	Yes	Yes
EEE Buffering	Yes	Yes	Yes	Yes
Synchronous Ethernet (SyncE)	Yes	Yes	Yes	Yes
Precise Timing Protocol (PTP)	Yes	Yes	Yes	Yes
Auto-Media Detect	No	No	Yes	No
Wake on LAN (WOL)	Yes	Yes	Yes	Yes
Package	48-pin QFN		56-pin QFN	
Industrial/Commercial Temperature	Commercial Industrial	Commercial	Commercial Industrial	Commercial



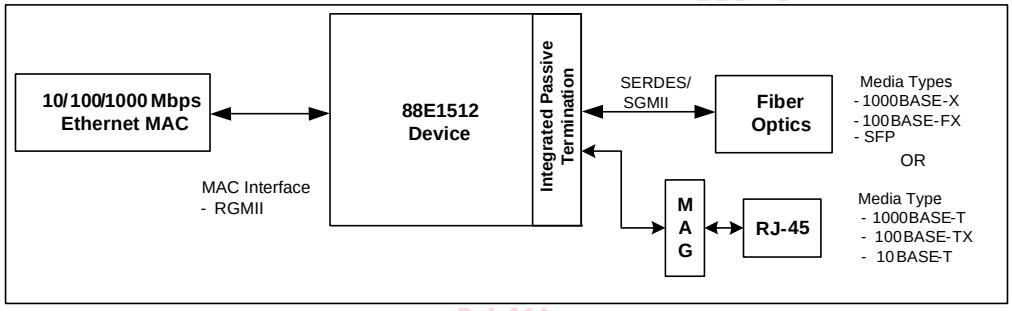
RGMII to Copper Device Application



SGMII to Copper Application



RGMII to Fiber/SGMII Application



RGMII to Copper/Fiber/SGMII Auto-Media Application

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1 Signal Description

1.1 Pin Description

Table 2: Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.1.1 88E1510/88E1518 48-Pin QFN Package Pinout

The 88E1510/88E1518 device is a 10/100/1000BASE-T Gigabit Ethernet transceiver.

Figure 1: 88E1510/88E1518 Device 48-Pin QFN Package (Top View)

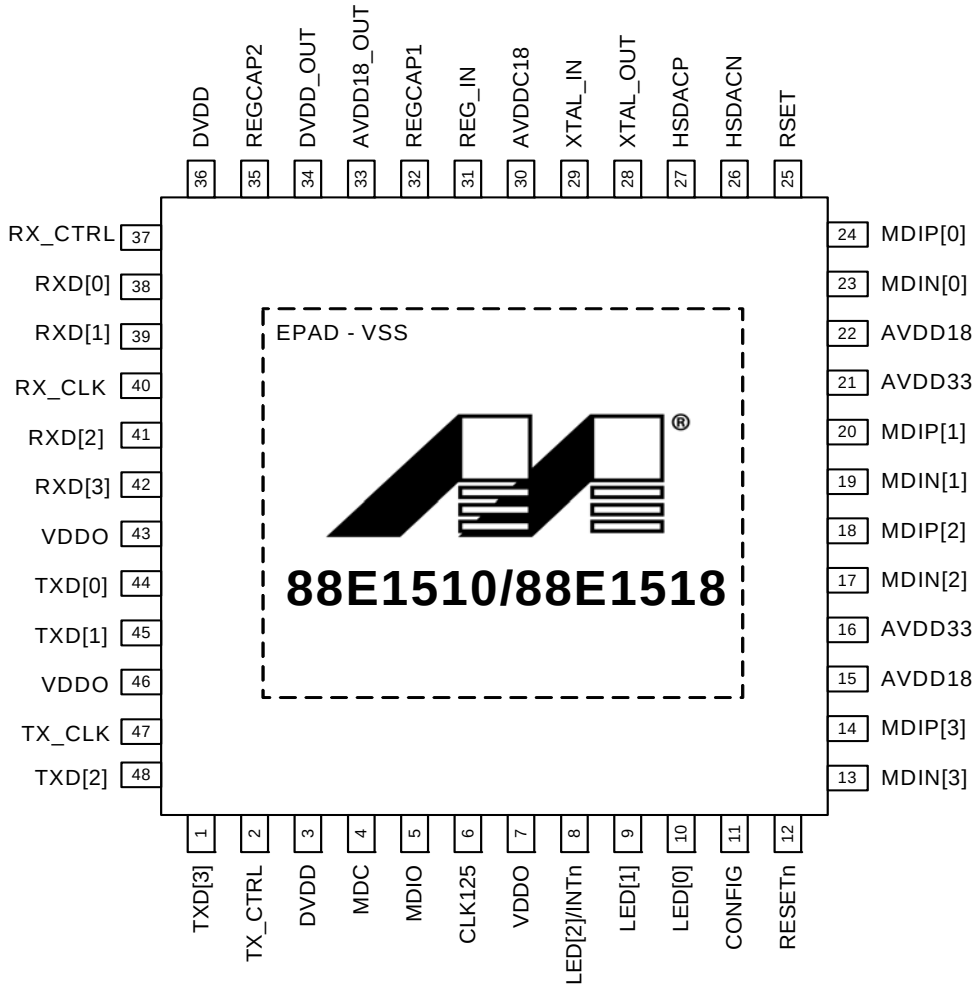


Table 3: Media Dependent Interface

48-QFN Pin #	Pin Name	Pin Type	Description
23 24	MDIN[0] MDIP[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIN/P[0] correspond to BI_DA±. In MDIX configuration, MDIN/P[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[0] are used for the transmit pair. In MDIX configuration, MDIN/P[0] are used for the receive pair. The device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
19 20	MDIN[1] MDIP[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIN/P[1] correspond to BI_DB±. In MDIX configuration, MDIN/P[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[1] are used for the receive pair. In MDIX configuration, MDIN/P[1] are used for the transmit pair. The device contains an internal 100 ohm resistor between the MDIP/N[1] pins.
17 18	MDIN[2] MDIP[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIN/P[2] correspond to BI_DC±. In MDIX configuration, MDIN/P[2] corresponds to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIN/P[2] are not used. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[2] pins.
13 14	MDIN[3] MDIP[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIN/P[3] correspond to BI_DD±. In MDIX configuration, MDIN/P[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIN/P[3] are not used. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[3] pins.

The RGMII interface supports 10/100/1000BASE-T modes of operation.

Table 4: RGMII Interface

48-QFN Pin #	Pin Name	Pin Type	Description
47	TX_CLK	I	RGMII Transmit Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance depending on speed.
2	TX_CTRL	I	RGMII Transmit Control. TX_EN is presented on the rising edge of TX_CLK. A logical derivative of TX_EN and TX_ER is presented on the falling edge of TX_CLK.
1 48 45 44	TXD[3] TXD[2] TXD[1] TXD[0]	I	RGMII Transmit Data. TXD[3:0] run at double data rate with bits [3:0] of each byte to be transmitted on the rising edge of TX_CLK, and bits [7:4] presented on the falling edge of TX_CLK. In 10/100BASE-T modes, the transmit data nibble is presented on TXD[3:0] on the rising edge of TX_CLK.
40	RX_CLK	O	RGMII Receive Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance derived from the received data stream depending on speed.
37	RX_CTRL	O	RGMII Receive Control. RX_DV is presented on the rising edge of RX_CLK. A logical derivative of RX_DV and RX_ER is presented on the falling edge of RX_CLK.
42 41 39 38	RXD[3] RXD[2] RXD[1] RXD[0]	O	RGMII Receive Data. RXD[3:0] run at double data rate with bits [3:0] of each byte received on the rising edge of RX_CLK, and bits [7:4] presented on the falling edge of RX_CLK. In 10/100BASE-T modes, the receive data nibble is presented on RXD[3:0] on the rising edge of RX_CLK.

Table 5: Management Interface and Interrupt

48-QFN Pin #	Pin Name	Pin Type	Description
4	MDC	I	MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12 MHz.
5	MDIO	I/O	MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.

Table 6: LED Interface

48-QFN Pin #	Pin Name	Pin Type	Description
10	LED[0]	O	LED output.
9	LED[1]	I/O	LED output/PTP Event Request Input/PTP Trigger Generate Response Output. LED[1] can be configured as PTP Event Request Input or PTP Trigger Generate Response Output. Refer to 2.28 "Precise Timing Protocol (PTP) Time Stamping Support" on page 90 for further details.
8	LED[2]/INTn	O, D	LED/Interrupt outputs. LED[2] pin also functions as an active low interrupt pin.

Table 7: Clock/Configuration/Reset/I/O

48-QFN Pin #	Pin Name	Pin Type	Description
11	CONFIG	I	Hardware Configuration.
6	CLK125	O	125 MHz Clock Output or SyncE Recovered Clock Output. See Section 2.28 CLK125 for more details.
29	XTAL_IN	I	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference or oscillator input. **NOTE:** The XTAL_IN pin is not 2.5V/3.3V tolerant. Refer to 'Oscillator level shifting' application note to convert a 2.5V/3.3V clock source to 1.8V clock.
28	XTAL_OUT	O	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected, it should be left floating.
12	RESETn	I	Hardware reset. Active low. 0 = Reset 1 = Normal operation

Table 8: Control and Reference

48-QFN Pin #	Pin Name	Pin Type	Description
25	RSET	I	Constant voltage reference. External 4.99 kohm 1% resistor connection to VSS is required for this pin.

Table 9: Test

48-QFN Pin #	Pin Name	Pin Type	Description
26 27	HSDACN HSDACP	Analog O	Test Pins. These pins are used to bring out a differential TX_TCLK. Connect these pins with a 50 ohm termination resistor to VSS for IEEE testing. If IEEE testing is not important, these pins may be left floating.

Table 10: Power, Ground & Internal Regulators

48-QFN Pin #	Pin Name	Pin Type	Description
30	AVDDC18	Power	Analog supply - 1.8V[1]. AVDDC18 can be supplied externally with 1.8V, or via the 1.8V internal regulator.
15 22	AVDD18	Power	Analog supply - 1.8V. AVDD18 can be supplied externally with 1.8V, or via the 1.8V internal regulator.
16 21	AVDD33	Power	Analog Supply - 3.3V.
31	REG_IN	Power	Analog Supply for the internal regulator – 3.3V. If the internal regulator is not used, this pin must be left open – No connect. **NOTE:** For further details on pin connections, refer to the Section 2.34 "Regulators and Power Supplies" on page 104. **NOTE:** Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device.
32 35	REGCAP1 REGCAP2		Capacitor terminal pins for the internal regulator. Connect a 220 nF ± 10% ceramic capacitor between REGCAP1 and REGCAP2 on the board and place it close to the device. If the internal regulator is not used, these pins must be left open (no connect). Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will permanently damage the device.
33	AVDD18_OUT	Power	Regulator output - 1.8V. If the internal regulator is used, this pin must be connected to 1.8V power plane that connected to AVDD18 and AVDDC18. If the external supply is used, this pin must be left open (no-connect).
34	DVDD_OUT	Power	Regulator output - 1.0V. If the internal regulator is used, this pin must be connected to 1.0V power plane that connected to DVDD. If the external supply is used, this pin must be left open (no-connect).
7 43 46	VDDO	Power	3.3V or 2.5V or 1.8V[2] digital I/O supply[3]. VDDO must be supplied externally if 2.5V or 3.3V is desired. For VDDO 1.8V operation the 1.8V regulator output can be used.

Table 10: Power, Ground (Continued)& Internal Regulators

48-QFN Pin #	Pin Name	Pin Type	Description
3 36	DVDD	Power	Digital core supply - 1.0V. DVDD can be supplied externally with 1.0V or via the 1.0V internal regulator.
Epad	VSS	GND	Ground to device. The 48-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD.

1. AVDDC18 supplies the XTAL_IN and XTAL_OUT pins.

2. For 1.8V VDDO operations, refer to the Part Ordering section for the ordering information.

3. VDDO supplies the MDC, MDIO, RESETn, LED[2:0], CONFIG, CLK125, and the RGMII pins.

1.1.2 88E1512 56-Pin QFN Package Pinout

The 88E1512 device is a 10/100/1000BASE-T Gigabit Ethernet transceiver.

Figure 2: 88E1512 Device 56-Pin QFN Package (Top View)

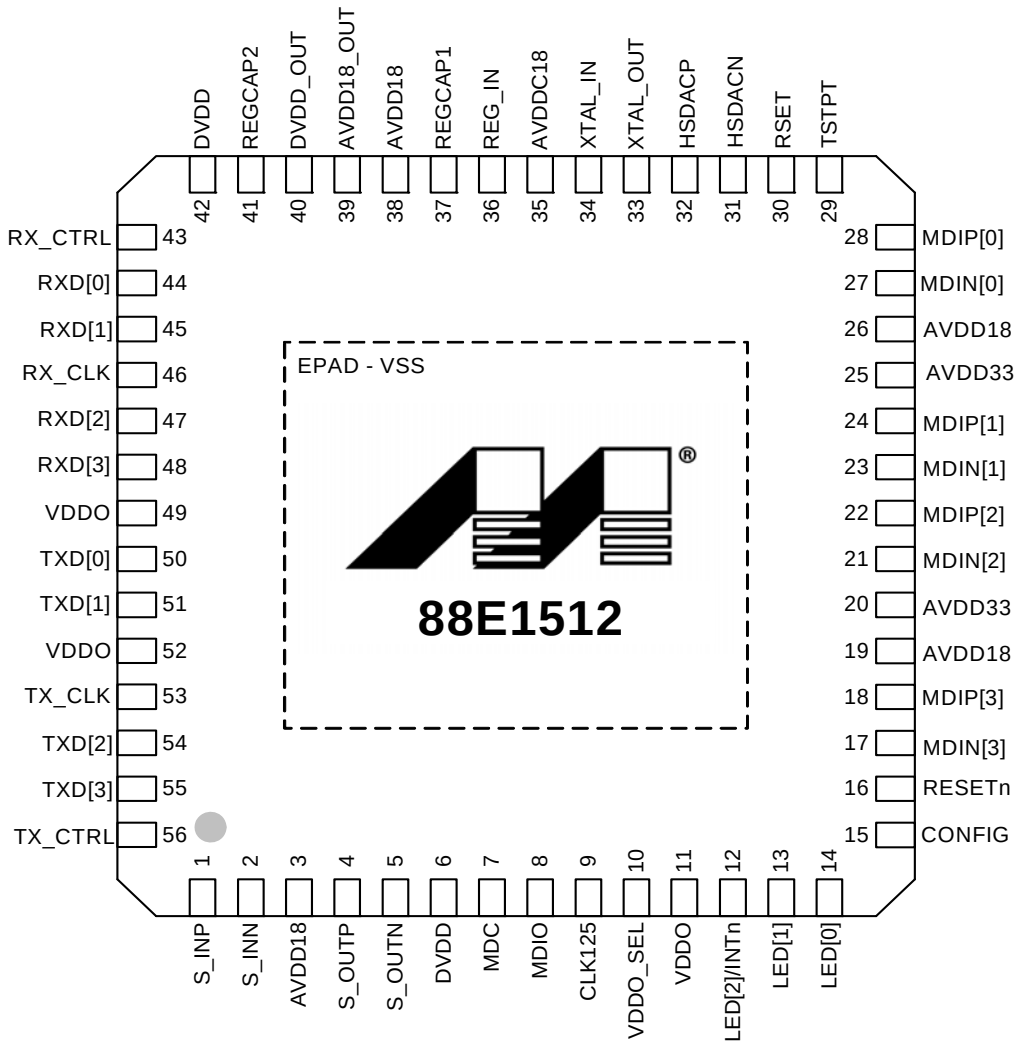


Table 11: Media Dependent Interface

56-QFN Pin #	Pin Name	Pin Type	Description
27 28	MDIN[0] MDIP[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIN/P[0] correspond to BI_DA±. In MDIX configuration, MDIN/P[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[0] are used for the transmit pair. In MDIX configuration, MDIN/P[0] are used for the receive pair. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
23 24	MDIN[1] MDIP[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIN/P[1] correspond to BI_DB±. In MDIX configuration, MDIN/P[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[1] are used for the receive pair. In MDIX configuration, MDIN/P[1] are used for the transmit pair. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[1] pins.

Table 11: Media Dependent Interface (Continued)

56-QFN Pin #	Pin Name	Pin Type	Description
21 22	MDIN[2] MDIP[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIN/P[2] correspond to BI_DC±. In MDIX configuration, MDIN/P[2] corresponds to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIN/P[2] are not used. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[2] pins.
17 18	MDIN[3] MDIP[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIN/P[3] correspond to BI_DD±. In MDIX configuration, MDIN/P[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIN/P[3] are not used. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[3] pins.

Table 12: RGMII Interface

56-QFN Pin #	Pin Name	Pin Type	Description
53	TX_CLK	I	RGMII Transmit Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance depending on speed.
56	TX_CTRL	I	RGMII Transmit Control. TX_EN is presented on the rising edge of TX_CLK. A logical derivative of TX_EN and TX_ER is presented on the falling edge of TX_CLK.
55 54 51 50	TXD[3] TXD[2] TXD[1] TXD[0]	I	RGMII Transmit Data. TXD[3:0] run at double data rate with bits [3:0] of each byte to be transmitted on the rising edge of TX_CLK, and bits [7:4] presented on the falling edge of TX_CLK. In 10/100BASE-T modes, the transmit data nibble is presented on TXD[3:0] on the rising edge of TX_CLK.
46	RX_CLK	O	RGMII Receive Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance derived from the received data stream depending on speed.

Table 12: RGMII Interface (Continued)

56-QFN Pin #	Pin Name	Pin Type	Description
43	RX_CTRL	O	RGMII Receive Control. RX_DV is presented on the rising edge of RX_CLK. A logical derivative of RX_DV and RX_ER is presented on the falling edge of RX_CLK.
48 47 45 44	RXD[3] RXD[2] RXD[1] RXD[0]	O	RGMII Receive Data. RXD[3:0] run at double data rate with bits [3:0] of each byte received on the rising edge of RX_CLK, and bits [7:4] presented on the falling edge of RX_CLK. In 10/100BASE-T modes, the receive data nibble is presented on RXD[3:0] on the rising edge of RX_CLK.

Table 13: Management Interface and Interrupt

56-QFN Pin #	Pin Name	Pin Type	Description
7	MDC	I	MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12 MHz.
8	MDIO	I/O	MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.

Table 14: LED Interface

56-QFN Pin #	Pin Name	Pin Type	Description
14	LED[0]	O	LED output.
13	LED[1]	I/O	LED output/PTP Event Request Input/PTP Trigger Generate Response Output. LED[1] can be configured as PTP Event Request Input or PTP Trigger Generate Response Output. Refer to 2.28 "Precise Timing Protocol (PTP) Time Stamping Support" on page 90 for further details.
12	LED[2]/INTn	O, D	LED/Interrupt outputs. LED[2] pin also functions as an active low interrupt pin.

Table 15: Clock/Configuration/Reset/I/O

56-QFN Pin #	Pin Name	Pin Type	Description
15	CONFIG	I	Hardware Configuration.
9	CLK125	O	125 MHz Clock Output or SyncE Recovered Clock Output. Refer to Section 2.28 for details.
34	XTAL_IN	I	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference or oscillator input. **NOTE:** The XTAL_IN pin is not 2.5V/3.3V tolerant. Refer to 'Oscillator level shifting' application note to convert a 2.5V/3.3V clock source to 1.8V clock.
33	XTAL_OUT	O	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected, it should be left floating.
16	RESETn	I	Hardware reset. Active low. 0 = Reset 1 = Normal operation

Table 16: SGMII I/Os

56-QFN Pin #	Pin Name	Pin Type	Description
2 1	S_INN S_INP	I	SGMII Receive Data. 1.25 GBaud input - Positive and Negative.
5 4	S_OUTN S_OUTP	O	SGMII Transmit Data. 1.25 GBaud output - Positive and Negative.

Table 17: Control and Reference

56-QFN Pin #	Pin Name	Pin Type	Description
30	RSET	I	Constant voltage reference. External 4.99 kohm 1% resistor connection to VSS is required for this pin.

Table 18: Test

56-QFN Pin #	Pin Name	Pin Type	Description
31 32	HSDACN HSDACP	Analog O	Test Pins. These pins are used to bring out a differential TX_TCLK. Connect these pins with a 50 ohm termination resistor to VSS for IEEE testing. If IEEE testing are not important, these pins may be left floating.
29	TSTPT	O	DC Test Point. The TSTPT pin should be left floating.

Table 19: Power, Ground, and Internal Regulators

56-QFN Pin #	Pin Name	Pin Type	Description
35	AVDDC18	Power	Analog supply - 1.8V[1]. AVDDC18 can be supplied externally with 1.8V, or via the 1.8V internal regulator.
3 19 26 38	AVDD18	Power	Analog supply - 1.8V. AVDD18 can be supplied externally with 1.8V, or via the 1.8V internal regulator.
20 25	AVDD33	Power	Analog Supply - 3.3V.
36	REG_IN	Power	Analog Supply for the internal regulator – 3.3V. If the internal regulator is not used, this pin must be left open – No connect. **NOTE:** For further details on pin connections, refer to the Section 2.34 "Regulators and Power Supplies" on page 104. **NOTE:** Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device.

Table 19: Power, Ground, and Internal Regulators

56-QFN Pin #	Pin Name	Pin Type	Description
37 41	REGCAP1 REGCAP2		Capacitor terminal pins for the internal regulator. Connect a 220 nF ± 10% ceramic capacitor between REGCAP1 and REGCAP2 on the board and place it close to the device. If the internal regulator is not used, these pins must be left open (no connect). **NOTE:** Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device.
39	AVDD18_OUT	Power	Regulator output - 1.8V. If the internal regulator is used, this pin must be connected to 1.8V power plane that connected to AVDD18 and AVDDC18. If the external supply is used, this pin must be left open (no-connect).
40	DVDD_OUT	Power	Regulator output - 1.0V. If the internal regulator is used, this pin must be connected to 1.0V power plane that connected to DVDD. If the external supply is used, this pin must be left open (no-connect).
11 49 52	VDDO	Power	3.3V or 2.5V or 1.8V digital I/O supply[2]. See VDDO_SEL for further details. VDDO must be supplied externally when 3.3V or 2.5V is used. For 1.8V operation, the 1.8V regulator output can be used.
10	VDDO_SEL	Power	VDDO Voltage Control. For VDDO 2.5V/3.3V operation, VDDO_SEL must be tied to VSS. For VDDO 1.8V operation, VDDO_SEL must be tied to VDDO.
6 42	DVDD	Power	Digital core supply - 1.0V. DVDD can be supplied externally with 1.0V or via the 1.0V internal regulator.
EPAD	VSS	GND	Ground to device. The 56-pin QFN package has an exposed die pad (E-PAD) at its base. This EPAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD.

1. AVDDC18 supplies the XTAL_IN and XTAL_OUT pins.
2. VDDO supplies the MDC, MDIO, RESETn, LED[2:0], CONFIG, CLK125, VDDO_SEL, and the RGMII pins.

1.1.3 88E1514 56-Pin QFN Package Pinout

The 88E1514 device is a 10/100/1000BASE-T Gigabit Ethernet transceiver.

Figure 3: 88E1514 Device 56-Pin QFN Package (Top View)

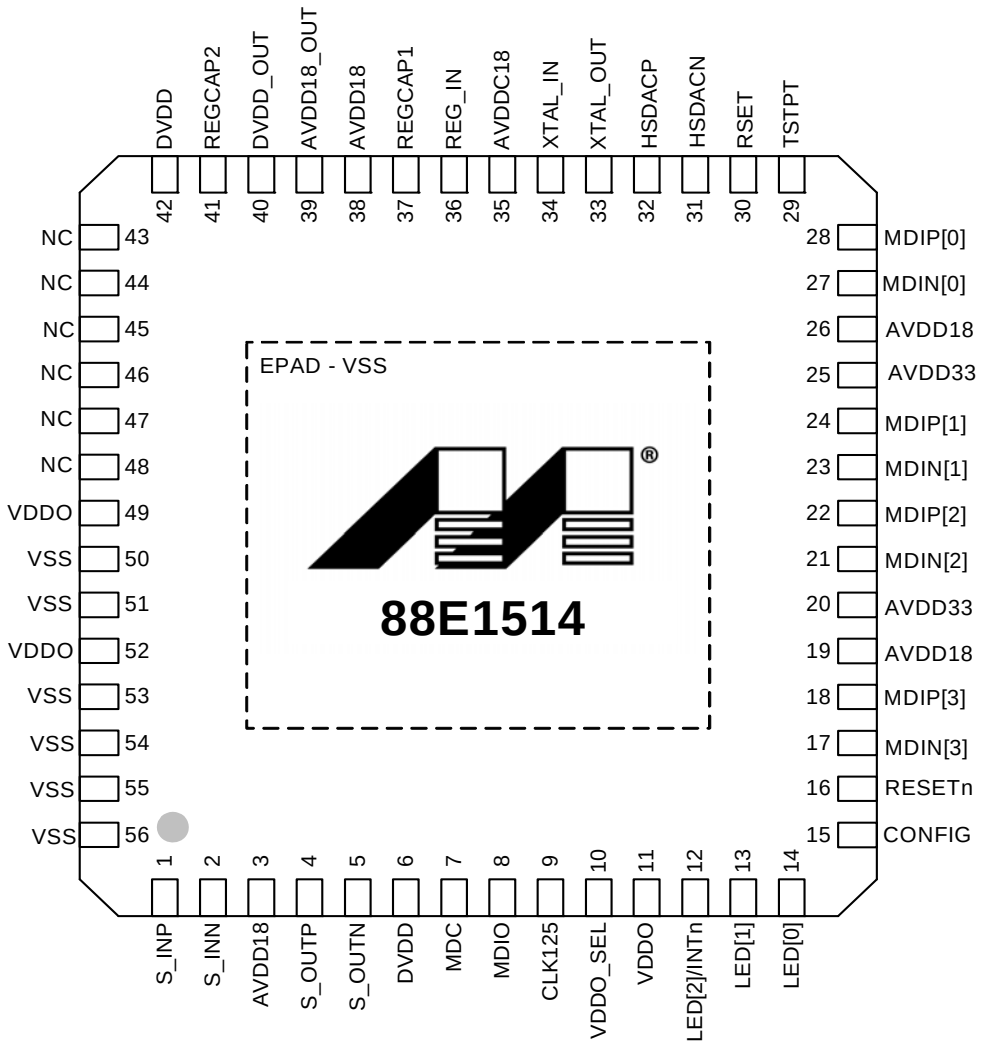


Table 20: Media Dependent Interface

56-QFN Pin #	Pin Name	Pin Type	Description
27 28	MDIN[0] MDIP[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIN/P[0] correspond to BI_DA±. In MDIX configuration, MDIN/P[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[0] are used for the transmit pair. In MDIX configuration, MDIN/P[0] are used for the receive pair. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
23 24	MDIN[1] MDIP[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIN/P[1] correspond to BI_DB±. In MDIX configuration, MDIN/P[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[1] are used for the receive pair. In MDIX configuration, MDIN/P[1] are used for the transmit pair. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[1] pins.

Table 20: Media Dependent Interface (Continued)

56-QFN Pin #	Pin Name	Pin Type	Description
21 22	MDIN[2] MDIP[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIN/P[2] correspond to BI_DC±. In MDIX configuration, MDIN/P[2] corresponds to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIN/P[2] are not used. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[2] pins.
17 18	MDIN[3] MDIP[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIN/P[3] correspond to BI_DD±. In MDIX configuration, MDIN/P[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIN/P[3] are not used. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[3] pins.

Table 21: Management Interface and Interrupt

56-QFN Pin #	Pin Name	Pin Type	Description
7	MDC	I	MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12 MHz.
8	MDIO	I/O	MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.

Table 22: LED Interface

56-QFN Pin #	Pin Name	Pin Type	Description
14	LED[0]	O	LED output.
13	LED[1]	I/O	LED output/PTP Event Request Input/PTP Trigger Generate Response Output. LED[1] can be configured as PTP Event Request Input or PTP Trigger Generate Response Output. Refer to 2.28 "Precise Timing Protocol (PTP) Time Stamping Support" on page 90 for further details.
12	LED[2]/INTn	O, D	LED/Interrupt outputs. LED[2] pin also functions as an active low interrupt pin.

Table 23: Clock/Configuration/Reset/I/O

56-QFN Pin #	Pin Name	Pin Type	Description
15	CONFIG	I	Hardware Configuration.
9	CLK125	O	125 MHz Clock Output or SyncE Recovered Clock Output. Refer to Section 2.28 for details.
34	XTAL_IN	I	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference or oscillator input. **NOTE:** The XTAL_IN pin is not 2.5V/3.3V tolerant. Refer to 'Oscillator level shifting' application note to convert a 2.5V/3.3V clock source to 1.8V clock.
33	XTAL_OUT	O	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected, it should be left floating.
16	RESETn	I	Hardware reset. Active low. 0 = Reset 1 = Normal operation

Table 24: SGMII I/Os

56-QFN Pin #	Pin Name	Pin Type	Description
2 1	S_INN S_INP	I	SGMII Receive Data. 1.25 GBaud input - Positive and Negative.
5 4	S_OUTN S_OUTP	O	SGMII Transmit Data. 1.25 GBaud output - Positive and Negative.

Table 25: Control and Reference

56-QFN Pin #	Pin Name	Pin Type	Description
30	RSET	I	Constant voltage reference. External 4.99 kohm 1% resistor connection to VSS is required for this pin.

Table 26: Test

56-QFN Pin #	Pin Name	Pin Type	Description
31 32	HSDACN HSDACP	Analog O	Test Pins. These pins are used to bring out a differential TX_TCLK. Connect these pins with a 50 ohm termination resistor to VSS for IEEE testing g. If IEEE testing are not important, these pins may be left floating.
29	TSTPT	O	DC Test Point. The TSTPT pin should be left floating.

Table 27: Power, Ground, and Internal Regulators

56-QFN Pin #	Pin Name	Pin Type	Description
35	AVDDC18	Power	Analog supply - 1.8V[1]. AVDDC18 can be supplied externally with 1.8V, or via the 1.8V internal regulator.
3 19 26 38	AVDD18	Power	Analog supply - 1.8V. AVDD18 can be supplied externally with 1.8V, or via the 1.8V internal regulator.
20 25	AVDD33	Power	Analog Supply - 3.3V.
36	REG_IN	Power	Analog Supply for the internal regulator – 3.3V. If the internal regulator is not used, this pin must be left open – No connect. **NOTE:** For further details on pin connections, refer to the Section 2.34 "Regulators and Power Supplies" on page 104. **NOTE:** Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device.
37 41	REGCAP1 REGCAP2		Capacitor terminal pins for the internal regulator. Connect a 220 nF ± 10% ceramic capacitor between REGCAP1 and REGCAP2 on the board and place it close to the device. If the internal regulator is not used, these pins must be left open (no connect). **NOTE:** Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device.

Table 27: Power, Ground, and Internal Regulators

56-QFN Pin #	Pin Name	Pin Type	Description
39	AVDD18_OUT	Power	Regulator output - 1.8V. If the internal regulator is used, this pin must be connected to 1.8V power plane that connected to AVDD18 and AVDDC18. If the external supply is used, this pin must be left open (no-connect).
40	DVDD_OUT	Power	Regulator output - 1.0V. If the internal regulator is used, this pin must be connected to 1.0V power plane that connected to DVDD. If the external supply is used, this pin must be left open (no-connect).
11 49 52	VDDO	Power	3.3V or 2.5V or 1.8V digital I/O supply[2]. See VDDO_SEL for further details. VDDO must be supplied externally when 3.3V or 2.5V is used. For 1.8V operation, the 1.8V regulator output can be used.
10	VDDO_SEL	Power	VDDO Voltage Control. For VDDO 2.5V/3.3V operation, VDDO_SEL must be tied to VSS. For VDDO 1.8V operation, VDDO_SEL must be tied to VDDO.
6 42	DVDD	Power	Digital core supply - 1.0V. DVDD can be supplied externally with 1.0V or via the 1.0V internal regulator.
50 51 53 54 55 56	VSS	GND	These pins must be tied to the GND.
EPAD	VSS	GND	Ground to device. The 56-pin QFN package has an exposed die pad (E-PAD) at its base. This EPAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD.

1. AVDDC18 supplies the XTAL_IN and XTAL_OUT pins.
2. VDDO supplies the MDC, MDIO, RESETn, LED[2:0], CONFIG, CLK125, VDDO_SEL, and the RGMII pins.

Table 28: No Connect

56-QFN Pin #	Pin Name	Pin Type	Description
43 44 45 46 47 48	NC	--	These pins must be left floating.

1.2 Pin Assignment List

1.2.1 88E1510 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
33	AVDD18_OUT	18	MDIP[2]
15	AVDD18	14	MDIP[3]
22	AVDD18	32	REGCAP1
30	AVDDC18	35	REGCAP2
16	AVDD33	31	REG_IN
21	AVDD33	40	RX_CLK
6	CLK125	37	RX_CTRL
11	CONFIG	12	RESETn
3	DVDD	25	RSET
36	DVDD	38	RXD[0]
34	DVDD_OUT	39	RXD[1]
26	HSDACN	41	RXD[2]
27	HSDACP	42	RXD[3]
10	LED[0]	47	TX_CLK
9	LED[1]	2	TX_CTRL
8	LED[2]/INTn	44	TXD[0]
4	MDC	45	TXD[1]
23	MDIN[0]	48	TXD[2]
19	MDIN[1]	1	TXD[3]
17	MDIN[2]	7	VDDO
13	MDIN[3]	43	VDDO
5	MDIO	46	VDDO
24	MDIP[0]	29	XTAL_IN
20	MDIP[1]	28	XTAL_OUT

1.2.2 88E1518 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
33	AVDD18_OUT	18	MDIP[2]
15	AVDD18	14	MDIP[3]
22	AVDD18	32	REGCAP1
30	AVDDC18	35	REGCAP2
16	AVDD33	31	REG_IN
21	AVDD33	40	RX_CLK
6	CLK125	37	RX_CTRL
11	CONFIG	12	RESETn
3	DVDD	25	RSET
36	DVDD	38	RXD[0]
34	DVDD_OUT	39	RXD[1]
26	HSDACN	41	RXD[2]
27	HSDACP	42	RXD[3]
10	LED[0]	47	TX_CLK
9	LED[1]	2	TX_CTRL
8	LED[2]/INTn	44	TXD[0]
4	MDC	45	TXD[1]
23	MDIN[0]	48	TXD[2]
19	MDIN[1]	1	TXD[3]
17	MDIN[2]	7	VDDO
13	MDIN[3]	43	VDDO
5	MDIO	46	VDDO
24	MDIP[0]	29	XTAL_IN
20	MDIP[1]	28	XTAL_OUT

1.2.3 88E1512 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
39	AVDD18_OUT	37	REGCAP1
3	AVDD18	41	REGCAP2
19	AVDD18	36	REG_IN
26	AVDD18	46	RX_CLK
38	AVDD18	43	RX_CTRL
35	AVDDC18	16	RESETn
20	AVDD33	30	RSET
25	AVDD33	44	RXD[0]
9	CLK125	45	RXD[1]
15	CONFIG	47	RXD[2]
6	DVDD	48	RXD[3]
40	DVDD_OUT	2	S_INN
42	DVDD	1	S_INP
31	HSDACN	5	S_OUTN
32	HSDACP	4	S_OUTP
14	LED[0]	29	TSTPT
13	LED[1]	53	TX_CLK
12	LED[2]/INTn	56	TX_CTRL
7	MDC	50	TXD[0]
27	MDIN[0]	51	TXD[1]
23	MDIN[1]	54	TXD[2]
21	MDIN[2]	55	TXD[3]
17	MDIN[3]	11	VDDO
8	MDIO	49	VDDO
28	MDIP[0]	52	VDDO
24	MDIP[1]	10	VDDO_SEL
22	MDIP[2]	34	XTAL_IN
18	MDIP[3]	33	XTAL_OUT

1.2.4 88E1514 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name

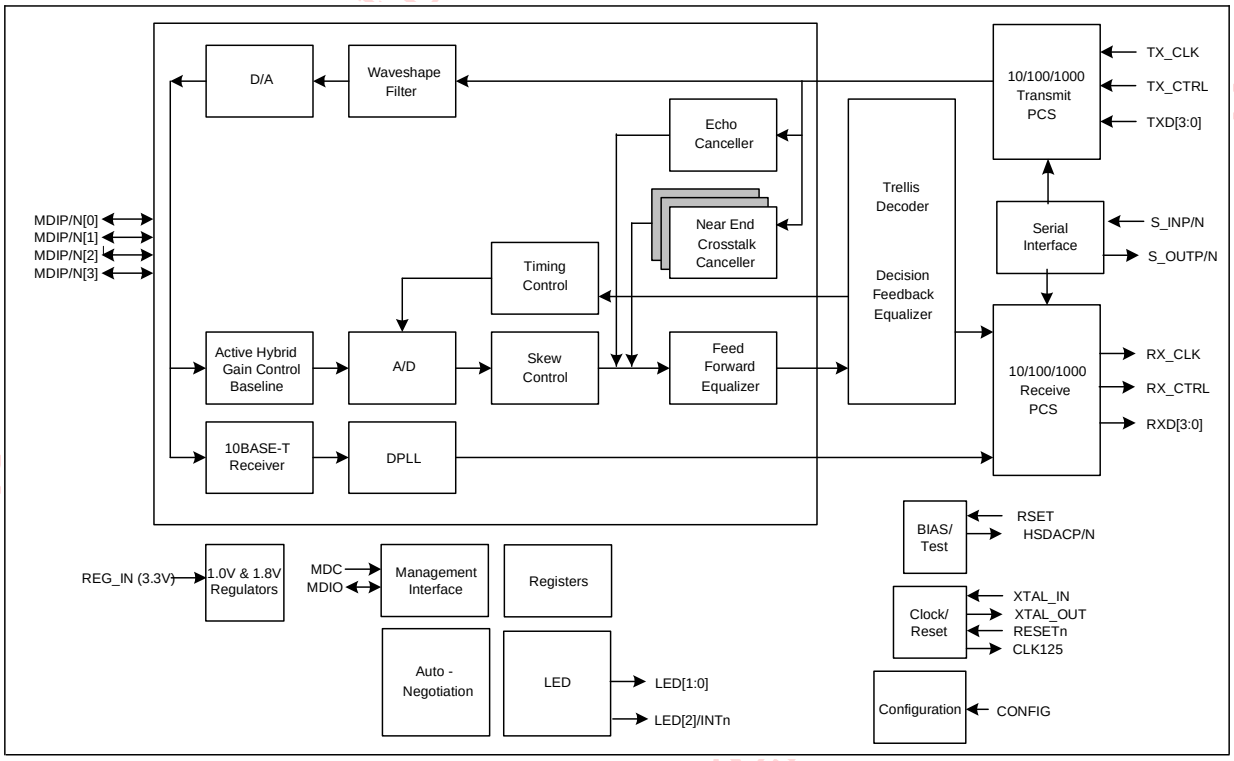
Pin #	Pin Name	Pin #	Pin Name
39	AVDD18_OUT	43	NC
3	AVDD18	44	NC
19	AVDD18	45	NC
26	AVDD18	46	NC
38	AVDD18	47	NC
35	AVDDC18	48	NC
20	AVDD33	16	RESETn
25	AVDD33	30	RSET
9	CLK125	37	REGCAP1
15	CONFIG	41	REGCAP2
6	DVDD	36	REG_IN
40	DVDD_OUT	2	S_INN
42	DVDD	1	S_INP
31	HSDACN	5	S_OUTN
32	HSDACP	4	S_OUTP
14	LED[0]	29	TSTPT
13	LED[1]	11	VDDO
12	LED[2]/INTn	49	VDDO
7	MDC	52	VDDO
27	MDIN[0]	10	VDDO_SEL
23	MDIN[1]	53	VSS
21	MDIN[2]	56	VSS
17	MDIN[3]	50	VSS
8	MDIO	51	VSS
28	MDIP[0]	54	VSS
24	MDIP[1]	55	VSS
22	MDIP[2]	34	XTAL_IN
18	MDIP[3]	33	XTAL_OUT

2 PHY Functional Specifications

The device is a single-port 10/100/1000 Gigabit Ethernet transceiver. Figure 4 shows the functional block diagram of the device.

Note Refer to Overview for a list of features supported by the device.

Figure 4: Device Functional Block Diagram



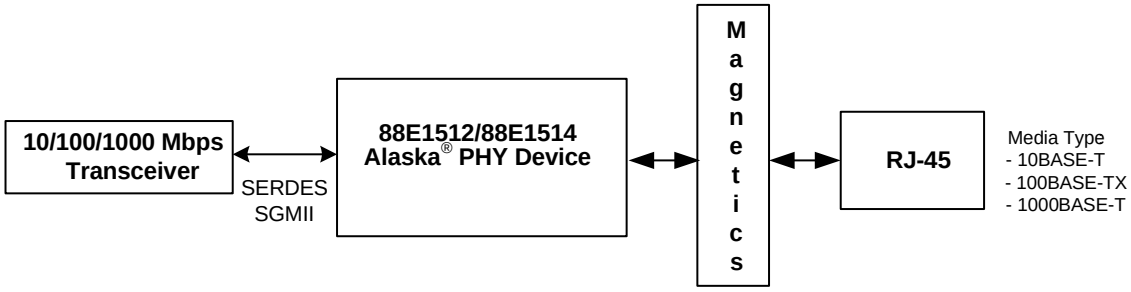
2.1 Modes of Operation and Major Interfaces

The device has three separate major electrical interfaces:

- MDI Interface to Copper Cable (88E1510/88E1518/88E1512/88E1514 devices)
- SERDES/SGMII Interface (88E1512/88E1514 device only)
- RGMII Interface (88E1510/88E1518/88E1512 devices)

The MDI Interface is always a media interface. The RGMII interface is always a system interface. The SGMII interface can either be a system interface, or a media interface. (The system interface is also known as MAC interface. It is typically the connection between the PHY and the MAC or the system ASIC). The block diagrams describing the different applications of the 88E1510/88E1518/88E1512/88E1514 devices can be found below.

Figure 5: 88E1512/88E1514 SGMII/SERDES System to Copper Media Interface Example



The 88E1512/88E1514 device can be used in media conversion applications which require a conversion from 1000BASE-T to 1000BASE-X provided the 1000BASE-X auto negotiation is disabled on both the upstream device and 88E1512/88E1514. 88E1512/88E1514 device in this application must be configured to operate in SGMII to Copper(MODE[2:0]=001) for the conversion with the SGMII Auto-Negotiation disabled through Register 0_1.12=0.

When used as a system interface, the device implements the PHY SGMII Auto-Negotiation status (link, duplex, etc.) advertisements as specified in the Cisco SGMII specification. The system interface replicates the speed and duplex setting of the media interface

When used as a Media interface, the device implements the MAC SGMII Auto-Negotiation function, which monitors PHY status advertisements

For details of how SGMII Auto-Negotiation operates, see Section 2.10.3 as well as the Cisco SGMII specification 1.8.

Figure 6: 88E1510/88E1518 RGMII System to Copper Interface Example

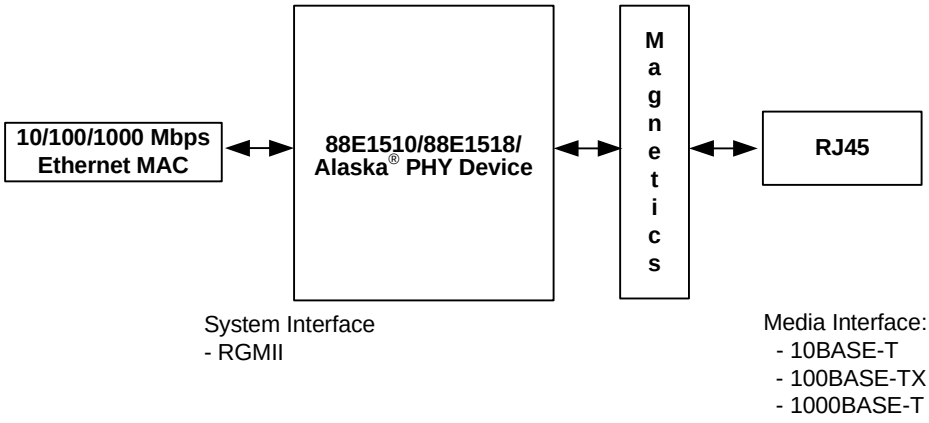
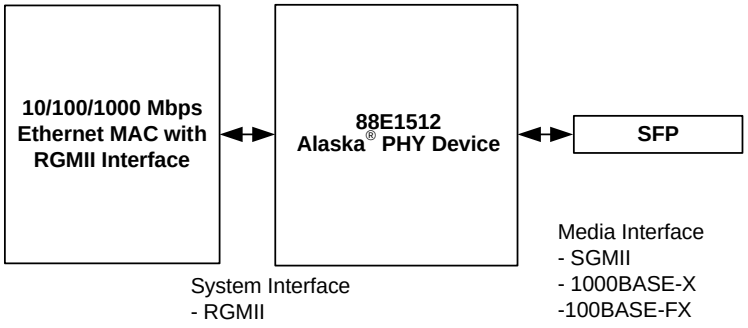


Figure 7: 88E1512 RGMII System to SERDES Interface Example



The 88E1512 device supports 7 modes of operation as shown in Table 29. On hardware reset the 88E1512 device, by default is configured to RGMII (System mode) to Auto media detect (Copper/1000BASE-X). For modes of operation supported by 88E1510, 88E1518, 88E1514, refer to Table 1.

The behavior of the 1.25 GHz SERDES interface is selected by setting the MODE[2:0] register in 20_18.2:0. The SERDES can operate in 100BASE-FX, 1000BASE-X, SGMII (System), and SGMII (Media).

Table 29: MODE[2:0] Select

MODE[2:0] Register 20_18.2:0	Description
000	RGMII (System mode) to Copper
001	SGMII (System mode) to Copper
010	RGMII (System mode) to 1000BASE-X
011	RGMII (System mode) to 100BASE-FX OR RGMII (System mode) to Auto Media Detect Copper/100BASE-FX (when 20_18.6 = 1)
100	RGMII (System mode) to SGMII (Media mode)

Table 29: MODE[2:0] Select (Continued)

MODE[2:0] Register 20_18.2:0	Description
101	Reserved
110	RGMII (System mode) to Auto Media Detect Copper/SGMII (Media mode)
111	RGMII (System mode) to Auto Media Detect Copper/1000BASE-X (when 20_18.6 = 0).

When the mode is set for auto media detect, register 20_18.5:4 specifies which media is the preferred media. See Section Section 2.6 "Fiber/Copper Auto-Selection" on page 57 for more details.

When link is up, two of the three interfaces pass packets back and forth. The unused interface is powered down.

There is no need to power down the unused interface via registers 0_0.11 and 0_1.11. The unused interface will automatically power down when not needed.

2.2 Copper Media Interface

The copper interface consists of the MDIP/N[3:0] pins that connect to the physical media for 1000BASE-T, 100BASE-TX, and 10BASE-T modes of operation.

The device integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between a PHY device and the magnetics. The resistors have to be very accurate to meet the strict IEEE return loss requirements. Typically, ± 1% accuracy resistors are used on the board. These additional components between the PHY and the magnetics complicate board layout. Integrating the resistors has many advantages including component cost savings, better ICT yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements.

2.2.1 Transmit Side Network Interface

2.2.1.1 Multi-mode TX Digital to Analog Converter

The device incorporates a multi-mode transmit DAC to generate filtered 4D PAM 5, MLT3, or Manchester coded symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement, which allows the use of low cost transformers.

2.2.1.2 Slew Rate Control and Waveshaping

In 1000BASE-T mode, partial response filtering and slew rate control are used to minimize high frequency EMI. In 100BASE-TX mode, slew rate control is used to minimize high frequency EMI. In 10BASE-T mode, the output waveform is pre-equalized via a digital filter.

2.2.2 Encoder

2.2.2.1 1000BASE-T

In 1000BASE-T mode, the transmit data bytes are scrambled to 9-bit symbols and encoded into 4D PAM5 symbols. Upon initialization, the initial scrambling seed is determined by the PHY address. This prevents multiple devices from outputting the same sequence during idle, which helps to reduce EMI.

2.2.2.2 100BASE-TX

In 100BASE-TX mode, the transmit data stream is 4B/5B encoded, serialized, and scrambled.

2.2.2.3 10BASE-T

In 10BASE-T mode, the transmit data is serialized and converted to Manchester encoding.

2.2.3 Receive Side Network Interface

2.2.3.1 Analog to Digital Converter

The device incorporates an advanced high speed ADC on each receive channel with greater resolution than the ADC used in the reference model of the IEEE 802.3ab standard committee. Higher resolution ADC results in better SNR, and therefore, lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate. The ADC samples the input signal at 125 MHz.

2.2.3.2 Active Hybrid

The device employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to use the same transformer for coupling to the twisted pair cable, which reduces the cost of the overall system.

2.2.3.3 Echo Canceller

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The device employs a fully developed digital echo canceller to adjust for echo impairments from more than 100 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

2.2.3.4 NEXT Canceller

The 1000BASE-T physical layer uses all 4 pairs of wires to transmit data to reduce the baud rate requirement to only 125 MHz. This results in significant high frequency crosstalk between adjacent pairs of cable in the same bundle. The device employs 3 parallel NEXT cancellers on each receive channel to cancel any high frequency crosstalk induced by the adjacent 3 transmitters. A fully adaptive digital filter is used to compensate for the time varying nature of channel conditions.

2.2.3.5 Baseline Wander Canceller

Baseline wander is more problematic in the 1000BASE-T environment than in the traditional 100BASE-TX environment due to the DC baseline shift in both the transmit and receive signals. The device employs an advanced baseline wander cancellation circuit to automatically compensate for this DC shift. It minimizes the effect of DC baseline shift on the overall error rate.

2.2.3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.2.3.7 Digital Phase Lock Loop

In 1000BASE-T mode, the slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty canceling the echo and NEXT components. In the device, an advanced DPLL is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own, thereby maximizing the achievable SNR.

2.2.3.8 Link Monitor

The link monitor is responsible for determining if link is established with a link partner. In 10BASE-T mode, link monitor function is performed by detecting the presence of valid link pulses (NLPs) on the MDIP/N pins.

In 100BASE-TX and 1000BASE-T modes, link is established by scrambled idles.

If Force Link Good register 16_0.10 is set high, the link is forced to be good and the link monitor is bypassed for 100BASE-TX and 10BASE-T modes. In the 1000BASE-T mode, register 16_0.10 has no effect.

2.2.3.9 Signal Detection

In 1000BASE-T mode, signal detection is based on whether the local receiver has acquired lock to the incoming data stream.

In 100BASE-TX mode, the signal detection function is based on the receive signal energy detected on the MDIP/N pins that is continuously qualified by the squelch detect circuit, and the local receiver acquiring lock.

2.2.4 Decoder

2.2.4.1 1000BASE-T

In 1000BASE-T mode, the receive idle stream is analyzed so that the scrambler seed, the skew among the 4 pairs, the pair swap order, and the polarity of the pairs can be accounted for. Once calibrated, the 4D PAM 5 symbols are converted to 9-bit symbols that are then descrambled into 8-bit data values. If the descrambler loses lock for any reason, the link is brought down and calibration is restarted after the completion of Auto-Negotiation.

2.2.4.2 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and converted to NRZ. The NRZ stream is descrambled and aligned to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded. The receiver does not attempt to decode the data stream unless the scrambler is locked. The descrambler “locks” to the *scrambler* state after detecting a sufficient number of consecutive idle code-groups. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The descrambler is always forced into the *unlocked* state when a link failure condition is detected, or when insufficient idle symbols are detected.

2.2.4.3 10BASE-T

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ, and then aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

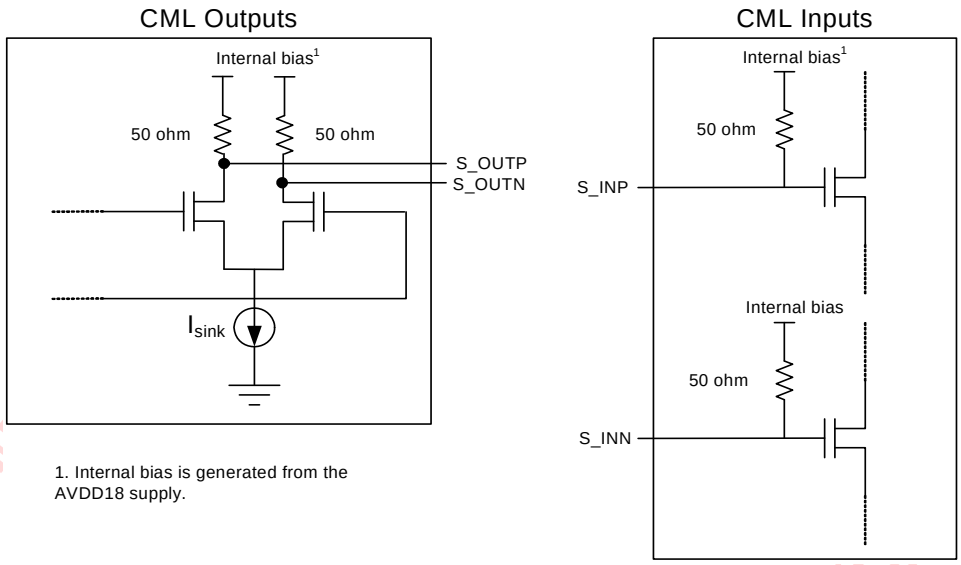
2.3 1.25 GHz SERDES Interface

The 1.25 GHz SERDES Interface can be configured as an SGMII to be hooked up to a MAC or as a 100BASE-FX/1000BASE-X/SGMII to be hooked up to the media.

2.3.1 Electrical Interface

The input and output buffers of the 1.25 GHz SERDES interface are internally terminated by 50 ohm impedance. No external terminations are required. The output swing can be adjusted by programming register 26_1.2:0. The 1.25 GHz SERDES I/Os are Current Mode Logic (CML) buffers. CML I/Os can be used to connect to other components with PECL or LVDS I/Os. See the “Reference Design Schematics” and “Fiber Interface” application note for details.

Figure 8: CML I/Os



1. Internal bias is generated from the AVDD18 supply.

2.4 MAC Interfaces

2.4.1 SGMII Interface

The 88E1512/88E1514 device supports the SGMI specification revision 1.8, except for the carrier extension block that has to be carried out in software. This interface supports 10, 100 and 1000 Mbps modes of operation.

2.4.1.1 SGMII Speed and Link

When the SGMII MAC interface is used, the media interface can only be copper. The operational speed of the SGMII MAC interface is determined according to Table 30 media interface status and/or loopback mode.

Table 30: SGMII (System Interface) Operational Speed

Link Status or Media Interface Status	SGMII (MAC Interface) Speed
No Link	Determined by speed setting of Register 21_2.6,13
MAC Loopback	Determined by speed setting of Register 21_2.6, 13
1000BASE-T at 1000 Mbps	1000 Mbps
100BASE-TX at 100 Mbps	100 Mbps
10BASE-T at 10 Mbps	10 Mbps

Two registers are available to determine whether the SGMII achieved link and sync. Status Register 17_1.5 indicates that the SERDES locked onto the incoming KDKDKD… sequence. Register 17_1.10 indicates whether link is established on the SERDES. If SGMII Auto-Negotiation is disabled, register 17_1.10 has the same meaning as register 17_1.5. If SGMII Auto-Negotiation is enabled, then register 17_1.10 indicates whether SGMII Auto-Negotiation successfully established link.

2.4.1.2 SGMII TRR Blocking

When the SGMII receives a packet with odd number of bytes, a single symbol of carrier extension will be passed on and transmitted onto 1000BASE-T. This carrier extension may cause problems with full-duplex MACs that incorrectly handle the carrier extension symbols. When register 16_1.13 is set to 1, all carrier extend and carrier extend with error symbols received by the SGMII will be converted to idle symbols when operating in full-duplex. Carrier extend and carrier extend with error symbols will not be blocked when operating in half-duplex, or if register 16_1.13 is set to 0. Note that symbol errors will continue to be propagated regardless of the setting of register 16_1.13.

2.4.1.3 False SERDES Link Up Prevention

The SERDES interface can operate in 1000BASE-X mode where an unconnected optical receiver can sometimes send full swing noise into the PHY. This random noise will look like a real signal and falsely cause the 1000BASE-X PCS to link up.

A noise filtering state machine can be enabled to reduce the probability of false link up. When the state machine is enabled it will cause a small delay in link up time. 1000BASE-X noise filtering is enabled through the register below.

Table 31: Fiber Noise Filtering

Register	Function	Setting	Mode	HW Rst	SW Rst
26_1.14	1000BASE-X Noise Filtering	1 = Enable 0 = Disable	R/W	0	Retain

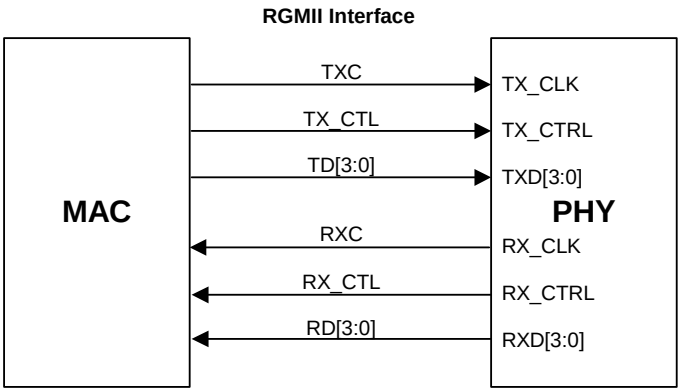
2.4.2 RGMII Interface

The device supports the RGMII specification (Version 1.2a, 9/22/2000, version 2.0, 04/2002). Four RGMII timing modes, with different receive clock to data timing and transmit clock to data timing, can be programmed by setting 21_2.4 and 21_2.5 described in Register 21_2.5. See “RGMII Delay Timing for different RGMII timing modes” on page 251 for timing details.

Table 32: RGMII Signal Mapping

Device Pin Name	RGMII Spec Pin Name	Description
TX_CLK	TXC	125 MHz, 25 MHz, or 2.5 MHz transmit clock with ±50 ppm tolerance based on the selected speed.
TX_CTRL	TX_CTL	Transmit Control Signals. TX_EN is encoded on the rising edge of TX_CLK, TX_ER XORed with TX_EN is encoded on the falling edge of TX_CLK.
TXD[3:0]	TD[3:0]	Transmit Data. In 1000BASE-T mode, TXD[3:0] are presented on both edges of TX_CLK. In 100BASE-TX and 10BASE-T modes, TXD[3:0] are presented on the rising edge of TX_CLK.
RX_CLK	RXC	125 MHz, 25 MHz, or 2.5 MHz receive clock derived from the received data stream and based on the selected speed.
RX_CTRL	RX_CTL	Receive Control Signals. RX_DV is encoded on the rising edge of RX_CLK, RX_ER XORed with RX_DV is encoded on the falling edge of RX_CLK.
RXD[3:0]	RD[3:0]	Receive Data. In 1000BASE-T mode, RXD[3:0] are presented on both edges of RX_CLK. In 100BASE-TX and 10BASE-T modes, RXD[3:0] are presented on the rising edge of RX_CLK.

Figure 9: RGMII Signal Diagram



2.4.3 10/100 Mbps Functionality

The RGMII supports 10 Mbps and 100 Mbps operation by reducing the clock-rate to 2.5 MHz and 25 MHZ respectively as shown in Table 32, RGMII Signal Mapping, on page 50.

During packet reception, RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulse is allowed. No glitching of the clocks is allowed during speed transitions.

The MAC must hold TX_CTRL (TX_CTL) low until the MAC has ensured that TX_CTRL (TX_CTL) is operating at the same speed as the PHY.

2.4.4 TX_ER and RX_ER Coding

See the RGMII Specifications for definitions of TX_ER, RX_ER, and in band status coding.

In RGMII mode, Register 21_2.3 is the register bit used to block carrier extension.

2.5 Loopback

The device implements various different loopback paths.

2.5.1 System Interface Loopback

The functionality, timing, and signal integrity of the System interface can be tested by placing the device in System interface loopback mode. This can be accomplished by setting register 0_0.14 = 1, if copper is the selected media, or 0_1.14 = 1, if fiber is the selected media. In loopback mode, the data received from the MAC is not transmitted out on the media interface. Instead, the data is looped back and sent to the MAC. During loopback, media link will be lost and packets will not be received.

If loopback is enabled while Auto-Negotiating, FLP Auto-Negotiation codes will be transmitted onto the copper media. If loopback is enabled in forced 10BASE-T mode, 10BASE-T idle link pulses will be transmitted on the copper side. If loopback is enabled in forced 100BASE-T mode, 100BASE-T idles will be transmitted on the copper side.

The speed of the SGMII or RGMII interface is determined by register 21_2.6, 13 during loopback. 21_2.2:6,13 is 00 = 10 Mbps, 01 = 100 Mbps, 10 = 1000 Mbps.

Figure 10: MAC Interface Loopback Diagram - Copper Media Interface

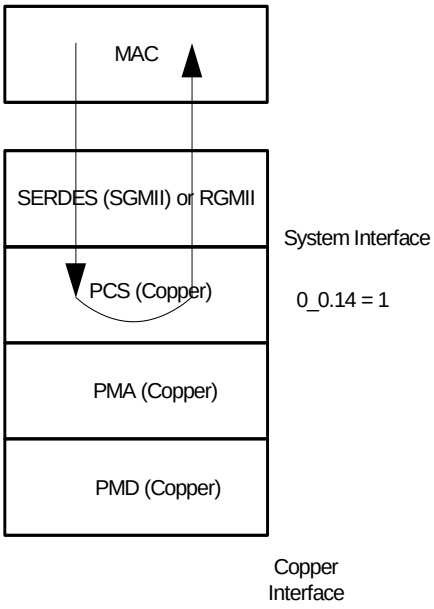
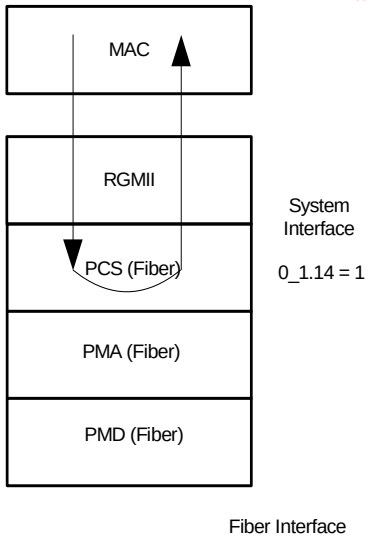


Figure 11: System Interface Loopback Diagram - Fiber Media Interface

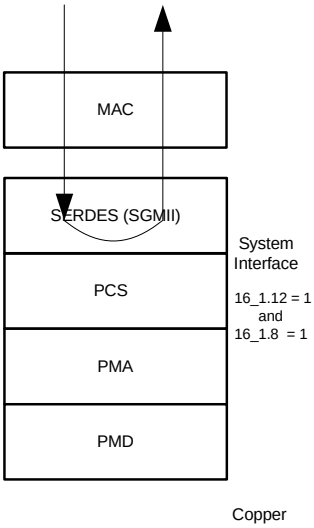


2.5.2 Synchronous SERDES Loopback

The 1.25 GHz SERDES can loop back the raw 10 bit symbol at the receiver back to the transmitter. In this mode of operation, the received data is assumed to be frequency locked with the transmit data output by the PHY. No frequency compensation is performed when the 10 bit symbol is looped back. This mode facilitates testing using non 8/10 symbols such as PRBS.

The 1.25 GHz SERDES synchronous loopback is enabled by setting register 16_1.12 = 1 and 16_1.8 = 1.

Figure 12: Synchronous SERDES Loopback Diagram



2.5.3 Line Loopback

Line loopback allows a link partner to send frames into the device to test the transmit and receive data path. Frames from a link partner into the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. Refer to Figure 13. This allows the link partner to receive its own frames.

Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. If Auto-Negotiation is enabled, both link partners should advertise the same speed and full-duplex. If Auto-Negotiation is disabled, both link partners need to be forced to the same speed and full-duplex. Once link is established, the line loopback mode can be enabled.

Register 21_2.14 = 1 enables the line loopback on the copper interface.

Register 16_1.12 = 1 and 16_1.8 = 0 enables the line loopback of the 1000BASE-X/SGMII media interface.

Figure 13: Copper Line Loopback Data Path

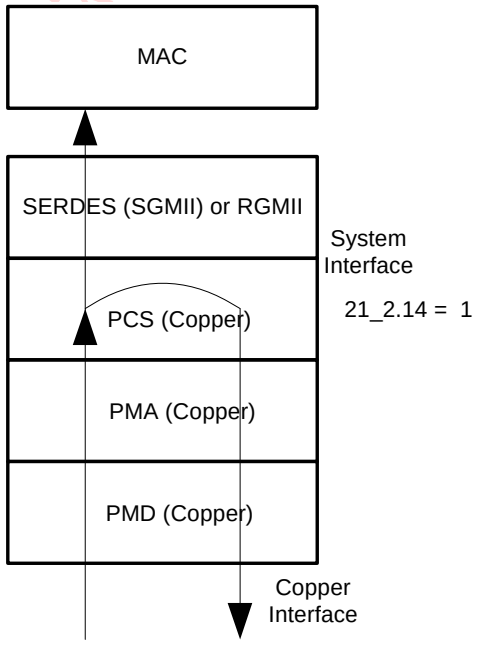
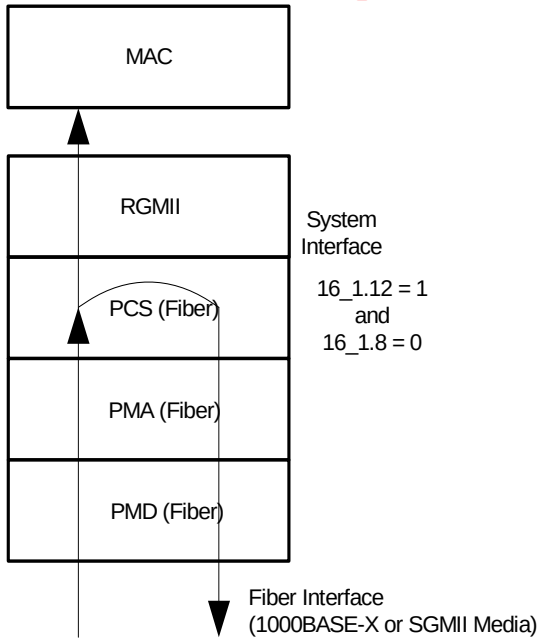


Figure 14: Fiber Line Loopback Data Path



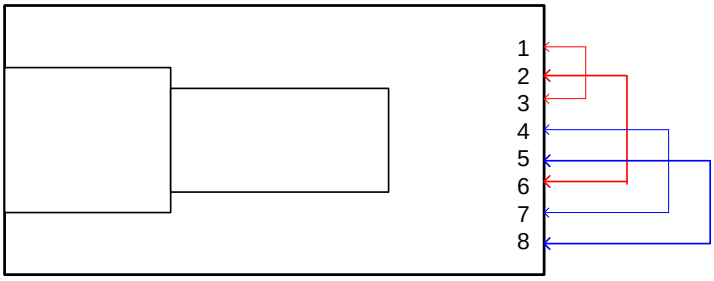
2.5.4 External Loopback

For production testing, an external loopback stub allows testing of the complete data path without the need of a link partner.

For 10BASE-T and 100BASE-TX modes, the loopback test requires no register writes. For 1000BASE-T mode, register 18_6.3 must be set to 1 to enable the external loopback. All copper modes require an external loopback stub.

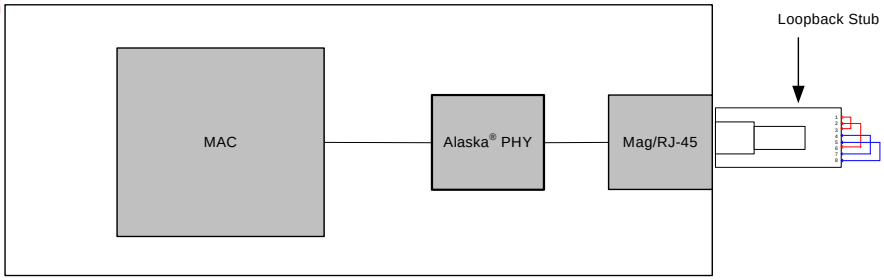
The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1,2 to pair 3,6 and connecting pair 4,5 to pair 7,8, as seen in Figure 15.

Figure 15: Loopback Stub (Top View with Tab up)



The external loopback test setup requires the presence of a MAC that will originate the frames to be sent out through the PHY. Instead of a normal RJ-45 cable, the loopback stubs allows the PHY to self-link at 10/100/1000 Mbps. It also allows the actual external loopback. See Figure 16. The MAC should see the same packets it sent looped back to it.

Figure 16: Test Setup for 10/100/1000 Mbps Modes using an External Loopback Stub



2.6 Fiber/Copper Auto-Selection

The device has a patented feature to automatically detect and switch between fiber and copper cable connections. The auto-selection operates in one of three modes: Copper /1000BASE-X, Copper/100BASE-FX, and Copper/SGMII Media Interface.

Register 20_18.2:0 and register 20_18.6 select the Fiber/Copper auto media modes of operation. See Table 33 for details.

Table 33: Fiber/Copper Auto-media Modes of Operation

Reg 20_18.2:0	Reg 20_18.6	Auto-media Modes of Operation
110	X	Copper/SGMII media
111	0	Copper/1000BASE-X
011	1	Copper/100BASE-FX

The device monitors the signals of the S_INP/N and the MDIP/N[3:0] lines. If a fiber optic cable is plugged in, the device will adjust itself to be in fiber mode. If an RJ-45 cable is plugged in, the device will adjust itself to be in copper mode. If both cables are connected then the first media to establish link, or the preferred media will be enabled. The media which is not enabled will be automatically turned off to save power. If the link on the first media is lost, then the inactive media will be powered up, and both media will once again start searching for link.

2.6.1 Preferred Media

The device can be programmed to give one media priority over the other. In other words if the non-preferred media establishes link first and subsequently energy is detected on the preferred media, the PHY will drop link on the non-preferred media for 4 seconds and give the preferred media a chance to establish link. Register 20_18.5:4 selects the preferred media.

- 00 = Link with the first media to establish link
- 01 = Prefer copper media
- 10 = Prefer fiber media

2.6.2 Definition of link in SGMII Media Interface in the context of auto media selection

In the conventional Copper/1000BASE-X definition of link, 1000BASE-X link is defined to be up when Auto-Negotiation is complete if 1000BASE-X Auto-Negotiation is turned on, or the acquisition of a comma if 1000BASE-X Auto-Negotiation is off. No link is defined to be up when the comma is not seen for some amount of time, or when Auto-Negotiation restarts.

In the Copper/SGMII Media Interface definition of link, the SGMII Media Interface link is up only if bit 15 of the SGMII Auto-Negotiation indicates that link is up. Completing Auto-Negotiation is not sufficient to bring the link up. With SGMII Auto-Negotiation turned off or in the link down case the link definition is identical to the 1000BASE-X case.

2.6.3 Notes on Determining which Media Linked Up

Since there are two sets of IEEE registers (one for copper and the other for fiber) the software needs to be aware of register 22.7:0 so that the correct set of registers are selected. In general the sequence is as follows.

1. Set the Auto-Negotiation registers of the copper medium. (This step may not be necessary if the hardware configuration defaults are acceptable).
2. Set the Auto-Negotiation registers of the fiber medium. (This step may not be necessary if the hardware configuration defaults are acceptable).
3. Poll for link status.Go to step 4 if there is link.
4. Once there is link determine whether the link is copper or fiber medium.
5. Look at the Auto-Negotiation results for the medium that established link.
6. Poll for link status. If link status goes down then go back to step 3.

An example of a polling method procedure is as follows:

1. Write register 22.7:0 to 0x00 to point to the copper medium.Write the appropriate Auto-Negotiation registers to advertise the desired capabilities.
2. Write register 22.7:0 to 0x01 to point to the fiber medium. Write the appropriate Auto-Negotiation registers to advertise the desired capabilities.
3. If one medium is preferred over the other then write register 22.7:0 to 0x02 to point to the MAC registers. Set 20_18.5:4 to the preferred media.
4. Write 0_0.15 and 0_1.15 to '1' to issue software reset. This causes the Auto-Negotiation settings to take effect.
5. Write register 22.7:0 to 0x00 to point to the copper medium. Read the copper link status register 1_0.2. Write register 22.7:0 to 0x01 to point to the fiber medium. Read the fiber link status register 1_1.2. Keep doing this until one of the link comes up. It should be clear which link goes up. When link is up go to the next step.
6. Once the link is up set register 22.7:0 to 0x00 if the copper medium is up, or 0x01 if the fiber medium is up. Read the Auto-Negotiation registers for the Auto-Negotiation status if needed.
7. Poll register 1_0.2 or 1_1.2 depending on copper or fiber link. If link goes down go back to step 5.

2.7 Synchronizing FIFO

The device has transmit synchronizing FIFOs to reconcile frequency differences between the clocks of the MAC interface and the media side. There are two FIFOs on the transmit paths of the copper and Fiber/SGMII as shown in Figure 17. The depth of the FIFOs can be independently programmed by programming register bits 16_1.15:14 and 16_2.15:14. See the “Alaska Ultra FAQs” for details on how to calculate required FIFO depth and the details of the different clocks used for transmit in each mode of operation.

The FIFO depths can be increased in length to support longer frames. The device can handle jumbo frame sizes up to 16 Kbytes with up to ± 100 PPM clock jitter. The deeper the FIFO depth, the higher the latency will be.

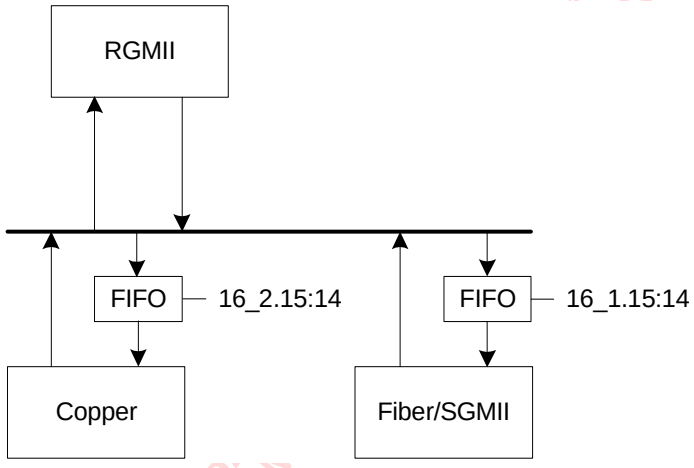
For the device, the status of the FIFO can be interrogated as in Table 34. Registers 19_2.3:2 are set depending on whether the copper transmit FIFO inserted or deleted idle symbols. Idles inserted or deleted will be flagged only if the interpacket gap is 24 bytes or less at the input of the FIFO. Inserted or deleted idles will be ignored if the inter packet gap is greater than 24 bytes.

The FIFO status bits can generate interrupts by setting the corresponding bits in register 18_1 and 18_2.

Table 34: Device FIFO Status Bits

Register	Function	Setting
19_1.7	Fiber Transmit FIFO Over/Underflow	1 = Over/Underflow error 0 = No FIFO error
19_2.7	Copper Transmit FIFO Over/Underflow	1 = Over/Underflow error 0 = No FIFO error
19_2.3	Copper Transmit FIFO Idle Inserted	1 = Idle inserted 0 = No idle inserted
19_2.2	Copper Transmit FIFO Idle Deleted	1 = Idle deleted 0 = No idle deleted

Figure 17: FIFO Locations



2.8 Resets

In addition to the hardware reset pin (RESETn) there are several software reset bits as summarized in Table 35.

The copper, fiber, and RGMII circuits are reset per port via register 0_0.15 and 0_1.15 respectively. A reset in one circuit does not directly affect another circuit.

Register 20_18.15 resets the mode control, port power management, and generator and checkers.

All the reset registers described so far self clear. However, register 20_6.9 is not self clearing. It resets the PTP circuit when it is not used. To re-enable the PTP circuit register 20_6.9 must be manually cleared. When register 20_6.9 is set to 1, registers in banks 8, 9, 10 and 11 are not accessible.

Table 35: Reset Control Bits

Reset Register	Register Effect	Functional Block
0_0.15	Software Reset for Registers in page 0, 2, 3, 5, 7	Copper
0_1.15	Software Reset for Registers in page 1	Fiber/SGMII
20_18.15	Software Reset for Registers in page 6 and 18	Generator/Checker/Mode
20_6.9	Power Down/Reset for Registers in page 8, 9, 12, 14. This register does not self clear. Registers in page 8, 9, 12, and 14 are not accessible if this bit is in reset.	TAI

2.9 Power Management

The device supports several advanced power management modes that conserve power.

2.9.1 Low Power Modes

Four low power modes are supported in the device.

- IEEE 22.2.4.1.5 compliant power down
- Energy Detect (Mode 1)
- Energy Detect+™ (Mode 2)
- IEEE 802.3az-2010 Energy Efficient Ethernet (EEE) compliant low power modes

IEEE 22.2.4.1.5 power down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect (Mode 1) allows the device to wake up when energy is detected on the wire.

Energy Detect+™ (Mode 2) is identical to Mode 1 with the additional capability to wake up a link partner. In Mode 2, the 10BASE-T link pulses are sent once every second while listening for energy on the line.

Energy Efficient ethernet allows the PHY to go into a Low Power Idle (LPI) mode to save power.

Details of each mode are described below.

2.9.1.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting register 0_0.11 or 0_1.11. In this mode, the PHY does not respond to any system interface (i.e., RGMII/SGMII) signals except the MDC/MDIO. It also does not respond to any activity on the copper or fiber media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 0_0.11 and 16_0.2 = 0 for copper and 0_1.11 = 0 for Fiber.

Note that Register 0_0.11 or 16_0.2 may be set to 1 to power down the copper media.

As shown in Table 36, each power down control independently powers down its respective circuits. In general, it is not necessary to power down an unused interface. The PHY will automatically power down any unused circuit. For example when auto-media detect is turned on, the unused interface will automatically power down.

The automatic PHY power management can be overridden by setting the power down control bits. These bits have priority over the PHY power management in that the circuit can not be powered up by the power management when its associated power down bit is set to 1. When a circuit is power back up by setting the bit to 0, a software reset is also automatically sent to the corresponding circuit.

Table 36: Power Down Control Bits

Reset Register	Register Effect
0_0.11	Copper Power Down
16_0.2	Copper Power Down
0_1.11	Fiber/SGMII Power Down

2.9.1.2 Copper Energy Detect Modes

The device can be placed in energy detect power down modes by selecting either of the two energy detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable. The status of the energy detect is reported in register 17_0.4 and the energy detect changes are reported in register 19_0.4. The energy detect modes only apply to the copper media. The energy detect modes will not work while Fiber/Copper Auto Select (2.5 “Fiber/Copper Auto-Selection” on page 45) is enabled. Normal 10/100/1000 Mbps operation can be entered by turning off energy detect mode by setting register 16_0.9:8 to 0x.

Energy Detect (Mode 1)

Energy Detect (Mode 1) is entered by setting register 16_0.9:8 to 10.

In Mode 1, only the signal detection circuitry and serial management interface are active. If the PHY detects energy on the line, it starts to Auto-Negotiate sending FLPs for 5 seconds. If at the end of 5 seconds the Auto-Negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If Auto-Negotiation is completed, then the PHY goes into normal 10/100/1000 Mbps operation. If during normal operation the link is lost, the PHY will re-start Auto-Negotiation. If no energy is detected after 5 seconds, the PHY goes back to monitoring receive energy.

Energy Detect +™ (Mode 2)

Energy Detect (Mode 2) is entered by setting register 16_0.9:8 to 11.

In Mode 2, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the device is in Mode 1, it cannot wake up a connected device; therefore, the connected device must be transmitting NLPs, or either device must be woken up through register access. If the device is in Mode 2, then it can wake a connected device.

Power Down Modes

When the PHY exits power down (register 0_0.11= 0 and 16_0.2=0) the active state will depend on whether the energy detect function is enabled (register 16_0.9:8 = 1x). If the energy detect function is enabled, the PHY will transition to the energy detect state first and will wake up only if there is a signal on the wire.

Table 37: Power Down Modes

Register 0_0.11	Register 16_0.2	Register 16_0.9:8	Behavior
1	x	xx	Power down
x	1	xx	Power down

2.9.1.3 Energy Efficient Ethernet (EEE) Low Power Modes

The 88E1510/88E1518/88E1512/88E1514 device supports IEEE 802.3az-2010 Energy Efficient Ethernet (EEE). The device supports EEE on the following Media Interface:

- 10BASE-Te
- 100BASE-TX EEE
- 1000BASE-T EEE

See Section 2.15 "Energy Efficient Ethernet (EEE)" on page 75 for further details.

2.9.2 RGMII/SGMII MAC Interface Power Down

In some applications, the MAC interface must run continuously regardless of the state of the media interface. Additional power will be required to keep the MAC interface running during low power states.

If absolute minimal power consumption is required during network interface power down mode or in the Energy Detect modes, then register 16_2.3 or 16_1.3 should be set to 0 to allow the MAC interface to power down.

In general 16_2.3 is used when the network interface is copper and 16_1.3 is used when the network interface is fiber. Note that for these settings to take effect a software reset must be issued.

In the auto media detect modes (MODE = 110 and 111) both the fiber side and copper side has to indicate power down before the RGMII port can be powered down.

2.10 Auto-Negotiation

The device supports three types of Auto-Negotiation.

- 10/100/1000BASE-T Copper Auto-Negotiation. (IEEE 802.3 Clauses 28 and 40)
- 1000BASE-X Fiber Auto-Negotiation (IEEE 802.3 Clause 37)
- SGMII Auto-Negotiation (Cisco specification)
- EEE Auto-Negotiation. For further details, refer to Section 2.15.3 "Energy Efficient Ethernet Auto-Negotiation" on page 76.

Auto-Negotiation provides a mechanism for transferring information from the local station to the link partner to establish speed, duplex, and Master/Slave preference (in the case of Copper Auto-Negotiation) during a link session.

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset (Register 0_0.15 or 0_1.15)
- Restart Auto-Negotiation (Register 0_0.9 or 0_1.9)
- Transition from power down to power up (Register 0_0.11 or 0_1.11)
- The link goes down

The following sections describe each of the Auto-Negotiation modes in detail.

2.10.1 10/100/1000BASE-T Auto-Negotiation

The 10/100/1000BASE-T Auto-Negotiation (AN) is based on Clause 28 and 40 of the IEEE 802.3 specification. It is used to negotiate speed, duplex, and flow control over CAT5 UTP cable. Once Auto-Negotiation is initiated, the device determines whether or not the remote device has Auto-Negotiation capability. If so, the device and the remote device negotiate the speed and duplex with which to operate.

If the remote device does not have Auto-Negotiation capability, the device uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-T modes. If link is established based on the parallel detect function, then it is required to establish link at half-duplex mode only. Refer to IEEE 802.3 clauses 28 and 40 for a full description of Auto-Negotiation.

After hardware reset, 10/100/1000BASE-T Auto-Negotiation can be enabled and disabled via Register 0_0.12. Auto MDI/MDIX and Auto-Negotiation may be disabled and enabled independently. When Auto-Negotiation is disabled, the speed and duplex can be set via registers 0_0.13, 0_0.6,

and 0_0.8 respectively. When Auto-Negotiation is enabled the abilities that are advertised can be changed via registers 4_0 and 9_0.

Changes to registers 0_0.12, 0_0.13, 0_0.6 and 0_0.8 do not take effect unless one of the following takes place:

- Software reset (registers 0_0.15)
- Restart Auto-Negotiation (register 0_0.9)
- Transition from power down to power up (register 0_0.11)
- The copper link goes down

To enable or disable Auto-Negotiation, Register 0_0.12 should be changed simultaneously with either register 0_0.15 or 0_0.9. For example, to disable Auto-Negotiation and force 10BASE-T half-duplex mode, register 0_0 should be written with 0x8000.

Registers 4_0 and 9_0 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine. Hence, a write into Register 4_0 or 9_0 has no effect once the device begins to transmit Fast Link Pulses (FLPs).This guarantees that sequences of FLPs transmitted are consistent with one another.

Register 7_0 is treated in a similar way as registers 4_0 and 9_0 during additional next page exchanges.

If 1000BASE-T mode is advertised, then the device automatically sends the appropriate next pages to advertise the capability and negotiate Master/Slave mode of operation. If the user does not wish to transmit additional next pages, then the next page bit (Register 4_0.15) can be set to zero, and the user needs to take no further action.

If next pages in addition to the ones required for 1000BASE-T are needed, then the user can set register 4_0.15 to one, and send and receive additional next pages via registers 7_0 and 8_0, respectively. The device stores the previous results from register 8 in internal registers, so that new next pages can overwrite register 8_0.

Note that 1000BASE-T next page exchanges are automatically handled by the device without user intervention, regardless of whether or not additional next pages are sent.

Once the device completes Auto-Negotiation, it updates the various status in registers 1_0, 5_0, 6_0, and 10_0. Speed, duplex, page received, and Auto-Negotiation completed status are also available in registers 17_0 and 19_0.

Refer to Register 17_0 and 19_0.

2.10.2 1000BASE-X Auto-Negotiation

1000BASE-X Auto-Negotiation is defined in Clause 37 of the IEEE 802.3 specification. It is used to Auto-Negotiate duplex and flow control over fiber cable. Registers 0_1, 4_1, 5_1, 6_1, and 15_1 are used to enable AN, advertise capabilities, determine link partner's capabilities, show AN status, and show the duplex mode of operation respectively.

Register 22.7:0 must be set to one to view the fiber Auto-Negotiation registers.

The device supports Next Page option for 1000BASE-X Auto-Negotiation. Register 7_1 of the fiber pages is used to transmit Next Pages, and register 8_1 of the fiber pages is used to store the received Next Pages. The Next Page exchange occurs with software intervention. The user must set Register 4_1.15 to enable fiber Next Page exchange. Each Next Page received in the registers should be read before a new Next Page to be transmitted is loaded in Register 7_1.

If the PHY enables 1000BASE-X Auto-Negotiation and the link partner does not, the link cannot link up. The device implements an Auto-Negotiation bypass mode. See Section 2.10.3.2 for more details.

2.10.3 SGMII Auto-Negotiation

SGMII is a de-facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the “Cisco SGMII Specification” and the “MAC Interfaces and Auto-Negotiation” application note for further details.

The device supports SGMII interface with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to Register 0_1.12 followed by a soft reset. If SGMII Auto-Negotiation is disabled, the MAC interface link, speed, and duplex status (determined by the media side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other way (e.g., by reading PHY registers for link, speed, and duplex status). However, the operational speed of the SGMII will follow the speed of the media (See Table 30 on page 49) regardless of whether the Auto-Negotiation is enabled or disabled.

In case of RGMII to SGMII mode of operation, the SGMII interface behaves as if it were the SGMII on the MAC side of the interface. When Auto-Negotiation is enabled, the SGMII Auto-Negotiation information like the speed, duplex, and link received from the PHY is used for determining the mode of operation. The RGMII interface will be adjusted accordingly when the SGMII Auto-Negotiation is completed.

2.10.3.1 Flow control Enhancement to SGMII Auto-Negotiation

During standard SGMII Auto-Negotiation the PHY passes the link, speed, and duplex information to the MAC. The flow control information is not communicated. Typically, the MAC will have to read the registers of the PHY to find out the flow control capability of the link partner. The device has added in-line flow control information by using some of the reserved bits of the Auto-Negotiation base page as defined by the SGMII specification. This feature is optional. The user can select the standard SGMII Auto-Negotiation or the enhanced mode as described in Table 39. Table 38 shows the bit definitions for the enhanced mode.

Bit 9 corresponds to register 17_1.3 and bit 8 corresponds to register 17_1.2.

Register 16_1.7 will enable this feature (Table 39). 0 = set bits 9:7 always to 000, 1 = set bits 9:7 according to Table 38. The default is disabled.

Table 38: Enhanced SGMII PHY Status

TX_CONFIG_REG[15:0]			
Bit Number	**Reg 16_1.7:6 = ‘00’**	**Reg 16_1.7:6 = ‘01’**	**Reg 16_1.7:6 = ‘10’**
15	1 = Link Up 0 = Link Down	1 = Link Up 0 = Link Down	1 = Link Up 0 = Link Down
14	Acknowledge	Acknowledge	Acknowledge
13	0 = Reserved	0 = Reserved	0 = Reserved
12	1 = Full-duplex 0 = Half-duplex	1 = Full-duplex 0 = Half-duplex	1 = Full-duplex 0 = Half-duplex
11:10	00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved	00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved	00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved
9	1 = EEE supported 0 = EEE not supported	1 = Transmit pause enabled 0 = Disabled	1 = EEE supported 0 = EEE not supported

Table 38: Enhanced SGMII PHY Status (Continued)

TX_CONFIG_REG[15:0]			
Bit Number	**Reg 16_1.7:6 = '00'**	**Reg 16_1.7:6 = '01'**	**Reg 16_1.7:6 = '10'**
8	1 = EEE clock stop supported 0 = EEE clock stop not supported	1 = Received pause enabled 0 = Disabled	1 = EEE clock stop supported 0 = EEE clock stop not supported
7	0 = Reserved	0 = 10/100/1000BASE-T 1 = 100BASE-FX/1000BASE-X	0 = Reserved
6	0 = Reserved	1 = EEE supported 0 = EEE not supported	0 = Reserved
5	0 = Reserved	1 = EEE clock stop supported 0 = EEE clock stop not supported	0 = Reserved
4	0 = Reserved	0 = Reserved	0 = Reserved
3	0 = Reserved	0 = Reserved	1 = Transmit pause enabled 0 = Disabled
2	0 = Reserved	0 = Reserved	1 = Received pause enabled 0 = Disabled
1	0 = Reserved	0 = Reserved	0 = 10/100/1000BASE-T 1 = 100BASE-FX/1000BASE-X
0	Always 1	Always 1	Always 1

Table 39: MAC Specific Control Register 1

Register	Function	Setting	Mode	HW Rst	SW Rst
16_1.7:6	Enhanced SGMII	00 = Do not pass flow control bits through SGMII Auto-Negotiation. SGMII (System mode) registers 4_1.9:7 are always 000. EEE bits are passed per IEEE. 01 = Pass flow control bits through SGMII Auto-Negotiation using 4_1.9:7. EEE bits are passed in alternate locations. 10 = Pass flow control bits through SGMII Auto-Negotiation using bits other than 4_1.9:7. EEE bits use 9:8. 11 = Reserved	R/W	0x0	Update

2.10.3.2 Serial Interface Auto-Negotiation Bypass Mode

If the MAC or the PHY implements the Auto-Negotiation function and the other does not, two-way communication is not possible unless Auto-Negotiation is manually disabled and both sides are configured to work in the same operational modes. To solve this problem, the device implements the SGMII Interface Auto-Negotiation Bypass Mode. When entering the state “Ability_Detect”, a bypass timer begins to count down from an initial value of approximately 200 ms. If the device receives idles during the 200 ms, the device will interpret that the other side is “alive” but cannot send configuration codes to perform Auto-Negotiation. After 200 ms, the state machine will move to a new state called “Bypass_Link_Up” in which the device assumes a link-up status and the operational mode is set to the value listed under the “Comments” column of Table 40. Refer to the Section 2.1 for further details.

Table 40: SGMII Auto-Negotiation modes

Reg. 0_1.12	Reg. 26_1.6	Comments
0	X	No Auto-Negotiation. User responsible for determining speed, link, and duplex status by reading PHY registers.
1	0	Normal SGMII Auto-Negotiation. Speed, link, and duplex status automatically communicated to the MAC during Auto-Negotiation.
1	1	MAC Auto-Negotiation enabled. Normal operation.
		MAC Auto-Negotiation disabled. After 200 ms the PHY will disable Auto-Negotiation and link based on idles.

2.11 Downshift Feature

Without the downshift feature enabled, connecting between two Gigabit link partners requires a four-pair RJ-45 cable to establish 10, 100, or 1000 Mbps link. However, there are existing cables that have only two-pairs, which are used to connect 10 Mbps and 100 Mbps Ethernet PHYs. With the availability of only pairs 1, 2 and 3,6, Gigabit link partners can Auto-Negotiate to 1000 Mbps, but fail to link. The Gigabit PHY will repeatedly go through the Auto-Negotiation but fail 1000 Mbps link and never try to link at 10 Mbps or 100 Mbps.

With the Marvell® downshift feature enabled, the device is able to Auto-Negotiate with another Gigabit link partner using cable pairs 1,2 and 3,6 to downshift and link at 10 Mbps or 100 Mbps, whichever is the next highest advertised speed common between the two Gigabit PHYs.

In the case of a three pair cable (additional pair 4,5 or 7,8 - but not both) the same downshift function for two-pair cables applies.

By default, the downshift feature is turned off. Refer to register 16_0.14:11 which describe how to enable this feature and how to control the downshift algorithm parameters.

To enable the downshift feature, the following registers must be set:

- Register 16_0.11 = 1 - enables downshift
- Register 16_0.14:12 - sets the number of link attempts before downshifting

2.12 Fast 1000BASE-T Link Down Indication

Per the IEEE 802.3 Clause 40 standard, a 1000BASE-T PHY is required to wait 750 milliseconds or more to report that link is down after detecting a problem with the link. For Metro Ethernet applications, a Fast Failover in 50 ms is specified, which cannot be met if the PHY follows the 750 ms wait time. This delay can be reduced by intentionally violating the IEEE standard by setting register 26_0.9 to 1.

The delay at which link down is to be reported can be selected by setting register 26_0.11:10. 00 = 0ms, 01 = 10 ± 2 ms, 10 = 20 ± 2ms, 11 = 40 ± 2ms.

2.13 Advanced Virtual Cable Tester®

The device Advanced Virtual Cable Tester feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The device transmits a signal of known amplitude (+1V) down each of the four pairs of an attached cable. It will conduct the cable diagnostic test on each pair, testing the MDI_0_0P/N, MDI_0_1P/N, MDI_0_2P/N, and MDI_0_3P/N pairs sequentially. The transmitted signal will continue down the cable until it reflects off of a cable imperfection.

The Advanced VCT™ has 4 modes of operation that is programmable via register 23_5.7:6. The first mode returns the peak with the maximum amplitude that is above a certain threshold. The second mode returns the first peak detected that is above a certain threshold. The third mode measures the systematic offset at the receiver. The fourth mode measures the amplitude seen at a certain specified distance.

The VCT test is initiated by setting register 23_5.15 to 1. This bit will self clear when the test is completed. Register 23_5.14 will be set to a 1 indicating that the TDR results in the registers are valid.

Each point in the VCT reflected waveform is sampled multiple times and averaged. The number of samples to take is programmable via register 23_5.10:8.

Each time the VCT test is enable, the results seen on the four receive channels are reported in registers 16_5, 17_5, 18_5, and 19_5. Register 23_5.13:11 selects which channel transmits the test pulse.

When register 23_5.13:11 is set to 000 the same channel reflection is recorded. In other words, channel 0 transmits a pulse and the reflection seen on channel 0 receiver is reported. Channel 1 transmits a pulse and the reflection seen on channel 1 receiver is reported. The same for channel 2 and channel 3.

When register 23_5.13:11 is set to 100 all 4 receive channels report the reflection seen by a pulse transmitted by channel 0.

When register 23_5.13:11 is set to 101 all 4 receive channels report the reflection seen by a pulse transmitted by channel 1.

When register 23_5.13:11 is set to 110 all 4 receive channels report the reflection seen by a pulse transmitted by channel 2.

When register 23_5.13:11 is set to 111 all 4 receive channels report the reflection seen by a pulse transmitted by channel 3.

Hence, if only the reflection seen on the same channel is desired the VCT test should be run with 23_5.13:11 = 000. If all same channel and cross channel combinations are desired then the VCT test must be run 4 times with 23_5.13:11 set to 100, 101, 110, and 111 for the 4 runs. Registers 16_5, 17_5, 18_5, and 19_5 should be read and stored between each run.

2.13.1 Maximum Peak

When register 23_5.7:6 is set to 00, the maximum peak above a certain threshold is reported. Pulses are sent out and recorded according to the setting of register 23_5.13:11.

There are 10 threshold settings for same channel reflections and are specified by registers 26_5.6:0, 26_5.14:8, 27_5.6:0, 27_5.14:8, and 28_5.6:0 for positive reflections and 26_7.6:0, 26_7.14:8, 27_7.6:0, 27_7.14:8, and 28_7.6:0 for negative reflections.

These settings correspond to the amplitude threshold the reflected signal has to exceed before it is counted. Any reflected signal below this threshold level is ignored. The threshold settings are based on cable length with the breakpoints at 10 m, 50 m, 110 m, and 140 m.

There are 4 threshold settings for cross-channel specified by registers 25_5.6:0 and 25_5.14:8 for positive reflections and 25_7.6:0 and 25_7.14:8 for negative reflections. The threshold settings are based on cable length with the breakpoints at 10 m.

The default values are targeted to 85 ohm to 115 ohms. However these threshold settings should be calibrated for the desired impedance setting on the target system.

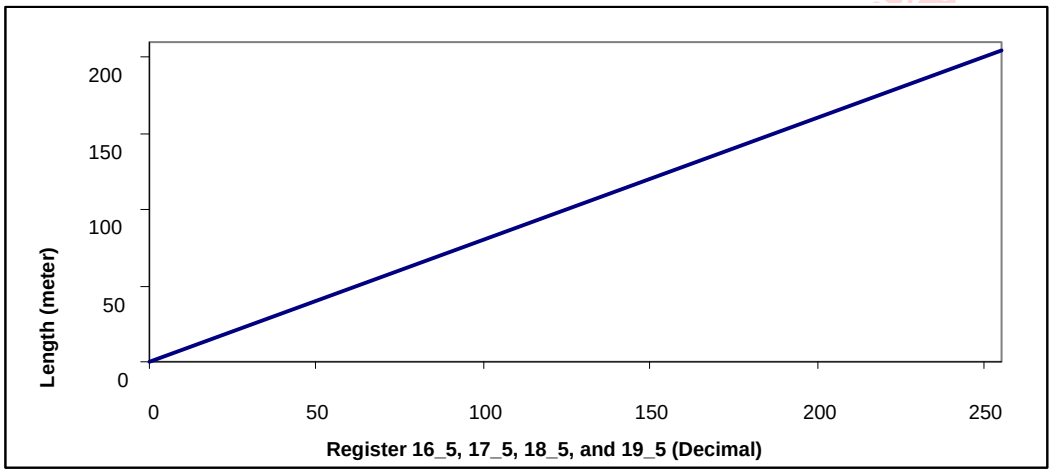
The results are stored in registers 16_5, 17_5, 18_5, and 19_5. Bits 7:0 report the distance of the peak. The distance can be converted to using the trend line in Figure 18. Bits 14:8 report the reflected amplitude. Bit 15 reports whether the reflected amplitude was positive or negative. When bits 15:8 return a value of 0x80, it means there was no peak detected above the threshold. If bits 15:8 return a value of 0x00 then the test failed.

Register 28_5.7 controls the exact distance that is reported. When set to 0 the distance where the amplitude falls to 50% of the peak amplitude is reported. When set to 1 the distance where the peak amplitude actually occurs is reported. In either case, the magnitude of the maximum amplitude is reported in bits 14:8.

In the maximum peak mode, register 24_5.7:0 is used to set the starting distance of the sweep. Normally this value should be set to 0. If this value is set to a non-zero value, any reflection below the starting distance is ignored. Note that 24_5.8 is ignored.

Note that the maximum peak only measures up to about 200 meters of cable.

Figure 18: Cable Fault Distance Trend Line



2.13.2 First Peak

When register 23_5.7:6 is set to 01, the first peak above a certain threshold is reported. The first peak operates in exactly the same way as the maximum peak except that there has to be some qualification as to what constitutes a peak since the first peak is not necessarily the maximum peak. The first peak is defined as the maximum amplitude seen before the reflected amplitude drops by some value below this peak. This hysteresis value is defined by register 23_5.5:0.

For example, in Figure 19, if Pa is greater than the hysteresis value in 23_5.5:0 and Va is above the threshold value, then Va and Da are reported since it is the first peak that is above the threshold.

If Pa is less than the hysteresis value in 23_5.5:0, then Va and Da are not reported as the first peak. Vb and Db will be reported as the first peak if Pb is greater than the hysteresis value in 23_5.5:0 and Vb is above the threshold value.

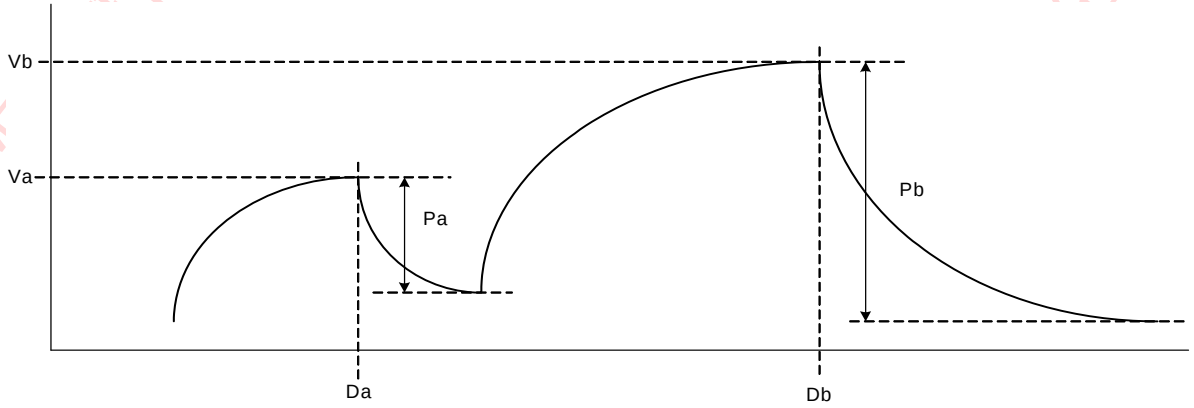
If Pa is greater than the hysteresis value in 23_5.5:0 but Va is below the threshold value then Va and Da are not reported as the first peak. Vb and Db will be reported as the first peak if Pb is greater than the hysteresis value in 23_5.5:0 and Vb is above the threshold value.

Register 28_5.7 controls the exact distance that is reported. When set to 0 the distance where the amplitude falls below the peak amplitude minus the hysteresis level as defined in register 23_5.5:0 is reported. When set to 1 the distance where the peak amplitude actually occurs is reported. In either case, the magnitude of the maximum amplitude of the first peak is reported in bits 14:8.

In the first peak mode register 24_5.7:0 is used to set the starting distance of the sweep. Normally, this value should be set to 0. If this value is set to a non-zero value, any reflection below the starting distance is ignored. This may be useful to ignore reflections at the transformer that are reported as the first peak. Note that 24_5.8 is ignored.

Note that the maximum peak only measures up to about 200 meters of cable.

Figure 19: First Peak Example



2.13.3 Offset

The offset reports the offset seen at the receiver. This is a debug mode. Bits 7:0 of registers 16_5, 17_5, 18_5, and 19_5 have no meaning. When bits 15:8 return a value of 0x80 it means there is zero offset. If bit 15:8 returns a value of 0x00 then the test failed.

Note that in the maximum peak, first peak, and sample point modes, the systematic offset is automatically subtracted from the results.

2.13.4 Sample Point

When register 23_5.7:6 is set to 11, the amplitude of the reflected pulse at a particular distance on the cable is reported. Unlike the maximum peak and first peak modes which only measures up to about 200 meters of cable, the sample point mode can measure up to 400 meters of cable.

The sample point returns the amplitude of the reflected pulse at a particular distance on the cable. The distance is set by register 24_5.8:0. The threshold registers 25_5, 26_5, 27_5, 28_5.6:0, 25_7, 26_7, 27_7, and 28_7.6:0 are ignored.

Bits 7:0 of registers 16_5, 17_5, 18_5, and 19_5 return the same value as 24_5.7:0. Note that register 24_5.8 is not returned. Bits 14:8 return the amplitude, and bit 15 the sign of the amplitude. If the test failed bits 15:8 will return 00000000 (zero amplitude will always return as 10000000).

By programming register 24_5.8:0 from 0x000 to 0x1FF and running the sample point test at each distance it is possible to reconstruct the reflected amplitude. Note that since the threshold is ignored, it is possible that some small reflections in the same channel measurements will be reported at short cable lengths when there are none. This is because the analog hybrid does not 100% cancel out the transmitted signal.

2.13.5 Pulse Amplitude and Pulse Width

The transmitted pulse amplitude and pulse width can be adjusted via registers 28_5.9:8 and 28_5.11:10 respectively. They should normally be set to full amplitude and full pulse width.

2.13.6 Drop Link

When register 28_5.12 is set to 0 the circuit will wait 1.5 seconds to break the link before starting VCT™. When set to 1 this delay is bypassed.

2.13.7 VCT™ with Link Up

The following status requires the PHY to link up with a link partner.

- Register 20_5 reports the pair skew of each pair of wires relative to each other.
- Register 21_5.3:0 reports the polarity of each pair of wires.
- Register 21_5.5:4 reports the crossover status
- Register 20_5 and 21_5 are not valid unless register 21_5.6 is set to 1.

2.13.8 Alternate VCT Control

The registers in page 7 provides an alternate means to control VCT. When using page 7 to control the VCT, the VCT results in registers 16_5, 17_5, 18_5, and 19_5 will be altered and are not meaningful. Register 21_7.14 must be set to 0 when controlling VCT using registers in page 5.

VCT will run when any one of the following three events occur:

- Register 21_7.12 transitions from 0 to 1.
- Register 21_7.15 transitions from 0 to 1.
- Link transitions from link up to link down and register 21_7.14 = 1.

Note that if the VCT circuit is busy when any of the three events occur, the event is ignored.

If register 21_7.15 triggers VCT then the 1.5s break link prior to measurement is bypassed.

If any of the other 2 events triggers VCT then the 1.5s break link prior to measurement is not bypassed.

If register 21_7.13 = 1 then only same pair is checked using the first peak method.

If register 21_7.13 = 0 then same pair and cross pair are checked using the first peak method.

Register 21_7.11 indicates whether the cable testing is completed or not. Once completed the results are presented in registers 16_7, 17_7, 18_7, 19_7, and 20_7. It may be possible for multiple faults to occur on the same pair but only one fault can be reported. The priority in reporting in descending order is as follows.

- Test failed (busy).
- Fault at the shortest distance from the PHY (open, short, cross pair short).
- In case of a tie in distance, open and short has higher priority than cross pair short.
- Cable good

When a pair is reported as good, the value in its corresponding cable length register is invalid.

Register 21_7.10 selects how the cable length is to be presented – in meters or centimeters. Note that register 21_7.10 should not be change in the middle of a VCT test. Once the testing is complete and cable length values written into registers 16_7, 17_7, 18_7, and 19_7, the values will not change when register 21_7.10 changes. Changes to 21_7.10 will only take effect the next time VCT is started.

Table 41: Alternate VCT™ Control

Register	Function	Setting	Mode
16_7.15:0	Pair 0 Cable Length	Length to fault in meters or centimeters based on register 21_7.10.	RO
17_7.15:0	Pair 1 Cable Length	Length to fault in meters or centimeters based on register 21_7.10.	RO
18_7.15:0	Pair 2 Cable Length	Length to fault in meters or centimeters based on register 21_7.10.	RO
19_7.15:0	Pair 3 Cable Length	Length to fault in meters or centimeters based on register 21_7.10.	RO
20_7.15:12	Pair 3 Fault Code	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved	RO

Table 41: Alternate VCT™ Control (Continued)

Register	Function	Setting	Mode
20_7.11:8	Pair 2 Fault Code	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved	RO
20_7.7:4	Pair 1 Fault Code	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved	RO
20_7.3:0	Pair 0 Fault Code	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved	RO
21_7.15	Run Immediately	0 = No Action 1 = Run VCT Now	R/W, SC
21_7.14	Run at each Auto-Negotiation Cycle	0 = Do No Run At Auto-Negotiation Cycle 1 = Run At Auto-Negotiation Cycle	R/W
21_7:13	Disable Cross Pair Check	0 = Enable Cross Pair Check 1 = Disable Cross Pair Check	R/W
21_7.12	Run After Break Link	0 = No Action 1 = Run VCT After Breaking Link	R/W, SC
21_7.11	Cable Diagnostics Status	0 = Complete 1 = In Progress	RO
21_7.10	Cable Length Unit	0 = Centimeters 1 = Meters	R/W

2.14 Data Terminal Equipment (DTE) Detect

The device supports the Data Terminal Equipment (DTE) power function. The DTE power function is used to detect if a link partner requires power supplied by the POE PSE device.

The DTE power function can be enabled by writing to register 26_0.8. When DTE is enabled, the device will first monitor for any activity transmitted by the link partner. If the link partner is active, then the link partner has power and power from the POE PSE device is not required. If there is no activity coming from the link partner, DTE power engages, and special pulses are sent to detect if the link partner requires DTE power. If the link partner has a low pass filter (or similar fixture) installed, the link partner will be detected as requiring DTE power.

The DTE power status register (Register 17_0.2) immediately comes up as soon as link partner is detected as a device requiring DTE power. Register 19_0.2 is a stray bit that reports the DTE power status has changed states.

If a link partner that requires DTE power is unplugged, the DTE power status (register 17_0.2) will drop after a user controlled delay (default is 20 seconds - Register 26_0.7:4) to avoid DTE power status register drop during the link partner powering up (for most applications), since the low pass filter (or similar fixture) is removed during power up. If DTE power status drop is desired to be reported immediately, write register 26_0.7:4 to 4'b0000.

A detailed description of the register bits used for DTE power detection for the device are shown in Table 42.

Table 42: Registers for DTE Power

Register	Description
26_0.8 - Enable power over Ethernet detection	1 = Enable DTE detect 0 = Disable DTE detect A soft reset is required to enable this feature HW reset: 0 SW reset: Update
17_0.2 - Power over Ethernet detection status	1 = Need power 0 = Do not need power HW reset: 0 SW reset: 0
19_0.2 - Power over Ethernet detection state changed	1 = Changed 0 = No change HW reset: 0 SW reset: 0
26_0.7:4 - DTE detect status drop	Once the PHY no longer detects that the link partner filter, the PHY will wait a period of time before clearing the power over Ethernet detection status bit (17_0.2). The wait time is 5 seconds multiplied by the value of these bits. Example: (5 * 0x4 = 20 seconds) Default at HW reset: 0x4 At SW reset: retain

2.15 Energy Efficient Ethernet (EEE)

2.15.1 Energy Efficient Ethernet Low Power Modes

The 88E1510/88E1518/88E1512/88E1514 devices support two EEE modes:

a) Legacy or Master mode

b) EEE aware or Slave mode

2.15.1.1 Master (Legacy) mode

The legacy mode of operation is used in systems where the external MAC is not EEE capable. The MAC and the system are completely transparent to the EEE operation. Entering and exiting out of EEE operation or Low Power Idle (LPI) mode is completely managed and controlled by the PHY alone. Once EEE capabilities are exchanged with an EEE compliant link partner, the PHY waits for an enter timer to expire. This enter timer tracks the amount of time without a data transaction between the MAC and the PHY. Once the enter timer expires the PHY begins to transmit the low power idles to save power. Once the low power mode is disabled, either because of a wake signal received from the link partner or data received from the MAC, the PHY waits for an exit timer to expire before it resumes normal operation. The exit timer tracks the transition from the low power idle mode to normal operation.

The Legacy mode of operation uses the EEE buffer for storing the data from the MAC before it exits out of the EEE LPI. Refer to Section 2.15.2 for further details.

The EEE buffer has an enter timer and an exit timer. The enter timer and exit timer settings are available in Register 1_18 and 2_18. By default, it assumes IEEE timer values. When the EEE buffer is empty, an enter timer will be initiated. Before the enter timer expires, if the EEE buffer receives any packet from the legacy MAC the enter timer will be restarted. But if the buffer remains empty until the expiration of the enter timer, then the device enters the LPI mode and begins transmitting LPI. As long as the buffer remains empty, the device continues to transmit LPI.

Once the EEE buffer begins receiving packets from the MAC, an exit timer is initiated and the device sends a WAKE signal to the link partner indicating that data will be transmitted shortly. Alternatively, the device can also transition out of the LPI mode if it receives a WAKE from its link partner. When the exit timer expires, the device transitions out of LPI mode to resume normal transmission.

2.15.1.2 Slave (EEE Aware) mode

By default the PHY is configured in EEE Slave mode (Reg 0_18.0 = 0). In the EEE Slave mode, the external MAC connected to the system interface must be EEE-capable and must meet the IEEE 802.3az-2010 Clause 78 requirements. In this mode, the EEE buffering is disabled and EEE enter/exit timers settings are ignored. The MAC is expected to handle all time requirements. The MAC is expected to buffer the packets while the PHY transitions from the LPI mode to normal mode. The MAC is also responsible for initiating the low power mode by sending the LPI idles (to initiate LPI mode) or normal idles (to exit the LPI mode) to the PHY. The PHY will pass through the LPI idles from the system interface to the media interface and vice versa.

2.15.1.3 10BASE-Te

10BASE-Te reduces power consumption by reducing the transmit amplitude. 10BASE-Te is enabled by register bit 20_0.7. When 10BASE-Te is enabled, transmit amplitude is reduced on the media interface to reduce the power consumption. 10BASE-Te capability is not part of 10/100/1000BASE-T Auto-Negotiation.

2.15.2 Energy Efficient Ethernet (EEE) Buffering for Master mode

The 88E1510/88E1518/88E1512/88E1514 devices have an built-in buffer to be used when the devices transition into Master mode EEE operation. This buffer is used to store data from a non -EEE compliant legacy MAC, when the PHY media interface is exiting the Low Power Idle (LPI) mode. The buffer basically ensures that no packets are lost by the PHY during the transition from LPI mode to normal mode of operation. Once the media interface exits the LPI mode, the data in the buffer is sent out through the media interface. The EEE buffer may be enabled by setting 0_18.0 = 1.

When the PHY in LPI mode detects data coming from the MAC interface, the LPI idles will be stopped on the media interface. This triggers the PHY to initiate a WAKE to the link partner to indicate that the data will be transmitted shortly. During this time an exit timer will enable the buffer to store the incoming data from the MAC until the media interface has completely come out of the sleep state. The exit timer values are stored in Register 1_18.

The 1000BASE-X, SGMII PCS are modified to support low power idle code groups /LI1/ and /LI2/ ordered sets. The SGMII Auto-Negotiation configuration code groups contain additional two bits to communicate EEE statuses through in-band SGMII Auto-Negotiation (See Table 38, Enhanced SGMII PHY Status, on page 65)

Note The slave and the Master mode EEE operation must not be confused with the Master and Slave mode operation of 1000BASE-T

2.15.3 Energy Efficient Ethernet Auto-Negotiation

In order for the EEE to work both the local PHY and its link partner needs to support EEE. The EEE capabilities are exchanged through standard 10/100/1000BASE-T Auto-Negotiation (IEEE 802.3 Clauses 28 and 40). These capabilities are exchanged through the Next Page exchanges. The Auto-Negotiation process is used only for the exchange of speed and duplex information and not any timer information with regards to the sleep, refresh and wake cycles. 10BASE-Te capability is not part of the 10/100/1000BASE-T Auto-Negotiation.

The device implements Energy Efficient Ethernet (EEE) functions based on IEEE 802.3az-2010. The device supports EEE on the following System and Media Interfaces:

- 10BASE-Te
- 100BASE-TX
- 1000BASE-T

The EEE registers are defined in Clause 22 Page 18 registers and Clause 45 XMDIO space. Refer to “PHY XMDIO Register Description” on page 226 for details.

2.16 CRC Error Counter and Frame Counter

The CRC counter and packet counters, normally found in MACs, are available in the device. The error counter and packet counter features are enabled through register writes and each counter is stored in eight register bits.

Register 18_18.2:0 controls which path the CRC checker and packet counter is counting.

If register 18_18.2:0 is set to 010 then the Copper receive path is checked.

If register 18_18.2:0 is set to 100 then the SGMII input path is checked.

If register 18_18.2:0 is set to 110 then the RGMII input path is checked.

2.16.1 Enabling The CRC Error Counter and Packet Counter

To enable the counters to count, set register 18_18.2:0 to a non-zero value.

To disable the counters, set register 18_18.2:0 to 000.

To read the CRC counter and packet counter, read register 17_18.

17_18.15:8 (Frame count is stored in these bits)

17_18.7:0 (CRC error count is stored in these bits)

The CRC counter and packet counter do not clear on a read command. To clear the counters, write Register 18_18.4 = 1. The register 18_18.4 is a self-clear bit. Disabling the counters by writing register 18_18.2:0 to 000 will also reset the counters.

2.17 Packet Generator

The device contains a very simple packet generator. Register 16_18.7:5 lists the device Packet Generator register details.

When 16_18.7:5 is set to 010 packets are generated on the copper transmit path.

When 16_18.7:5 is set to 100 packets are generated on the SGMII transmit path.

When 16_18.7:5 is set to 110 packets are generated on the RGMII transmit path.

Once enabled, fixed length packets of 64 or 1518 bytes (including CRC) will be transmitted separated by 12 bytes of IPG.The preamble length will be 8 bytes. The payload of the packet is either a fixed 5A, A5, 5A, A5 pattern or a pseudo random pattern. A correct IEEE CRC is appended to the end of the packet. An error packet can also be generated.

The registers are as follows:

16_18.7:5 Packet generation enable. 000 = Normal operation, Else = Enable internal packet generator.

16_18.2 Payload type. 0 = Pseudo random, 1 = Fixed 5A, A5, 5A, A5,...

16_18.1 Packet length. 0 = 64 bytes, 1 = 1518 bytes

16_18.0 Error packet. 0 = Good CRC, 1 = Symbol error and corrupt CRC.

16_18.15:8 Packet Burst Size. 0x00 = Continuous, 0x01 to 0xFF = Burst 1 to 255 packets.

If register 16_18.15:8 is set to a non-zero value, then register 16_18.7:5 will self clear once the required number of packets are generated. Note that if register 16_18.7:5 is manually set to 0 while packets are still bursting, the bursting will cease immediately once the current active packet finishes transmitting. The value in register 16_18.15:8 should not be changed while 16_18.7:5 is set to a non-zero value.

2.18 RX_ER Byte Capture

Whenever there is an RX_ER in the internal GMII interface the PHY will capture 4 bytes before the RX_ER is asserted. Once the bytes preceding the RX_ER assertion are captured into the registers, they will not be over written by new errors and they will only be cleared after the registers are read.

The capture register for the copper path is register 20_2. The capture register for the fiber path is register 26_18. The one for the RGMII path is register 20_4. The description below applies to the copper/fiber path and the RGMII paths but refers to register 26_18 only. Register 20_4 should be used when accessing the RGMII path and 20_2 should be used when accessing the copper path.

Once an error event is captured register 26_18.15 is set to 1 indicating that the capture data is valid. No further errors are captured until all captured registers are read. Register 26_18.13:12 is set to 00. Register 26_18.9:0 outputs the byte that is the earliest received. Once register 26_18 is read register 26_18.13:12 increments and register 26_18.9.0 is updated with the next earliest byte. The register is incremented and byte updated until the fourth read occurs. After the fourth read to register 26_18 is completed, register 26_18.15 is set to 0 and the error capturing resumes four RX_CLK cycles after the final read is completed. The 4 RX_CLK cycle delay is required to insure that the register has 4 valid bytes loaded prior to being frozen. Note that a side effect of doing this is the RX_ER may be high in the captured bytes.

Table 43: Error Byte Capture

Register	Function	Setting
26_18.15	Capture Data Valid	1 = Bits 14:0 Valid 0 = Bits 14:0 Invalid
26_18.13:12	Byte Number	00 = 4 bytes before RX_ER asserted 01 = 3 bytes before RX_ER asserted 10 = 2 bytes before RX_ER asserted 11 = 1 byte before RX_ER asserted The byte number increments after every read when register 26_18.15 is set to 1.
26_18.9	RX_ER	RX Error. Normally this bit will be low since the capture is triggered by RX_ER being high. However, it is possible to see an RX_ER high when the capture is re-enabled after reading the fourth byte and there happens to be a long sequence of RX_ER when the capture restarts.
26_18.8	RX_DV	RX Data Valid
26_18.7:0	RXD[7:0]	RX Data

2.19 1.25G PRBS Generator and Checker

A PRBS generator and checker are available for use on the 1.25G SERDES. PRBS7,PRBS23, and PRBS31 are supported.

A 32-bit checker is implemented. Note that the reads are atomic. A read to the LSB will update the MSB register. The counters only clear when register 23_1.4 is set to 1. This bit self clears.

The checker and generator polarity can be inverted by setting registers 23_1.7 and 23_1.6 respectively.

Register 23_1.5 controls whether the checker has to lock before counting commences.

Table 44: 1.25 GHz SERDES PRBS Registers

Register	Function	Setting
23_1.7	Invert Checker Polarity	0 = Invert 1 = Normal
23_1.6	Invert Generator Polarity	0 = Invert 1 = Normal
23_1.5	PRBS Lock	0 = Counter Free Runs 1 = Do not start counting until PRBS locks first
23_1.4	Clear Counter	0 = Normal 1 = Clear Counter
23_1.3:2	Pattern Select	00 = PRBS 7 01 = PRBS 23 10 = PRBS 31 11 = Generate 1010101010...pattern
23_1.1	PRBS Checker Enable	0 = Disable 1 = Enable
23_1.0	PRBS Generator Enable	0 = Disable 1 = Enable
24_1.15:0	PRBS Error Count LSB	A read to this register freezes register 25_1. Cleared only when register 23_1.4 is set to 1.
25_1.15:0	PRBS Error Count MSB	This register does not update unless register 24_1 is read first. Cleared only when register 23_1.4 is set to 1.

2.20 MDI/MDIX Crossover

The device automatically determines whether or not it needs to cross over between pairs as shown in Table 45 so that an external crossover cable is not required. If the device interoperates with a device that cannot automatically correct for crossover, the device makes the necessary adjustment prior to commencing Auto-Negotiation. If the device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 clause 40.4.4 determines which device performs the crossover.

When the device interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, the device follows the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the device uses signal detect to determine whether or not to crossover.

The auto MDI/MDIX crossover function can be disabled via register 16_0.6:5.

The pin mapping in MDI and MDIX modes is shown in Table 45.

Table 45: Media Dependent Interface Pin Mapping

Pin	MDI			MDIX		
	1000BASE-T	100BASE-TX	10BASE-T	1000BASE-T	100BASE-TX	10BASE-T
MDIP/N[0]	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDIP/N[1]	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDIP/N[2]	BI_DC±	unused	unused	BI_DD±	unused	unused
MDIP/N[3]	BI_DD±	unused	unused	BI_DC±	unused	unused

Note: Table 45 assumes no crossover on PCB.

The MDI/MDIX status is indicated by Register 17_0.6. This bit indicates whether the receive pairs (3,6) and (1,2) are crossed over. In 1000BASE-T operation, the device can correct for crossover between pairs (4,5) and (7,8) as shown in Table 45. However, this is not indicated by Register 17_0.6.

If 1000BASE-T link is established, pairs (1,2) and (3,6) crossover is reported in register 21_5.4, and pairs (4,5) and (7,8) crossover is reported in register 21_5.5.

2.21 Unidirectional Transmit

IEEE 802.3ah requires OAM support with unidirectional transmit capability. Unidirectional transmit allows a PHY to transmit data when the PHY does not have link due to potential issues on the receive path. 802.3ah formally requires two bits for this capability. Register 0.5 enables this capability, and 1.7 advertises this ability. This ability only applies to 10BASE-T, 100BASE-TX or 1000BASE-X. It doesn't apply to 1000BASE-T since 1000BASE-T requires a MASTER/SLAVE relationship and training with both link partners participating, which requires that link exists for any data transmit.

The device can support transmit of packets when there is no link by using register bit 16_0.10 = 1 (Force Copper Link Good) and 16_1.10 = 1(Force Fiber Link Good). This is not the official bit specified by the IEEE 802.3ah but serves the same function.

2.22 Polarity Correction

The device automatically corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes. In 100BASE-TX mode, the polarity does not matter.

In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

The polarity correction status is indicated by Register 17_0.1. This bit indicates whether the receive pair (3,6) is polarity reversed in MDI mode of operation. In MDIX mode of operation, the receive pair is (1,2) and Register 17_0.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, Register 17_0.1 only indicates polarity reversal on the pairs described above.

If 1000BASE-T link is established register 21_5.3:0 reports the polarity on all 4 pairs.

Polarity correction can be disabled by register write 16_0.1 = 1. Polarity will then be forced in normal 10BASE-T mode.

2.23 FLP Exchange Complete with No Link

Sometimes when link does not come up, it is difficult to determine whether the failure is due to the Auto-Negotiation Fast Link Pulse (FLP) not completing or from the 10/100/1000BASE-T link not being able to come up.

Register 19_0.3 is a sticky bit that gets set to 1 whenever the FLP exchange is completed but the link cannot be established for some reason. Once the bit is set, it can be cleared only by reading the register.

This bit will not be set if the FLP exchange is not completed, or if link is established.

2.24 Duplex Mismatch Indicator

When operating in half-duplex mode collisions should occur within the first 512 bit times. Collisions that are detected after this point can indicate an incorrect environment (too many repeaters in the system, too long cable) or it can indicate that the link partner thinks the link is a full-duplex link.

Registers 23_6.7:0, 23_6.15:8, 24_6.7:0, and 24_6.15:8 are 8 bit counters that count late collisions.

They will increment only when the PHY is in half-duplex mode and only applies to the copper interface. Each counter increments when a late collision is detected in a certain window as shown in Table 46. The four late collision counters will increment based on when the late collision starts. The counters clear on read. If the counter reaches FF it will not roll over.

Table 46: Late Collision Registers

Register	Function	Setting	Mode
23_6.15:8	Late Collision 97-128 bytes	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 96th to 128th bytes of the packet are transmitted.	RO, SC
		The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.	
23_6.7:0	Late Collision 65-96 bytes	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 65th to 96th bytes of the packet are transmitted.	RO, SC
		The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.	
24_6.15:8	Late Collision >192 bytes	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received after 192 bytes of the packet are transmitted.	RO, SC
		The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.	
24_6.7:0	Late Collision 129-192 bytes	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 129th to 192nd bytes of the packet are transmitted.	RO, SC
		The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.	
25_6.12:8	Late Collision Window Adjust	Number of bytes to advance in late collision window. 0 = start at 64th byte, 1 = start at 63rd byte, etc.	R/W

The real point of measurement for late collision should be done at the MAC and not at the PHY. In order to compensate for additional latency between the PHY and the MAC register 25_6.12:8 is used to move the window earlier. For example, if register 25_6.12.8 is set to 2 then the first window is 63 to 94 bytes, the second window is 95 to 129 bytes, etc. It is up to the user to program this register correctly since it is system dependent.

2.25 Link Disconnect Counter

The link disconnect counter increments every time the link transitions from up to down. This applies regardless of whether the link is a copper link or fiber link.

Register 25_18.7:0 is used as the counter. It clears on read and will not roll over when it reaches 0xFF.

2.26 LED

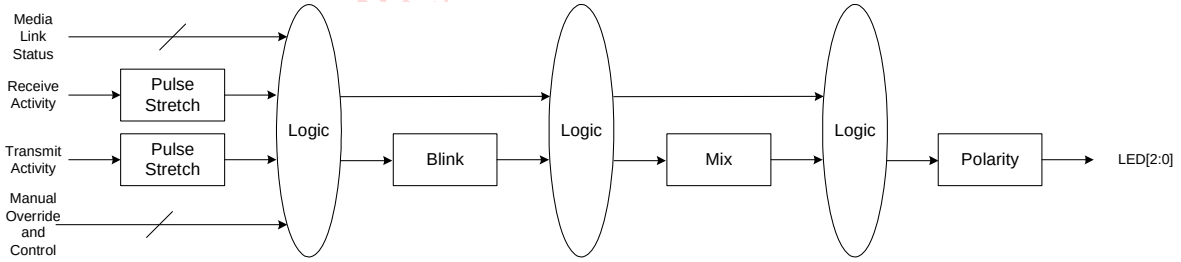
The LED[2:0] pins can be used to drive LED pins. Registers 16_3, 17_3, and 18_3 control the operation of the LED pins. LED[1:0] are used to configure the PHY per Section 2.31.1, Hardware Configuration, on page 101. After the configuration is completed, LED[1:0] will operate per the setting in 16_3.7:0.

In general, 16_3.11:8 control the LED[2] pin, 16_3.7:4 control the LED[1] pin, and 16_3.3:0 control the LED[0] pin. These are referred to as single LED modes.

However, there are some LED modes where LED[1:0] operate as a unit. These are entered when 16_3.3:2 are set to 11. These are referred to as dual LED modes. In dual LED modes, register 16_3.7:4 have no meaning when 16_3.3:2 are set to 11.

Figure 20 shows the general chaining of function for the LEDs. The various functions are described in the following sections.

Figure 20: LED Chain



2.26.1 LED Polarity

There are a variety of ways to hook up the LEDs. Some examples are shown in Figure 21. In order to make things more flexible registers 17_3.5:4, 17_3.3:2, and 17_3.1:0 specify the output polarity for the LED[2:0]. The lower bit of each pair specifies the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z.

Figure 21: Various LED Hookup Configurations

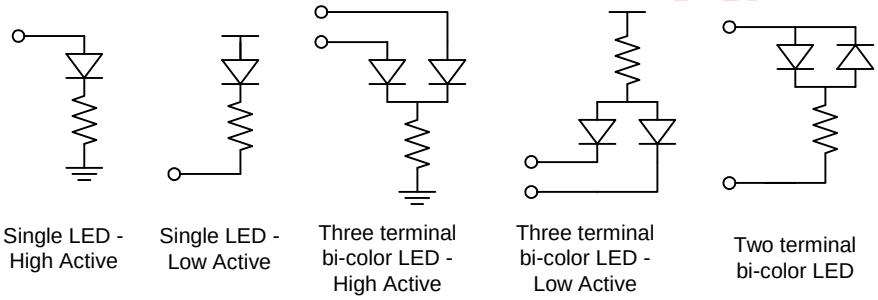


Table 47: LED Polarity

Register	Pin	Definition
17_3.5:4	LED[2] Polarity	00 = On - drive LED[2] low, Off - drive LED[2] high 01 = On - drive LED[2] high, Off - drive LED[2] low 10 = On - drive LED[2] low, Off - tristate LED[2] 11 = On - drive LED[2] high, Off - tristate LED[2]
17_3.3:2	LED[1] Polarity	00 = On - drive LED[1] low, Off - drive LED[1] high 01 = On - drive LED[1] high, Off - drive LED[1] low 10 = On - drive LED[1] low, Off - tristate LED[1] 11 = On - drive LED[1] high, Off - tristate LED[1]
17_3.1:0	LED[0] Polarity	00 = On - drive LED[0] low, Off - drive LED[0] high 01 = On - drive LED[0] high, Off - drive LED[0] low 10 = On - drive LED[0] low, Off - tristate LED[0] 11 = On - drive LED[0] high, Off - tristate LED[0]

2.26.2 Pulse Stretching and Blinking

Register 18_3.14:12 specify the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require blinking instead of a solid on. Register 18_3.10:8 specify the blink rate. Note that the pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

The stretched/blinked output will then be mixed if needed (Section 2.26.3) and then inverted/Hi-Z according to the polarity described in section (Section 2.26.1).

Table 48: Pulse Stretching and Blinking

Register	Pin	Definition
18_3.14:12	Pulse stretch duration	000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
18_3.10:8	Blink Rate	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved

2.26.3 Bi-Color LED Mixing

In the dual LED modes the mixing function allows the 2 colors of the LED to be mixed to form a third color. This is useful since the PHY is tri-speed and the three colors each represent one of the speeds. Register 17_3.15:12 control the amount to mix in the LED[1] pin. Register 17_3.11:8 control the amount to mix in the LED[0] pin. The mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

Note that there are two types of bi-color LEDs. There is the three terminal type and the 2 terminal type. For example, the third and fourth LED block from the left in Figure 21 illustrates three terminal types, and the one on the far right is the two terminal type. In the three terminal type both of the LEDs can be turned on at the same time. Hence the sum of the percentage specified by 17_3.15:12 and 17_3.11:8 can exceed 100%. However, in the two terminal type the sum should never exceed 100% since only one LED can be turned on at any given time.

The mixing only applies when register 16_3.3:0 are set to 11xx. There is no mixing in single LED modes.

Table 49: Bi-Color LED Mixing

Register	Function	Definition
17_3.15:12	LED[1] mix percentage	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
17_3.11:8	LED[0] mix percentage	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5%, . . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved

2.26.4 Modes of Operation

The LED pins relay some modes of the PHY so that these modes can be displayed by the LEDs. Most of the single LED modes are self-explanatory from the register map of register 16_3. The non-obvious ones are covered in this section.

Table 50: Modes of Operation

Register	Pin	Definition
16_3.11:8	LED[2] Control	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On- Full Duplex, Blink- Collision, Off- Half Duplex 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10/1000 Mbps Link, Off - Else 0111 = On - 10 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
16_3.7:4	LED[1] Control	If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On- Receive, Off- No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On- 100 Mbps Link/ Fiber Link 0110 = On - 100/1000 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
16_3.3:0	LED[0] Control	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 1 blink - 10 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

2.26.4.1 Compound LED Modes

Compound LED modes are defined in Table 51.

Table 51: Compound LED Status

Compound Mode	Description
Activity	Transmit Activity OR Receive Activity
Link	10BASE-T link OR 100BASE-TX Link OR 1000BASE-T Link

2.26.4.2 Speed Blink

When 16_3.3:0 is set to 0010 the LED[0] pin takes on the following behavior.

LED[0] outputs the sequence shown in Table 52 depending on the status of the link. The sequence consists of 8 segments. If a 1000 Mbps link is established the LED[0] outputs 3 pulses, 100 Mbps 2 pulses, 10 Mbps 1 pulse, and no link 0 pulses. The sequence repeats over and over again indefinitely.

The odd numbered segment pulse duration is specified in 18_3.1:0. The even numbered pulse duration is specified in 18_3.3:2.

Table 52: Speed Blinking Sequence

Segment	10 Mbps	100 Mbps	1000 Mbps	No Link	Duration
1	On	On	On	Off	18_3.1:0
2	Off	Off	Off	Off	18_3.3:2
3	Off	On	On	Off	18_3.1:0
4	Off	Off	Off	Off	18_3.3:2
5	Off	Off	On	Off	18_3.1:0
6	Off	Off	Off	Off	18_3.3:2
7	Off	Off	Off	Off	18_3.1:0
8	Off	Off	Off	Off	18_3.3:2

Table 53: Speed Blink

Register	Pin	Definition
18_3.3:2	Pulse Period for even segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
18_3.1:0	Pulse Period for odd segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

2.26.4.3 Manual Override

When 16_3.11:10, 16_3.7:6, and 16_3.3:2 are set to 10 the LED[2:0] are manually forced. Registers 16_3.9:8, 16_3.5:4, and 16_3.1:0 then select whether the LEDs are to be on, off, Hi-Z, or blink.

If bi-color LEDs are used, the manual override will select only one of the 2 colors. In order to get the third color by mixing MODE 1 and MODE 2 should be used (Section 2.26.4.4).

2.26.4.4 MODE 1, MODE 2, MODE 3, MODE 4

MODE 1 to 4 are dual LED modes. These are used to mix to a third color using bi-color LEDs.

When 16_3.3:0 is set to 11xx then one of the 4 modes are enabled.

MODE 1 – Solid mixed color. The mixing is discussed in Section 2.26.3.

MODE 2 – Blinking mixed color. The mixing is discussed in Section 2.26.3. The blinking is discussed in section Section 2.26.2.

MODE 3 – Behavior according to Table 54.

MODE 4 – Behavior according to Table 55.

Note that MODE 4 is the same as MODE 3 except the 10 Mbps and 100 Mbps are reversed.

Table 54: MODE 3 Behavior

Status	LED[1]	LED[0]
1000 Mbps Link - No Activity	Off	Solid On
1000 Mbps Link - Activity	Off	Blink
100 Mbps Link - No Activity	Solid Mix	Solid Mix
100 Mbps Link - Activity	Blink Mix	Blink Mix
10 Mbps Link - No Activity	Solid On	Off
10 Mbps Link - Activity	Blink	Off
No link	Off	Off

Table 55: MODE 4 Behavior

Status	LED[1]	LED[0]
1000 Mbps Link - No Activity	Off	Solid On
1000 Mbps Link - Activity	Off	Blink
100 Mbps Link - No Activity	Solid On	Off
100 Mbps Link - Activity	Blink	Off
10 Mbps Link - No Activity	Solid Mix	Solid Mix
10 Mbps Link - Activity	Blink Mix	Blink Mix
No link	Off	Off

2.27 CLK125

The CLK125 output supplies a 125 MHz clock that can be used to clock other digital logic. The CLK125 should not be used as an input to devices that require a higher quality clock.

Register 16_2.1 is used to disable/enable the CLK125 output pin, where register 16_2.1 = 1 disables the CLK125 output pin by tristating it and 16_2.1 = 0 enables the current selected clock to go out. The default value of 16_2.1 is 0 on power on reset or hardware reset. The CLK125 output will not glitch when going in or out of tristate.

The CLK125 can be in one of two states: hardware reset or normal operation. When transitioning between states, the CLK125 will not glitch.

Hardware Reset State

When hardware reset is asserted the CLK125 outputs a 25 MHz copy of the XTAL_IN clock.

Normal Operation

Two sources (an internally generated 125 MHz clock or SyncE clock) can be selected to drive the CLK125 output. Register 16_2.0 = 1 will output the SyncE clock and register 16_2.0 = 0 will output internally generated 125 MHz clock. The default value of 16_2.0 is 0 for power on reset or hardware reset.

When register 16_2.0 = 0 (an internally generated 125 MHz clock is selected), the CLK125 outputs a 125 MHz clock if register 16_2.2 is set to 0. The CLK125 will continue to toggle when the PHY enters the power down state (register 0_0.11 = 1) or in energy detect state. When register 16_2.2 is set to 1, the CLK125 signal is held low. The default value of 16_2.2 is 0 on power on reset or hardware reset.

2.27.1 Synchronous Ethernet Recovered Clock

When register 16_2.0 = 1 (SyncE clock is selected), the CLK125 outputs either a 125 MHz or 25 MHz clock that is based on the 125 MHz recovered clock on the copper receive path when linked up in1000BASE-T or 100BASE-TX. If a 25 MHz clock is selected, the 125 MHz recovered clock is internally divided by 5.

Register 16_2.11 selects whether the CLK125 outputs 25 MHz based on the XTAL clock or drives LOW when the link is down or when the copper receiver is linked to 10BASE-T. The default value of 16_2.11 is 0 on power on reset or hardware reset.

- 0 = CLK125 outputs 25 MHz XTAL clock during link down or 10BASE-T
- 1 = CLK125 drives LOW during link down or 10BASE-T

Setting register 16_2.10 to 1 allows the recovered clock to go out on the CLK125. When register 16_2.10 is set to 0, the recovered clock is held low. The default value of 16_2.10 is 1 on power on reset or hardware reset.

Register 16_2.12 selects whether the CLK125 outputs 25 MHz or 125 MHz(0 = 25 MHz, 1 = 125 MHz). The default value of 16_2.12 is 0 on power on reset or hardware reset.

Synchronous Ethernet recovered clock support is provided when the device is operating in 1000BASE-X or 100BASE-FX on the line interface. The CLK125 pin is used to output the recovered clock. Refer to Section 2.27, CLK125, on page 89 for configuring the CLK125 pin as recovered clock output. When the device is configured in SLAVE mode of operation, the CLK125 will output the recovered clock from the line interface. If the device is configured in 1000BASE-T MASTER mode of operation, the CLK125 will output the clock based on the XTAL.

2.28 Precise Timing Protocol (PTP) Time Stamping Support

Precise Time Protocol (PTP) is used by IEEE specifications to determine the time of day for systems across a network. The IEEE specifications are IEEE 802.1AS, IEEE 1588 version 1, and IEEE 1588 version 2. The PTP protocol is typically used in audio video bridging (PTP) applications, or industrial and test automation applications.

The fundamental concept is to be able to time stamp the PTP frames with high precision as close to the physical wires as possible. As such, doing the time stamping in the PHY increases the accuracy compared to doing it in the MAC or higher layers since the MAC interface FIFOs can add up to ±2 bytes of uncertainty.

The PTP core in the device consists of two sub-cores, namely the Packet Time Stamping and the Time Application Interface (TAI). The time stamping core supports time stamping of frame formats as defined in IEEE 802.1AS, IEEE 1588v1, and IEEE1588v2 frames. c

2.28.1 PTP Control

To support the PTP Time Stamping function, the device has four pins that are global to the entire PHY.

- PTP clock input pin (The CONFIG pin is used for this purpose.)
- PTP Event Request input pin (The LED[1] pin is used for this purpose)
- PTP Trigger Generate output pin (The LED[1][1] pin is used for this purpose)
- Interrupt Pin (The LED[2] pin is used for this purpose)

2.28.1.1 PTP Clock Input

The PTP clock input is an option to use an external clock for the Time of Day counter instead of the free running internal clock. Register 20_6.8 is used to select the clock source. After configuration is completed and the external clock source is enabled (Register 20_6.8 = 1), the CONFIG pin is used as the external 125 MHz reference clock input.

Note

Because LED[1] pin is also used for PTP Event Request input, the PTP Trigger Generate output feature can never be used at the same time.

2.28.1.2 PTP Event Request

The PTP Event Request input pin can be configured to capture an external event (referred to as EventReq) and record the time at which the event occurred using the PTP Global Time Register (PTP Global Time Register - Page 12, Registers 14 and 15). Users must program 20_6.7 to 1 to enable this function. The definition of an external event is a low to high transition on the LED[1] pin. The event time is captured in EventCapRegister (Event Capture Register, Page 12, Register 10 and 11). This field is validated by EventCapValid bit (TAI Global Configuration Register 9, Page 12, Register 9).

2.28.1.3 PTP Trigger Generate

The PTP Trigger Generate output pin is used to output an external signal (referred to as TrigGenResp) when the internal Time of Day counter matches a value programmed into a PHY register. When there is a match this output will go from low to high. The LED[1] pin is used for this function. It is selected by setting register 20_6.6 = 1.

1. Refer to Section 2.26, LED, on page 83 for further details on LED[1] pin.

2.28.1.4 PTP Control Register

The PTP circuit timestamps packets as it passes through the PHY. The register control to this function can be accessed via pages 8, 9, 12, and 14. The PTP circuit can be powered down when it is not used via register 20_6.9. When register 20_6.9 is set to 1 the registers in pages 8, 9, 12, and 14 are not accessible since the entire circuit is powered down.

By default Register 20_6.9 is set to 1. Register 20_6.9 must be set to 0 to enable PTP.

Table 56: PTP Control Register

Register	Function	Setting
20_6.9	PTP Power Down	1 = Power Down 0 = Power Up
20_6.8	PTP Reference Clock Source	1 = Use 125 MHz clock supplied to the CONFIG pin 0 = Use internal 125 MHz clock
20_6.7	PTP Input Source	1 = Use LED[1] pin for PTP Event Request input 0 = Force input to 0
20_6.6	PTP Output Source	1 = Use LED[1] pin for PTP Trigger Generate Output 0 = Use LED[1] for non-PTP functions.
20_6.6:0	Reserved	Reserved

2.28.2 Packet Time Stamping

The device supports two sets of hardware arrival time stamp registers to be able to capture two different PTP event messages' time stamp before the CPU reads the time stamp registers out of the device. For every incoming PTP message type either PTPArr0Time (PTP Arrival 0 Time Registers - Page 8, Registers 9 and 10) or PTPArr1Time (PTP Arrival 1 Time Registers - Page 8, Registers 13 and 14) registers can be chosen by configuring TSArrPtr (PTP Global Configuration Register 2 - Page 14, Register 2). The SequenceID from the PTP Common header is captured as part of Arrival 0, Arrival 1 and/or Departure time stamp register sets so software can correlate the collected time stamps with the received or transmitted PTP event message. Hardware can be enabled to generate an interrupt upon capturing the time stamp information by writing a 0x1 to the interrupt enable register bits PTPArrIntEn (PTP Port Configuration Register 2 - Page 8, Register 2) for incoming PTP event messages or PTPDepIntEn (PTP Port Configuration Register 2 - Page 8, Register 2) for outgoing PTP event messages. In addition to generating an interrupt on the interrupt pin, an interrupt status (PTPArr0IntStatus, PTPArr1IntStatus, and PTPDepIntStatus) gets generated which indicates if there were to be an error related to the time stamp register. The interrupt status gets set to 0x1 when the time stamp counter gets overwritten before the previous time stamp registers have been read out. The interrupt status gets set to a 0x2, when a time stamp could not be captured for a PTP event message because DisTSOverwrite (PTP Port Configuration Register - Page 8, Register 0) is set to a 0x1.

Given that the device registers are accessed in units of 16-bits, to retain the entire 32-bit time stamp and the associated error messages and the SequenceID for a given PTP frame, the hardware treats the Arrival 0 block of registers (Page 8, Registers 8 through 11), Arrival 1 block registers (Page 8, Registers 12 through 15) and Departure block registers (Page 9, Registers 0 through 3) as a group and atomic operations are supported for these block of registers.

It is important to note that the device does not alter the contents of any PTP packet in either the ingress or egress directions. Time stamping at the device level does not involve adding a time stamp to a packet or changing its CRC. It also does not involve the device looking at time stamps that are

embedded within a packet. The PHY does not add any additional latency when the PTP function is enabled. The PHY only identifies that a packet is a PTP frame and records the enter and exit time. The PHY does this by parsing the packet for certain fields as described in later sections. If the packet is identified as such a PTP packet, then the device loads the value of an internal “time of day counter” to a register showing the time for the first byte or SFD of the packet. The device then can inform the CPU or the PTP higher level firmware/software that such an event happened by activating an interrupt pin. The CPU can then read the relevant registers to find out if the event was in the RX or TX directions and the value of the “time of day counter” when the event happened.

Using the above time information and following the PTP protocol, the CPU or higher level entity can then determine the offset in time of day between a grand master clock and the SLAVE node, as well as the frequency difference between the Grand Master Clock and the SLAVE clock in case they are not frequency locked. These calculations are above the PHY level. The PHY provides full flexibility by allowing its time of day counter to be adjusted based on the CPU’s calculations, as well as a totally new time of day value to be entered. The CPU can also use the time information provided by the PHY to create PTP packets that inform the link partners or the Grand Master when the packets had arrived or left the port in question.

The maximum jitter associated with capturing the time stamps collected by the logic is one TSClkPer (TAI Global Configuration Register 1 - Page 12, Register 1). Note that there are inherent delay variation introduced in PHY layer pipelines both in receive and transmit direction which add to the overall jitter of the time stamps collected by the hardware and frequency/phase computations done in PTP protocol software.

For achieving higher accuracies in terms of PTP, it is recommended that an external clock device is used to adjust the time stamping clock with the frequency/phase offset information computed in PTP protocol software. The frequency and/or phase adjusted clock can in turn be fed back into the device to be used by the time stamping logic.

2.28.3 Time Application Interface (TAI)

The Precise Timing Protocol provides both frequency and time-of-day with respect to the PTP Grand Master for the entire PTP network. In a given endpoint device (media talker or a media listener), once the PTP Grand Master aware clock and time are available, it needs to be transported over to the rest of the subsystem without loss of accuracy. For example, if a Digital Video Recorder is the end device, the network clock and time needs to be transported to the Video SoC and/or Storage SoC and the host processor seamlessly. This ensures that when the media is played out of the DVR, the network time aware presentation time of the content is required to be carried through.

The TAI “Timing Interface Block” supports features required for the above purpose. This block utilizes two signals to offer various services. One signal is called EventRequest input signal and the second is called TriggerGenerate output signal.

Using the above signals there are several functions that this block supports:

1. An event pulse capture function.
2. Multiple event counter function.
3. A trigger pulse generate function with pulse width control.
4. A trigger clock generate function with digital clock compensation.
5. A PTP global time increment and/or decrement function.
6. A multi-ptp device time sync function.

2.28.3.1 Event pulse capture interface

In many IEEE 1588 applications like industrial automation etc. it is important to precisely capture the time at which a particular event has happened. The event is defined by a low to high transition on an external signal called EventRequest. The event time is captured in EventCapRegister (Page 12,

Register 10 and 11). This field is validated by EventCapValid bit (TAI Global Configuration Register 9, Page 12, Register 9).

The captured event time register needs to be read out by software and valid bit cleared before the hardware captures another event. If there were to be two back to back events before the software read the results of the first event an error indication is set in EventCapErr (TAI Global Configuration Register 9 - Page 12, Register 9). If the user chooses that the hardware rather overwrite the Event capture register then it can be configured by setting a 0x1 to EventCapOv (TAI Global Configuration Register 0 - Page 12, Register 0).

Once an event has been captured the software can optionally (EventCapIntEn, Page 12, Register 0) be interrupted and an EventInt (Page 12, Register 9) bit is also set.

The maximum jitter associated with capturing the EventRequest signal pulse is one TSClkPer (TAI Global Configuration, Register 1 - Page 12, Register 1). The minimum pulse width of the EventRequest signal needs to be 1.5 times the TSClkPer (TAI Global Configuration, Register 1 - Page 12, Register 1). In order for the hardware logic to detect distinct events on the EventRequest signal, the minimum gap between two events needs to be 150 ns plus 5 times TSClkPer amount.

2.28.3.2 Multiple Event Counter Function

Similar to the Event Pulse capture interface described above, if multiple events need to be captured for an application to detect how many times a particular event is happening on the EventRequest input signal, EventCtrStart (TAI Global Configuration Register - Page 12, Register 0) needs to be set to a 0x1 and EventCapOv (TAI Global Configuration Register - Page 12, Register 0) needs to set to a 0x1.

The Multiple Event Counter function is capable of capturing up to 255 events in EventCapCtr (TAI Global Configuration Register 9 - Page 12, Register 9).

The maximum jitter associated with capturing the EventRequest signal pulse is one TSClkPer (TAI Global Configuration Register 1 - Page 12, Register 1). The minimum pulse width of the EventRequest signal needs to be 1.5 times the TSClkPer (TAI Global Configuration Register 1 - Page 12, Register 1). In order for the hardware logic to detect distinct events on the EventRequest signal, the minimum gap between two events needs to be 150 ns plus 5 times TSClkPer amount.

Note

In the multiple event counter mode, the EventCapRegister (Page 12, Registers 10 and 11) indicate the time stamp value for the last captured event register.

2.28.3.3 Trigger Pulse Generate Function

In many PTP applications, the time of day computed in PTP needs to be distributed in some form to the rest of the node. One commonly used method is to generate a pulse whenever the PTP Global Time matches certain configured value. The pulse gets output on an TrigGenResp output signal.

The above function can be achieved by:

a) Configuring the TrigGenReq (TAI Global Configuration Register 0 - Page 12, Register 0) to a 0x1 and
b) Configuring the TrigMode (TAI Global Configuration Register 0 - Page 12, Register 0) to 0x1 and
c) Configuring the time amount when the pulse needs to be generated in TrigGenAmt (TAI Global Configuration Register 2 - Page 12, Register 2 and 3).

The PTP Global Timer gets compared to the TrigGenAmt and upon a match a pulse signal gets generated on the TrigGenResp output signal.

Optionally after generating the TrigGenResp pulse the CPU can be notified by setting the TrigGenIntEn (TAI Global Configuration Register 0, Page 12, Register 0) and along with the pulse output, TrigGenInt (TAI Global Configuration Register 8, Page 12, Register 8) bit gets set. Upon receiving the interrupt, it is the CPUs job to clear the interrupt bit.

The pulse width of the output signal can be controlled by PulseWidth (TAI Global Configuration Register 5 - Page 12, Register 5). Do not set the PulseWidth to a zero value.

2.28.3.4 Trigger Clock Generate Function

Similar to the trigger pulse generation function described above, the same set of registers can be used to generate a periodic clock. The value specified in TrigGenAmt (TAI Global Configuration Register 2 - Page 12, Register 2 and 3) is used to generate the base period of the clock output. For this functional mode the TrigMode (TAI Global Configuration Register 0 - Page 12, Register 0) needs to be set a 0x0 and TrigGenReq (TAI Global Configuration Register 0 - Page 12, Register 0) needs to be set to a 0x1.

The output clock can be compensated by configuring the field TrigClkComp (TAI Global Configuration Register 4 - Page 12, Register 4). This field specifies the remainder amount for the clock that is being generated with the period specified by the TrigGenAmt. The TrigClkComp amount gets constantly accumulated and when this accumulated amount exceeds the value specified in TSClkPer, a TSClkPer gets added to the output clock momentarily to compensate for the remainder accumulated over time.

Note The TrigGenAmt should be set to no less than 2 times the TSCLKPer amount.

2.28.3.5 PTP Global Time Increment/Decrement Function

As stated earlier, the Time of Day counter for the PTP is kept partially in hardware 32-bit ns part and the 64-bit seconds part is kept in software. As every PTP slave node constantly computes the time of day, it needs to adjust its hardware with the updated phase offset information. The PTP core assists by providing a PTP Global Timer adjustment functions.

For an increment operation:

a) Set TimeIncDecOp (TAI Global Configuration Register 5 - Page 12, Register 5) to a 0x0 and
b) Configure the TimeIncDecAmt (TAI Global Configuration Register 5 - Page 12, Register 5) to whatever value that needs to be added to the current PTP Global Time value.
c) Enable the TimeIncDecEn (TAI Global Configuration Register 0 - Page 12, Register 0) to a 0x1,

For an decrement operation:

a) Set TimeIncDecOp (TAI Global Configuration Register 5 - Page 12, Register 5) to a 0x1 and
b) Configure the TimeIncDecAmt (TAI Global Configuration Register 5 - Page 12, Register 5) to whatever value that needs to be subtracted to the current PTP Global Time value.
c) Enable the TimeIncDecEn (TAI Global Configuration Register 0 - Page 12, Register 0) to a 0x1

Given that TimeIncDecAmt is only a 11-bit parameter and the PTP Global Timer is 31 bits wide, multiple iterations of the operation need to be performed to get to the adjusted time of day value.

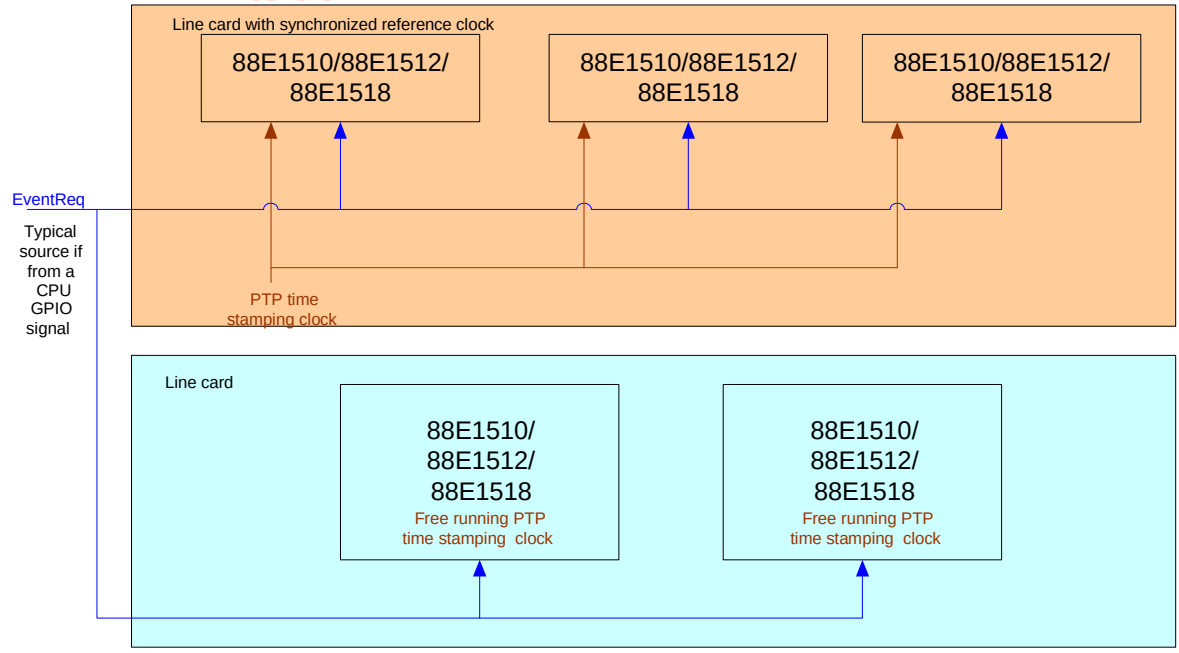
2.28.3.6 Multi-PTP device time sync Function

When PTP is enabled on devices on enterprise, service provider line cards and/or chassis, it is important for various PTP capable devices on the system to have the common notion of PTP Global Time. Typically a central processing card is present in these chassis which runs the PTP software for

the entire chassis and all the data line cards send the PTP frames and the time stamp information to the central PTP software entity. Given that there can be so many ports on each line card and each of the line cards may be plugged into the chassis at different times, the PTP global Time counter value in each of the PTP devices on the line cards may not be synchronized. The PTP Global Timer increment/decrement operations cannot be used for this as the inherent programming delay uncertainties introduced due to CPU interface protocols like MDC/MDIO. Thus the hardware needs to provide a sure shot way for all the PTP capable devices across various line cards regardless of when the line cards have been powered on, to be synchronized to the same PTP Global Time so that the PTP protocol software doesn't have to remember the offsets with respect to the PTP Grand Master and also with respect to each of these devices.

The background for this feature is that the PTP nodes derive the time of day via PTP message exchange. The derived time of day consists of 64 bits of seconds and 32 bits of nanoseconds. The PTP slave nodes are expected to derive the frequency and phase offset information with respect to the PTP Grand Master node. The derived offset information is used to periodically adjust various device PTP global timer values. In a system with a single PTP device, the PTP Global Timer increment/decrement functions are provided to achieve this. For multi PTP (Marvell devices only) capable devices the goal is to synchronize all the nodes with a common 32-bit nanoseconds field and also adjust the nanoseconds field with the computed PTP Grand Master offset information.

Figure 22: Multiple devices across multiple line cards connected by an EventReq input signal



This feature is enabled by setting a 0x1 to MultiPTPSyncMode (TAI Global Configuration Register 0 - Page 12, Register 0). Note that once this bit is enabled, the functions EventRequest, TriggerGen and TimeIncDec are disabled.

When MultiPTPSyncMode is 0x1, a low to high transition on the EventRequest signal triggers transfer of TrigGenAmt to the PTP Global Timer register. At the timer of the low to high transition for further software time correlation, the EventCapTime register is also updated with the value of the PTP Global Time before it got overwritten.

Note that even though the above schema ensures that the PTP Global Time register value is synchronized, the following are the possible sources of jitter associated from a system level (which can be avoided):

a) The reference clock sources for various PTP devices that support the multi-sync EventReq interface on the same line card and/or across line cards may not be synchronized.
b) The added delays in the clock path between various PTP devices that support the multi-sync EventReq interface on the same line card and/or across line cards.
c) Inherent operating system related jitter from the point a command is issued to when it actually gets executed in hardware. This is applicable for EventReq pulse generation from a GPIO as well. This tends to be more predictable with real time operating systems.

One guaranteed method to avoid the above mentioned jitter factors a and b is by using a flip-flop with the EventReq as the data input and PTP time stamping clock as the clock input into the flop and the flop output gets distributed with matched delays across various PTP devices that support the multi-sync EventReq. One method to reduce the operating system associated uncertainties is to choose an operating system in which the scheduler tasks are predictable down to 1's of nanoseconds accuracy.

2.28.4 ReadPlus Command

The PTP Global Time Registers are used as 32-bit global timer value that is running off of the free running PHY clock. A Read from the PTP Global Time Registers must be done with ReadPlus command. A Read directly to the PTP Global Time Registers without using ReadPlus command will return 0. The PTP Global Time Registers value can be loaded directly by writing back-to-back to the PTP Global Time Register Byte 3 & 2 – Page 12, Register 15 first followed by PTP Global Time Register Byte 1 & 0 – Page 12, Register 14.

To read from PTP Global Time Register:

1. Write to Reg 22 = 0xE (Page 14)
2. Write to Reg 14 = 0x8E0E (ReadPlus Command from PTP Global Time Register)
3. Read from Reg 15 (PTP Global Time Registers Bit[15:0])
4. Read from Reg 15 (PTP Global Time Registers Bit[31:16])

Note It is recommended to use the PTP Global Time Increment Decrement or Event Request function to adjust the PTP Global Time Registers instead of writing to the registers directly. If the PTP Global Time Register values are written directly to the registers, the lower 16-bits of the PTP Global Time Registers may have been wrapped around before the higher 16-bits are written.

2.29 Interrupt

When Register 18_3.7 is set to 1, LED[2] outputs the interrupt. Register 18_3.11 selects the polarity of the interrupt signal when it is active, where 18_3.11 = 1 means it is active low and 18_3.11 = 0 means it is active high.

Registers 18_0 and 18_2 are the Interrupt Enable registers for the copper media.

Registers 19_0 and 19_2 are the Interrupt Status registers for the copper media.

Register 18_1 is the Interrupt Enable register and 19_1 is the Interrupt Status register for the fiber media.

There are force bits and polarity bits for fiber and copper media See Table 57 and Table 58.

Table 57: Copper

Register	Function
18_3.15	Force Interrupt
18_3.11	Set Polarity

Table 58: Fiber

Register	Function
26_1.15	Force Interrupt
16_1.2	Set Polarity

For Auto-Media Detect (AMD) modes, copper bits should be used. If the active media is fiber then the bits in Table 58 should be used. If the active media is copper then the bits in Table 57 should be used.

2.30 Automatic and Manual Impedance Calibration

2.30.1 MAC Interface Calibration Circuit

Auto-calibration is available for the MAC interface I/Os. The PHY runs the automatic calibration circuit with a 47.3 ohm impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes. Individual NMOS and PMOS output transistors can be controlled.

Manual NMOS and PMOS settings are available if the automatic calibration is not desired. If the PCB traces are different from 47.3 ohms, the output impedance of the MAC interface I/O buffers can be programmed to match the trace impedance. Users can adjust the NMOS and PMOS driver output strengths to perfectly match the transmission line impedance and eliminate reflections completely.

2.30.2 MAC Interface Calibration Register Definitions

Table 59: RGMII Output Impedance Calibration Override
Page 2, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Restart Calibration	R/W, SC	0x0	Retain	Calibration will start once bit 15 is set to 1. 0 = Normal 1 = Restart
14	Calibration Complete	RO	0x0	Retain	Calibration is done once bit 14 becomes 1. 0 = Not done 1 = Don
13	VDDO Level	RW	See Descr.	Retain	VDDO level- must be programmed to indicate the VDDO supply voltage used for the 88E1510/88E1512/88E1514 parts. This value is a don't care for 88E1518 parts (VDDO is 1.8V). The bit mapping is: 0 = 3.3V 1 = 2.5V If the CONFIG pin input values bit 1:0 are: 00, then VDDO Level = 3.3V 11, then VDDO Level = 3.3V 10, then VDDO Level = 2.5V 01, then VDDO Level = 2.5V Note: 3.3V is assumed initially until this value is changed.
12	1.8V VDDO Used	R/O	See Descr	Retain	This bit indicates whether VDDO = 1.8V is used or not. 1 = VDDO = 1.8V 0 = VDDO = 2.5V or 3.3V
11:8	PMOS Value	R/W	See Descr	Retain	0000 = All fingers off 1111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once Register 24_2.6 is set to 1 the new calibration value is written into the I/O pad. The automatic calibrated value is lost.
7	Reserved	RW	0x0	Retain	Reserved.

Table 59: RGMII Output Impedance Calibration Override (Continued)
Page 2, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
6	Force PMOS/NMOS	R/W	0x0	Retain	1 = Force value from 24_2.11:8 to PMOS, and 24_2.3:0 to NMOS. (Used for manual settings)
5:4	Reserved	R/O	0x0	Retain	Reserved.
3:0	NMOS value	R/W	See Descr	Retain	0000 = All fingers off 1111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once 24_2.6 is set to 1 the new calibration value is written into the I/O pad. The automatic calibrated value is lost.

Table 60: RGMII Output Impedance Target
Page 2, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
2:0	Calibration target	RW	0x3	Retain	000 = 78.8 Ohm 001 = 64.5 Ohm 010 = 54.6 Ohm 011 = 47.3 Ohm 100 = 41.7 Ohm 101 = 37.3 Ohm 110 = 33.8 Ohm 111 = 30.9 Ohm

2.30.3 Changing Auto Calibration Targets

The PHY runs the automatic calibration circuit with a 47.3 ohm impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes.

To change the auto calibration targets:

Write to register 25_2.2:0 with the target impedance and then

Write to register 24_2 = 0x8000 (Restarts the auto-calibration with the new target).

2.30.4 Manual Settings to The Calibration Registers

To use manual calibration, write to the following registers:

Write to register 24_2.11:8 = b'PPPP and register 24_2.3:0 = b'NNNN adjusts the PMOS and NMOS fingers accordingly.

Where PPPP is the 4 bit value for the PMOS strength.

Where NNNN is the 4 bit value for the NMOS strength.

PPPP or NNNN will depend on the PCB used. The '1111' value enables all the fingers for maximum drive strength and for minimum impedance. The '0000' value turns all fingers off for minimum drive strength and for maximum impedance. For assessment of the auto-calibration required on a

particular PCB, the RGMII pins at the destination can be monitored and depending on the signal integrity on the PCB the auto-calibration values can be changed accordingly. For example, if the automatic calibration has a 47.3 ohm target, and the RGMII trace impedance on the board is 60 ohms, then by monitoring the RX_CLK pin at the destination, reflections can be noticed. This is shown in Figure 23. Through manual calibration the reflections can be eliminated as shown in Figure 24.

Figure 23: Signal Reflections, using the 50 ohm setting, 60 ohm line

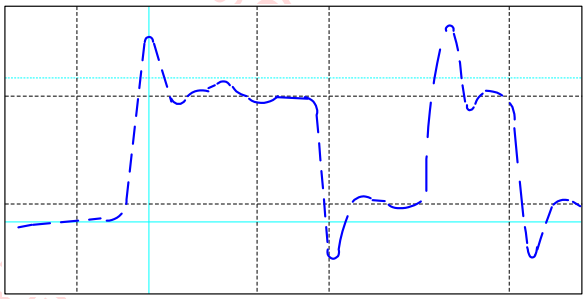
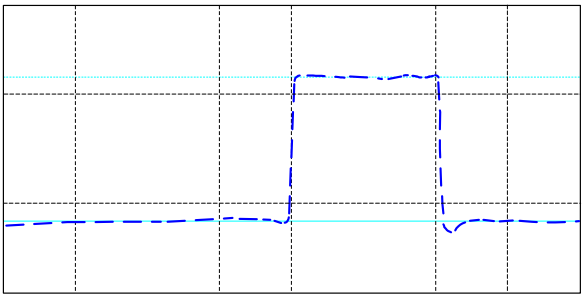


Figure 24: Clean signal after manual calibration for the 60 ohm



2.31 Configuring the 88E1510/88E1518/88E1512/88E1514 Device

The device can be configured two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

The VDDO_LEVEL configuration bit can be overwritten by software. PHYAD cannot be overwritten.

2.31.1 Hardware Configuration

After the deassertion of RESETn the device will be hardware configured.

The device is configured through the CONFIG pin. This pin is used to configure 2 bits. The 2-bit value is set depending on what is connected to the CONFIG pin soon after the deassertion of hardware reset. The 2-bit mapping is shown in Table 61.

Table 61: Two-Bit Mapping

Pin	Bit 1,0
VSS	00
LED[0]	01
LED[1]	10
LED[2]	Unused
VDDO	11

The 2 bits for the CONFIG pin is mapped as shown in Table 62.

Table 62: Configuration Mapping

Pin	CONFIG Bit1	CONFIG Bit 0	Value Assignment
CONFIG	0	0	PHYAD[0] = 0 VDDO_LEVEL[1] = 3.3V
CONFIG	1	1	PHYAD[0] = 1 VDDO_LEVEL[1] = 3.3V
CONFIG	1	0	PHYAD[0] = 0 VDDO_LEVEL[1] = 2.5V
CONFIG	0	1	PHYAD[0] = 1 VDDO_LEVEL[1] = 2.5V

1. This is valid only for 88E1510/88E1512/88E1514. For 88E1518, the VDDO_LEVEL is fixed at 1.8V, hence the bit mapping for VDDO_LEVEL is ignored.

Each bit in the configuration is defined as shown in Table 63.

Table 63: Configuration Definition

Bits	Definition	Register Affected
PHYAD[0][1]	PHY Address LSB (Bit 0)	None
VDDO_LEVEL	VDDO level at power up 1 = 2.5V 0 = 3.3V 3.3V is assumed until this bit is initialized.	24_2.13

1. PHYAD[4:1] = 0000.

2.31.2 Software Configuration - Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u Clause 22 and Clause 45 MDIO protocol. MDC is the management data clock input and, it can run from DC to a maximum rate of 12 MHz. At high MDIO fanouts the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm that pulls the MDIO high during the idle and turnaround phases of read and write operations.

Bit 0 of the PHY address is configured during the hardware reset sequence. PHY address bits[4:1] are set to "0000" internally in the device. Refer to Section 2.31.1, Hardware Configuration, on page 101 for more information on how to configure this.

Typical read and write operations on the management interface are shown in Figure 25 and Figure 26. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in Section 3, 88E1510/88E1518/88E1512/88E1514 Register Description, on page 108.

Figure 25: Typical MDC/MDIO Read Operation

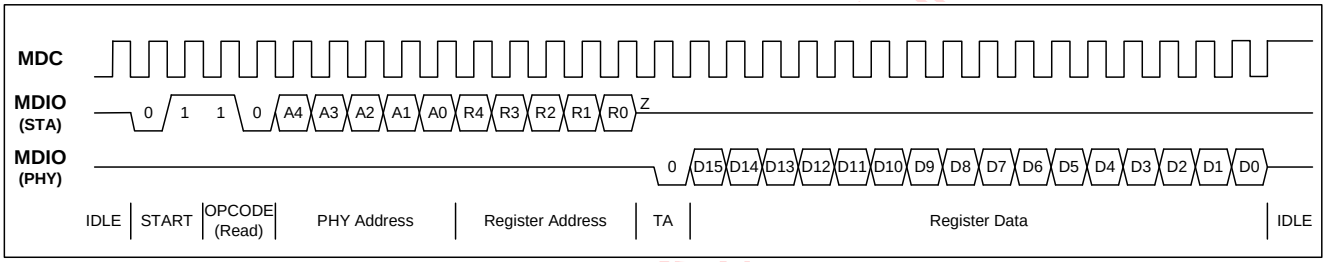


Figure 26: Typical MDC/MDIO Write Operation

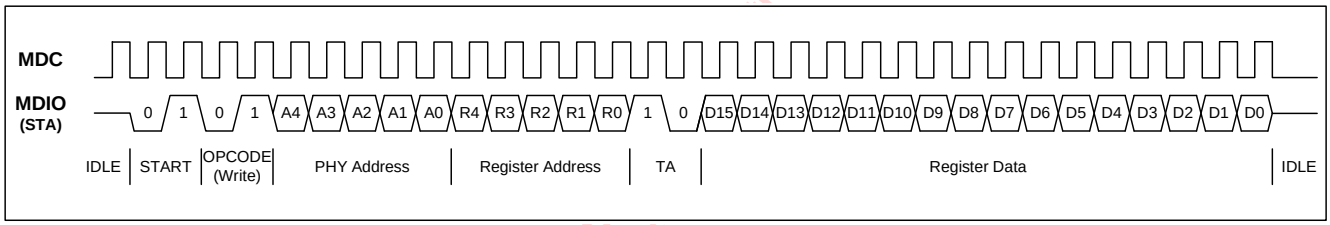


Table 64 is an example of a read operation.

Table 64: Serial Management Interface Protocol

32-Bit Preamble	Start of Frame	OpCode Read = 10 Write = 01	5-Bit PHY Device Address	5-Bit PHY Register Address (MSB)	2-Bit Turn around Read = z0 Write = 10	16-Bit Data Field	Idle
11111111	01	10	00000	00000	z0	0001001100000000	11111111

2.31.2.1 Preamble Suppression

The device is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.32 Jumbo Packet Support

The device supports jumbo packets up to 16Kbytes on all data paths.

2.33 Temperature Sensor

The device features an internal temperature sensor. The sensor reports the die temperature and is updated approximately once per second. The temperature is obtained by reading the value in Register 26_6:4:0 and performing conversion functions as described in Table 65.

An interrupt can be generated when the temperature exceeds a certain threshold.

Register 26_6.6 is set high whenever the temperature is greater than or equal to the value programmed in register 26_6.12:8. Register 26_6.6 remains high until read.

Register 26_6.7 controls whether the interrupt pin is asserted when register 26_6.6 is high.

Table 65: Temperature Sensor

Register	Function	Setting	Mode	HW Rst	SW Rst
26_6.12:8	Temperature Threshold	Temperature in C = 5 x 26_6.4:0 - 25 i.e., for 100C the value is 11001	R/W	11001	Retain
26_6.7	Temperature Sensor Interrupt Enable	1= Interrupt Enable 0 = Interrupt Enable	R/W	0	Retain
26_6.6	Temperature Sensor Interrupt	1 = Temperature Reached Threshold 0 = Temperature Below Threshold	RO, LH	0	0

Table 65: Temperature Sensor

Register	Function	Setting	Mode	HW Rst	SW Rst
26_6.4:0	Temperature Sensor	Temperature in C = 5 x 26_6.4:0 - 25 i.e., for 100C the value is 11001	RO	xxxxx	xxxxx

2.34 Regulators and Power Supplies

The 88E1510/88E1518/88E1512/88E1514 devices have built-in switch-cap regulators to support single rail operation from a 3.3V source. These internal regulators generate 1.8V and 1.0V. The integrated regulators greatly reduce the PCB BOM cost. If regulators are not used then an external 1.8V and 1.0V supply are needed. Table 66 and Table 67 lists the valid combinations of regulator usage.

The VDDO supply can run at 2.5V or 3.3V for the 88E1510 and 1.8V for 88E1518. 88E1512/88E1514 VDDO can operate at 1.8V/2.5V/3.3V supplies depending on the VDDO_SEL pin selection.

Note

- If VDDO is tied to either 1.8V or 2.5V, then the I/Os are not 3.3V tolerant.
- AVDDC18 is tied to 1.8V, so the XTAL_IN pin is not 2.5V/3.3V tolerant.

Table 66: Power Supply Options - Integrated Switching Regulator (REG_IN)

Functional Description	AVDD33	AVDDC18/ AVDD18	DVDD	Setup
Supply Source	3.3V	1.8V from Internal Regulator	1.0V from Internal Regulator	Single 3.3V external supply Internal regulator enabled

Table 67: Power Supply Options - External Supplies

Functional Description	AVDD33	AVDDC18/ AVDD18	DVDD	Setup
Supply Source	3.3V	1.8V External	1.0V from External	3.3V, 1.8V, 1.0V external supplies Internal regulator disabled.

Note

When internal regulator option is preferred, both 1.0V and 1.8V regulators must be used. Supplying 1.0V internally and 1.8V externally (or vice versa) is not supported.

2.34.1 AVDD18

AVDD18 is used as the 1.8V analog supply. AVDD18 can be supplied externally with 1.8V, or via the 1.8V regulator.

2.34.2 AVDDC18

AVDDC18 is used as a 1.8V analog supply for XTAL_IN/OUT pins. AVDDC18 can be supplied externally with 1.8V, or via the 1.8V regulator.

2.34.3 AVDD33

AVDD33 is used as a 3.3V analog supply.

2.34.4 DVDD

DVDD is used as the 1.0V digital supply. DVDD can be supplied externally with 1.0V, or via the internal switching 1.0V regulator.

2.34.5 REG_IN

REG_IN is used as the 3.3V supply to the internal regulator that generates the 1.8V for AVDD18 and AVDDC18 and 1.0V for DVDD. If the 1.8V or 1.0V regulators are not used, REG_IN must be left floating in addition to leaving REGCAP1 and REGCAP2 floating.

2.34.6 AVDD18_OUT

AVDD18_OUT is the internal regulator 1.8V output. This must be connected to 1.8V power plane that connects to AVDD18 and AVDDC18. If an external supply is used to supply AVDD18 and AVDDC18, AVDD18_OUT must be left floating.

2.34.7 DVDD_OUT

DVDD_OUT is the internal regulator 1.0V output. When internal regulator is used, DVDD_OUT must be connected to the DVDD plane. If an external supply is used to supply DVDD, DVDD_OUT must be left floating.

2.34.8 VDDO

VDDO supplies all digital I/O pins which use LVCMOS I/O standards. The supported voltages are 2.5V or 3.3V for 88E1510. 88E1518 supports only 1.8V. 88E1512/88E1514 supports 2.5V/3.3V if VDDO_SEL is tied to VSS and 1.8V if VDDO_SEL is tied to VDDO which is 1.8V. For VDDO 1.8V operation, the power can be supplied by the internal regulator.

2.34.9 Power Supply Sequencing

On power-up, no special power supply sequencing is required.

2.35 Wake on Lan (WOL) Event Detection

The device supports the detection and reporting of Wake On LAN (WOL) events. There are 3 types of events:

- Wake Up Frame Event
- Magic Packet Event
- Link Change Event

WOL related registers are grouped in 16_17 to 29_17. See Registers 16_17 to 29_17 for further details.

Register 19_0.7 indicates whether any of the events have been detected or not. If 19_0.7 = 1, then at least one of the 3 types of events have been detected. Setting 18_0.7 to 1 will enable an interrupt to be generated which can be sent out the LED[2] pin. See LED 19_0.7 for further details.

2.35.1 Wake Up Frame Event

There is an on-chip SRAM that can store up to eight 128-byte frame patterns to be matched to. Each pattern can be individually enabled, including it in the matching. The matching itself is enabled by setting 16_17.15 to 1 and 16_17.7:0 are used to enable which patterns are used in the matching. If any of the frame patterns enabled for matching are present in frames received by the PHY, then a Wake Up Frame Event has happened and 17_17.15 will assert to 1. Which patterns were detected in the frames received is shown by 17_17.7:0. These status bits may be cleared by setting 16_17.12 to 1.

The length of each frame pattern is programmable using 18_17 to 21_17. The maximum length of each pattern is 128 bytes. A received frame cannot be considered matching to a frame pattern if that received frame has a shorter length than what is specified by 18_17 to 21_17 even if all of the bytes in the received frame match the frame pattern up to the received frame's length. A received frame is considered matching to a frame pattern if that received frame has an equal or longer length than what is specified in addition to all bytes match up.

Each byte in the frame pattern has an associated compare bit, written to the SRAM in 27_17.8. When that compare bit is 1, the associated byte (written to the SRAM in 27_17.7:0) is compared to the corresponding byte in a received packet, otherwise when the compare bit is 0, it is not compared. As long as all bytes in a received frame that are enabled for comparison to the corresponding frame pattern bytes from Start of Frame (SOF) to the pattern length match, a Wake Up Frame Event will be indicated. Note that each compare bit and byte to be written to the SRAM must be programmed in 27_17 first then 26_17.10 must be set 1 in order for this data to actually be written into the SRAM.

The SRAM can be read on a per byte basis by programming the address in 26_17 and reading the data retrieved in 28_17.8:0 after 26_17.11 is set to 1. The data structure in the SRAM is shown in Table 68. For further details, refer to the 88E1310 WOL application notes.

Table 68: SRAM Data Structure

Bits	71:64	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
Row add 0x00	64 = Enable pat 0 B0 65 = Enable pat 1 B0 . . 71 = Enable pat 7 B0	pat 7 byte 0	pat 6 byte 0	pat 5 byte 0	pat 4 byte 0	pat 3 byte 0	pat 2 byte 0	pat 1 byte 0	pat 0 byte 0
Row add 0x01	64 = Enable pat 0 B1 65 = Enable pat 1 B1 . . 71 = Enable pat 7 B1	pat 7 byte 1	pat 6 byte 1	pat 5 byte 1	pat 4 byte 1	pat 3 byte 1	pat 2 byte 1	pat 1 byte 1	pat 0 byte 1

Table 68: SRAM Data Structure (Continued)

Bits	71:64	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
...	...		..	..	..	..	..	..	..
Row add 0x7f	64 = Enable pat 0 B127 65 = Enable pat 1 B127 . . 71 = Enable pat 7 B127	pat 7 byte 127	pat 6 byte 127	pat 5 byte 127	pat 4 byte 127	pat 3 byte 127	pat 2 byte 127	pat 1 byte 127	pat 0 byte 127

Note that when writing or reading the SRAM using register accesses, the SRAM packet matching logic must be disabled by setting 16_17.15 = 0 otherwise internal memory accesses done for this may conflict with register memory accesses.

2.35.2 Magic Packet Event

If any of the frames received by the device contain 6 bytes of FF followed by 16 iterations of the destination address programmed in Register 23_17, 24_17 and 25_17, then such a frame is considered to be a Magic Packet and a Magic Packet Event has happened. Magic Packet detection can be enabled/disabled by 16_17.14. 17_17.14 will be set to 1 when a Magic Packet Event has happened and can be cleared by setting 16_17.12 to 1.

2.35.3 Link Change Event

If the link status changes from link down to up, then a Link Change Event has happened. This detection can be enabled/disabled by 16_17.13. 17_17.13 will be set to 1 when a Link Change Event has happened and can be cleared by setting 16_17.12 to 1.

3 88E1510/88E1518/88E1512/88E1514 Register Description

Table 69 below defines the register types used in the register map.

Table 69: Register Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
RES	Reserved. All reserved bits are read as zero unless otherwise noted.
Retain	The register value is retained after software reset is executed.
RO	Read only.
ROC	Read only clear. After read, register field is cleared.
RW	Read and Write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field doesn't take effect until soft reset is executed.
WO	Write only. Reads from this type of register field return undefined data.
NR	Non-Rollover Register

3.1 PHY MDIO Register Description

The device supports both Clause 22 MDIO register access protocol and Clause 45 XMDIO register access protocol. The device also supports Clause 22 MDIO access to registers in Clause 45 XMDIO register space using Page 0 registers 13 and 14.

Table 70: Register Map

Register Name	Register Address	Table and Page
Copper Control Register	Page 0, Register 0	Table 71, p. 113
Copper Status Register	Page 0, Register 1	Table 72, p. 115
PHY Identifier 1	Page 0, Register 2	Table 73, p. 117
PHY Identifier 2	Page 0, Register 3	Table 74, p. 117
Copper Auto-Negotiation Advertisement Register	Page 0, Register 4	Table 75, p. 118
Copper Link Partner Ability Register - Base Page	Page 0, Register 5	Table 76, p. 120
Copper Auto-Negotiation Expansion Register	Page 0, Register 6	Table 77, p. 122
Copper Next Page Transmit Register	Page 0, Register 7	Table 78, p. 122
Copper Link Partner Next Page Register	Page 0, Register 8	Table 79, p. 123
1000BASE-T Control Register	Page 0, Register 9	Table 80, p. 123
1000BASE-T Status Register	Page 0, Register 10	Table 81, p. 125
XMDIO MMD control Register	Page 0, Register 13	Table 82, p. 126
XMDIO MMD address data Register	Page 0, Register 14	Table 83, p. 126
Extended Status Register	Page 0, Register 15	Table 84, p. 126
Copper Specific Control Register 1	Page 0, Register 16	Table 85, p. 127
Copper Specific Status Register 1	Page 0, Register 17	Table 86, p. 128
Copper Specific Interrupt Enable Register	Page 0, Register 18	Table 87, p. 130
Copper Interrupt Status Register	Page 0, Register 19	Table 88, p. 131
Copper Specific Control Register 2	Page 0, Register 20	Table 89, p. 133
Copper Specific Receive Error Counter Register	Page 0, Register 21	Table 90, p. 133
Page Address	Page Any, Register 22	Table 91, p. 134
Global Interrupt Status	Page 0, Register 23	Table 92, p. 134
Copper Specific Control Register 3	Page 0, Register 26	Table 93, p. 134
Fiber Control Register	Page 1, Register 0	Table 94, p. 135
Fiber Status Register	Page 1, Register 1	Table 95, p. 137
PHY Identifier	Page 1, Register 2	Table 96, p. 139
PHY Identifier	Page 1, Register 3	Table 97, p. 139
Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)	Page 1, Register 4	Table 98, p. 139
Fiber Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_1.1:0 = 10)	Page 1, Register 4	Table 99, p. 141
Fiber Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_1.1:0 = 11)	Page 1, Register 4	Table 100, p. 142
Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)	Page 1, Register 5	Table 101, p. 142
Fiber Link Partner Ability Register - SGMII (System mode) (Register 16_1.1:0 = 10)	Page 1, Register 5	Table 102, p. 143

Table 70: Register Map

Register Name	Register Address	Table and Page
Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11)	Page 1, Register 5	Table 103, p. 143
Fiber Auto-Negotiation Expansion Register	Page 1, Register 6	Table 104, p. 144
Fiber Next Page Transmit Register	Page 1, Register 7	Table 105, p. 145
Fiber Link Partner Next Page Register	Page 1, Register 8	Table 106, p. 146
Extended Status Register	Page 1, Register 15	Table 84, p. 126
Fiber Specific Control Register 1	Page 1, Register 16	Table 108, p. 147
Fiber Specific Status Register	Page 1, Register 17	Table 109, p. 148
Fiber Interrupt Enable Register	Page 1, Register 18	Table 110, p. 149
Fiber Interrupt Status Register	Page 1, Register 19	Table 111, p. 150
Fiber Receive Error Counter Register	Page 1, Register 21	Table 112, p. 151
PRBS Control	Page 1, Register 23	Table 113, p. 151
PRBS Error Counter LSB	Page 1, Register 24	Table 114, p. 152
PRBS Error Counter MSB	Page 1, Register 25	Table 115, p. 152
Fiber Specific Control Register 2	Page 1, Register 26	Table 116, p. 152
MAC Specific Control Register 1	Page 2, Register 16	Table 117, p. 153
MAC Specific Interrupt Enable Register	Page 2, Register 18	Table 118, p. 155
MAC Specific Status Register	Page 2, Register 19	Table 119, p. 155
Copper RX_ER Byte Capture	Page 2, Register 20	Table 120, p. 156
MAC Specific Control Register 2	Page 2, Register 21	Table 121, p. 156
RGMII Output Impedance Calibration Override	Page 2, Register 24	Table 122, p. 157
RGMII Output Impedance Target	Page 2, Register 25	Table 123, p. 158
LED[2:0] Function Control Register	Page 3, Register 16	Table 124, p. 159
LED[2:0] Polarity Control Register	Page 3, Register 17	Table 125, p. 160
LED Timer Control Register	Page 3, Register 18	Table 126, p. 161
PTP LED Function Control	Page 3, Register 19	Table 127, p. 162
RGMII RX_ER Byte Capture	Page 4, Register 20	Table 128, p. 162
Advanced VCT TX to MDI[0] Rx Coupling	Page 5, Register 16	Table 129, p. 163
Advanced VCT TX to MDI[1] Rx Coupling	Page 5, Register 17	Table 130, p. 163
Advanced VCT TX to MDI[2] Rx Coupling	Page 5, Register 18	Table 131, p. 165
Advanced VCT TX to MDI[3] Rx Coupling	Page 5, Register 19	Table 132, p. 166
1000BASE-T Pair Skew Register	Page 5, Register 20	Table 133, p. 166
1000BASE-T Pair Swap and Polarity	Page 5, Register 21	Table 134, p. 167
Advance VCT Control	Page 5, Register 23	Table 135, p. 167
Advanced VCT Sample Point Distance	Page 5, Register 24	Table 136, p. 168
Advanced VCT Cross Pair Positive Threshold	Page 5, Register 25	Table 137, p. 169

Table 70: Register Map

Register Name	Register Address	Table and Page
Advanced VCT Same Pair Impedance Positive Threshold 0 and 1	Page 5, Register 26	Table 138, p. 169
Advanced VCT Same Pair Impedance Positive Threshold 2 and 3	Page 5, Register 27	Table 139, p. 169
Advanced VCT Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control	Page 5, Register 28	Table 140, p. 170
Copper Port Packet Generation	Page 6, Register 16	Table 141, p. 171
Copper Port CRC Counters	Page 6, Register 17	Table 142, p. 172
Checker Control	Page 6, Register 18	Table 143, p. 172
Copper Port Packet Generation	Page 6, Register 19	Table 144, p. 172
General Control Register	Page 6, Register 20	Table 145, p. 172
Late Collision Counters 1 & 2	Page 6, Register 23	Table 146, p. 173
Late Collision Counters 3 & 4	Page 6, Register 24	Table 147, p. 173
Late Collision Window Adjust/Link Disconnect	Page 6, Register 25	Table 148, p. 174
Misc Test	Page 6, Register 26	Table 149, p. 174
Misc Test: Temperature Sensor Alternative Reading	Page 6, Register 27	Table 150, p. 175
PHY Cable Diagnostics Pair 0 Length	Page 7, Register 16	Table 151, p. 175
PHY Cable Diagnostics Pair 1 Length	Page 7, Register 17	Table 152, p. 176
PHY Cable Diagnostics Pair 2 Length	Page 7, Register 18	Table 153, p. 176
PHY Cable Diagnostics Pair 3 Length	Page 7, Register 19	Table 154, p. 176
PHY Cable Diagnostics Results	Page 7, Register 20	Table 155, p. 176
PHY Cable Diagnostics Control	Page 7, Register 21	Table 156, p. 177
Advanced VCT Cross Pair Negative Threshold	Page 7, Register 25	Table 157, p. 178
Advanced VCT Same Pair Impedance Negative Threshold 0 and 1	Page 7, Register 26	Table 158, p. 178
Advanced VCT Same Pair Impedance Negative Threshold 2 and 3	Page 7, Register 27	Table 159, p. 178
Advanced VCT Same Pair Impedance Negative Threshold 4	Page 7, Register 28	Table 160, p. 179
PTP Port Configuration Register 0	Page 8, Register 0	Table 161, p. 179
PTP Port Configuration Register 1	Page 8, Register 1	Table 162, p. 180
PTP Port Configuration Register 2	Page 8, Register 2	Table 163, p. 181
PTP Port Configuration Register 3	Page 8, Register 3	Table 164, p. 183
PTP Arrival 0 Time Port Status Register	Page 8, Register 8	Table 165, p. 184
PTP Arrival 0 Time Register Bytes 1 & 0	Page 8, Register 9	Table 166, p. 185
PTP Arrival 0 Time Register Bytes 3 & 2	Page 8, Register 10	Table 167, p. 186
PTP Arrival 0 Sequence Identifier Register	Page 8, Register 11	Table 168, p. 187
PTP Arrival 1 Time Port Status Register	Page 8, Register 12	Table 169, p. 187
PTP Arrival 1 Time Register Bytes 1 & 0	Page 8, Register 13	Table 170, p. 188

Table 70: Register Map

Register Name	Register Address	Table and Page
PTP Arrival 1 Time Register Bytes 3 & 2	Page 8, Register 14	Table 171, p. 189
PTP Arrival 1 Sequence Identifier Register	Page 8, Register 15	Table 172, p. 190
PTP Departure Time Port Status Register	Page 9, Register 0	Table 173, p. 190
PTP Departure Time Register Bytes 1 & 0	Page 9, Register 1	Table 174, p. 191
PTP Departure Time Register Bytes 3 & 2	Page 9, Register 2	Table 175, p. 192
PTP Departure Sequence Identifier Status Register	Page 9, Register 3	Table 176, p. 193
PTP Port Discard Counter Register	Page 9, Register 5	Table 177, p. 193
TAI Global Configuration Register 0	Page 12, Register 0	Table 178, p. 195
TAI Global Configuration Register 1	Page 12, Register 1	Table 179, p. 198
TAI Global Configuration Register 2	Page 12, Register 2	Table 180, p. 198
TAI Global Configuration Register 3	Page 12, Register 3	Table 181, p. 199
TAI Global Configuration Register 4	Page 12, Register 4	Table 182, p. 199
TAI Global Configuration Register 5	Page 12, Register 5	Table 183, p. 200
TAI Global Configuration Register 6	Page 12, Register 6	Table 184, p. 201
TAI Global Configuration Register 7	Page 12, Register 7	Table 185, p. 201
TAI Global Configuration Register 8	Page 12, Register 8	Table 186, p. 202
TAI Global Configuration Register 9	Page 12, Register 9	Table 187, p. 202
Event Capture Register Byte 1 & 0	Page 12, Register 10	Table 188, p. 203
Event Capture Register Byte 3 & 2	Page 12, Register 11	Table 189, p. 205
TAI Global Configuration Register 12	Page 12, Register 12	Table 190, p. 206
TAI Global Configuration Register 13	Page 12, Register 13	Table 191, p. 206
PTP Global Time Register Bytes 1 & 0	Page 12, Register 14	Table 192, p. 207
PTP Global Time Register Bytes 3 & 2	Page 12, Register 15	Table 193, p. 209
PTP Global Configuration Register 0	Page 14, Register 0	Table 194, p. 210
PTP Global Configuration Register 1	Page 14, Register 1	Table 195, p. 211
PTP Global Configuration Register 2	Page 14, Register 2	Table 196, p. 212
PTP Global Configuration Register 3	Page 14, Register 3	Table 197, p. 212
PTP Global Status Register	Page 14, Register 8	Table 198, p. 213
ReadPlus Command Register	Page 14, Register 14	Table 199, p. 213
ReadPlus Data Register	Page 14, Register 15	Table 200, p. 214
WOL Control	Page 17, Register 16	Table 201, p. 214
WOL Status	Page 17, Register 17	Table 202, p. 215
SRAM Packets 7/6 Length	Page 17, Register 18	Table 203, p. 216
SRAM Packets 5/4 Length	Page 17, Register 19	Table 204, p. 217
SRAM Packets 3/2 Length	Page 17, Register 20	Table 205, p. 217
SRAM Packets 1/0 Length	Page 17, Register 21	Table 206, p. 217
Magic Packet Destination Address Word 2	Page 17, Register 23	Table 207, p. 218

Table 70: Register Map

Register Name	Register Address	Table and Page
Magic Packet Destination Address Word 1	Page 17, Register 24	Table 208, p. 218
Magic Packet Destination Address Word 0	Page 17, Register 25	Table 209, p. 218
SRAM Byte Address Control	Page 17, Register 26	Table 210, p. 219
SRAM Byte Data Control	Page 17, Register 27	Table 211, p. 220
SRAM Read Control	Page 17, Register 28	Table 212, p. 220
EEE Buffer Control Register 1	Page 18, Register 0	Table 213, p. 220
EEE Buffer Control Register 2	Page 18, Register 1	Table 214, p. 221
EEE Buffer Control Register 3	Page 18, Register 2	Table 215, p. 221
Packet Generation	Page 18, Register 16	Table 216, p. 221
CRC Counters	Page 18, Register 17	Table 217, p. 222
Checker Control	Page 18, Register 18	Table 218, p. 223
Packet Generation	Page 18, Register 19	Table 219, p. 223
General Control Register 1	Page 18, Register 20	Table 220, p. 224
Link Disconnect count	Page 18, Register 25	Table 221, p. 225
SERDES RX_ER Byte Capture	Page 18, Register 26	Table 222, p. 225

Table 71: Copper Control Register
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Reset	R/W, SC	0x0	SC	Copper Software Reset. Affects pages 0, 2, 3, 5, and 7. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the data from the MAC presented to the PHY is looped back inside the PHY and then sent back to the MAC. Link is broken when loopback is enabled. Loopback speed is determined by Registers 21_2.6,13. 1 = Enable Loopback 0 = Disable Loopback

Table 71: Copper Control Register
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Speed Select (LSB)	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
12	Auto-Negotiation Enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 is set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	0x0	Retain	Power down is controlled via register 0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_15) and Restart Auto-Negotiation (0.9) are not set by the user. IEEE power down shuts down the chip except for the RGMII interface if 16_2.3 is set to 1. If 16_2.3 is set to 0, then the RGMII interface also shuts down. 1 = Power down 0 = Normal operation
10	Isolate	R/W	0x0	0x0	1 = Isolate 0 = Normal Operation

Table 71: Copper Control Register
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
9	Restart Copper Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Copper Duplex Mode	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation 1 = Full-duplex 0 = Half-Duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
5:0	Reserved	RO	Always 000000	Always 000000	Will always be 0.

Table 72: Copper Status Register
Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	Always 1	Always 1	1 = PHY able to perform full-duplex 100BASE-X

Table 72: Copper Status Register
Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
13	100BASE-X Half-Duplex	RO	Always 1	Always 1	1 = PHY able to perform half-duplex 100BASE-X
12	10 Mbps Full-Duplex	RO	Always 1	Always 1	1 = PHY able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	Always 1	Always 1	1 = PHY able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Must always be 0.
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed
5	Copper Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Copper Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected
3	Auto-Negotiation Ability	RO	Always 1	Always 1	1 = PHY able to perform Auto-Negotiation
2	Copper Link Status	RO,LL	0x0	0x0	This register bit indicates that link was down since the last read. For the current link status, either read this register back-to-back or read Register 17_0.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Jabber Detect	RO,LH	0x0	0x0	1 = Jabber condition detected 0 = Jabber condition not detected
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 73: PHY Identifier 1
Page 0, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

Table 74: PHY Identifier 2
Page 0, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI Lsb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit24
9:4	Model Number	RO	Always 011101	Always 011101	Model Number 011101
3:0	Revision Number	RO	See Descr	See Descr	Rev Number. Contact Marvell® FAEs for information on the device revision number.

Table 75: Copper Auto-Negotiation Advertisement Register
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
14	Ack	RO	Always 0	Always 0	Must be 0.
13	Remote Fault	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Reserved	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down Reserved bit is R/W to allow for forward compatibility with future IEEE standards.
11	Asymmetric Pause	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Asymmetric Pause 0 = No asymmetric Pause

Table 75: Copper Auto-Negotiation Advertisement Register
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Pause	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	R/W	0x0	Retain	0 = Not capable of 100BASE-T4
8	100BASE-TX Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised
7	100BASE-TX Half-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised

Table 75: Copper Auto-Negotiation Advertisement Register
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
6	10BASE-TX Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised
5	10BASE-TX Half-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised
4:0	Selector Field	R/W	0x01	Retain	Selector Field mode 00001 = 802.3

Table 76: Copper Link Partner Ability Register - Base Page
Page 0, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page

Table 76: Copper Link Partner Ability Register - Base Page
Page 0, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Acknowledge	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
13	Remote Fault	RO	0x0	0x0	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
12	Technology Ability Field	RO	0x0	0x0	Received Code Word Bit 12
11	Asymmetric Pause	RO	0x0	0x0	Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	Pause Capable	RO	0x0	0x0	Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
9	100BASE-T4 Capability	RO	0x0	0x0	Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
8	100BASE-TX Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
7	100BASE-TX Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
6	10BASE-T Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
5	10BASE-T Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
4:0	Selector Field	RO	0x00	0x00	Selector Field Received Code Word Bit 4:0

Table 77: Copper Auto-Negotiation Expansion Register
Page 0, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	0x000	Reserved. Must be 00000000000.
4	Parallel Detection Fault	RO,LH	0x0	0x0	Register 6_0.4 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function
3	Link Partner Next page Able	RO	0x0	0x0	Register 6_0.3 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	0x1	0x1	Register 6_0.2 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Local Device is Next Page able 0 = Local Device is not Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_0.1 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	Register 6_0.0 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 78: Copper Next Page Transmit Register
Page 0, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_0 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Link fail will clear Reg 7_0. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14

Table 78: Copper Next Page Transmit Register
Page 0, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 79: Copper Link Partner Next Page Register
Page 0, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 80: 1000BASE-T Control Register
Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode	R/W	0x0	Retain	TX_CLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (Register 0_0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved

Table 80: 1000BASE-T Control Register
Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
12	MASTER/SLAVE Manual Configuration Enable	R/W	0x0	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
11	MASTER/SLAVE Configuration Value	R/W	0x0	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE
10	Port Type	R/W	0x0	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Register 9_0.10 is ignored if Register 9_0.12 is equal to 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Advertise 0 = Not advertised

Table 80: 1000BASE-T Control Register
Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Reserved	R/W	0x00	Retain	0

Table 81: 1000BASE-T Status Register
Page 0, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER/SLAVE Configuration Fault	RO,LH	0x0	0x0	This register bit will clear on read. 1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected
14	MASTER/SLAVE Configuration Resolution	RO	0x0	0x0	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE
13	Local Receiver Status	RO	0x0	0x0	1 = Local Receiver OK 0 = Local Receiver is Not OK
12	Remote Receiver Status	RO	0x0	0x0	1 = Remote Receiver OK 0 = Remote Receiver Not OK
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T full-duplex 0 = Link Partner is not capable of 1000BASE-T full-duplex
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T half-duplex 0 = Link Partner is not capable of 1000BASE-T half-duplex
9:8	Reserved	RO	0x0	0x0	Reserved
7:0	Idle Error Count	RO, SC	0x00	0x00	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Table 82: XMDIO MMD control Register
Page 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0x0	0x0	15.14 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	0x000	0x000	Reserved
4:0	DEVAD	R/W	0x00	0x00	Device address

Table 83: XMDIO MMD address data Register
Page 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0x0000	0x0000	If 13.15:14 = 00, this register is the MMD DEVAD's address register. Otherwise, it is the MMD DEVAD's data register as indicated by the contents of its address register

Table 84: Extended Status Register
Page 0, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	Always 0	Always 0	0 = Not 1000BASE-X full-duplex capable
14	1000BASE-X Half-Duplex	RO	Always 0	Always 0	0 = Not 1000BASE-X half-duplex capable
13	1000BASE-T Full-Duplex	RO	Always 1	Always 1	1 = 1000BASE-T full-duplex capable
12	1000BASE-T Half-Duplex	RO	Always 1	Always 1	1 = 1000BASE-T half-duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000

Table 85: Copper Specific Control Register 1
Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable Link Pulses	R/W	0x0	0x0	1 = Disable Link Pulse 0 = Enable Link Pulse
14:12	Downshift counter	R/W	0x3	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1x, 2x,...8x is the number of times the PHY attempts to establish Gigabit link before the PHY downshifts to the next highest speed. 000 = 1x 100 = 5x 001 = 2x 101 = 6x 010 = 3x 110 = 7x 011 = 4x 111 = 8x
11	Downshift Enable	R/W	0x0	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Enable downshift. 0 = Disable downshift.
10	Force Copper Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. In 1000BASE-T mode this has no effect. 1 = Force link good 0 = Normal operation
9:8	Energy Detect	R/W	0x0	Update	0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP (Energy Detect+TM)
7	Reserved				Reserved.
6:5	MDI Crossover Mode	R/W	0x3	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Reserved	R/W	0x0	Retain	Set to 0
3	Copper Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable

Table 85: Copper Specific Control Register 1
Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Power Down	R/W	0x0	Retain	Power down is controlled via register 0_0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_0.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. 1 = Power down 0 = Normal operation
1	Polarity Reversal Disable	R/W	0x0	Retain	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled The detected polarity status is shown in Register 17_0.1, or in 1000BASE-T mode, 21_5.3:0.
0	Disable Jabber	R/W	0x0	Retain	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

Table 86: Copper Specific Status Register 1
Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x2	Retain	These status bits are valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled 17_0.11 = 1. 1 = Resolved 0 = Not resolved
10	Copper Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down

Table 86: Copper Specific Status Register 1
Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
9	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
8	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
7	Reserved	RO	0x0	0x0	0
6	MDI Crossover Status	RO	0x1	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
5	Downshift Status	RO	0x0	0x0	1 = Downshift 0 = No Downshift
4	Copper Energy Detect Status	RO	0x0	0x0	1 = Sleep 0 = Active
3	Global Link Status	RO	0x0	0x0	1 = Copper link is up 0 = Copper link is down
2	DTE power status	RO	0x0	0x0	1 = Link partner needs DTE power 0 = Link partner does not need DTE power
1	Polarity (real time)	RO	0x0	0x0	1 = Reversed 0 = Normal Polarity reversal can be disabled by writing to Register 16_0.1. In 1000BASE-T mode, polarity of all pairs are shown in Register 21_5.3:0.
0	Jabber (real time)	RO	0x0	0x0	1 = Jabber 0 = No jabber

Table 87: Copper Specific Interrupt Enable Register
Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Auto-Negotiation Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	WOL Event Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6	MDI Crossover Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
5	Downshift Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
4	Copper Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3	FLP Exchange Complete but no Link Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	DTE power detection status changed interrupt enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 87: Copper Specific Interrupt Enable Register
Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 88: Copper Interrupt Status Register
Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Auto-Negotiation Error	RO,LH	0x0	0x0	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
14	Copper Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Copper Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Copper Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Copper Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Copper Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Copper Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	Copper False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	WOL Event Happened	RO, LH	0x0	0x0	1 = WOL event happened 0 = WOL event did not happen
6	MDI Crossover Changed	RO,LH	0x0	0x0	1 = Crossover changed 0 = Crossover not changed
5	Downshift Interrupt	RO,LH	0x0	0x0	1 = Downshift detected 0 = No down shift
4	Copper Energy Detect Changed	RO,LH	0x0	0x0	1 = Energy Detect state changed 0 = No Energy Detect state change detected

Table 88: Copper Interrupt Status Register
Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
3	FLP Exchange Complete but no Link	RO,LH	0x0	0x0	1 = FLP Exchange Completed but Link Not Established 0 = No Event Detected
2	DTE power detection status changed interrupt	RO,LH	0x0	0x0	1 = DTE power detection status changed 0 = No DTE power detection status change detected
1	Polarity Changed	RO,LH	0x0	0x0	1 = Polarity Changed 0 = Polarity not changed
0	Jabber	RO,LH	0x0	0x0	1 = Jabber 0 = No jabber

Table 89: Copper Specific Control Register 2
Page 0, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x000	Retain	Write all 0s.
7	10BASE-Te Enable			Retain	1= 10BASE-Te EEE Enable 0 = 10BASE-TE EEE Disable
6	Break Link On Insufficient IPG	R/W	0x0	Retain	0 = Break link on insufficient IPGs in 10BASE-T and 100BASE-TX 1 = Do not break link on insufficient IPGs in 10BASE-T and 100BASE-TX
5	100 BASE-T Transmitter Clock Source	R/W	0x1	Update	1 = Local Clock 0 = Recovered Clock
4	Accelerate 100BASE-T Link Up	R/W	0x0	Retain	0 = No Acceleration 1 = Accelerate
3	Reverse MDIP/ N[3] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity
2	Reverse MDIP/ N[2] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity
1	Reverse MDIP/ N[1] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity
0	Reverse MDIP/ N[0] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity

Table 90: Copper Specific Receive Error Counter Register
Page 0, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

Table 91: Page Address
Page Any, Register 22

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	All 0's
7:0	Page select for registers 0 to 28	R/W	0x00	Retain	Page Number

Table 92: Global Interrupt Status
Page 0, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x0000	0x0000	Reserved.
0	Interrupt	RO	0x0	0x0	1 = Interrupt active on port X 0 = No interrupt active on port X

Table 93: Copper Specific Control Register 3
Page 0, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Reserved.
14	Disable 1000BASE-T	R/W	0x0	Retain	When set to disabled, 1000BASE-T will not be advertised even if registers 9.9 or 9.8 are set to 1. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Disable 1000BASE-T Advertisement 0 = Enable 1000BASE-T Advertisement
13	Reverse Auto-Neg	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Reverse Auto-Negotiation 0 = Normal Auto-Negotiation

Table 93: Copper Specific Control Register 3
Page 0, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Reserved	R/W	0x0	Retain	Reserved
11:10	Gigabit Link Down Delay	R/W	0x0	Retain	This register only have effect if register 26_0.9 is set to 1. 00 = 0ms 01 = 10 ± 2 ms 10 = 20 ± 2 ms 11 = 40 ± 2 ms
9	Speed Up Gigabit Link Down Time	R/W	0x0	Retain	1 = Enable faster gigabit link down 0 = Use IEEE gigabit link down
8	DTE detect enable	R/W	0x0	Update	1 = Enable DTE detection 0 = Disable DTE detection
7:4	DTE detect status drop hysteresis	R/W	0x4	Retain	0000: Report immediately 0001: Report 5s after DTE power status drop ... 1111: Report 75s after DTE power status drop
3:2	100 MB test select	R/W	0x0	Retain	0x = Normal Operation 10 = Select 112 ns sequence 11 = Select 16 ns sequence
1	10 BT polarity force	R/W	0x0	Retain	1 = Force negative polarity for Receive only 0 = Normal Operation
0	Reserved	R/W	0x0	Retain	Set to 0

Table 94: Fiber Control Register
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Fiber Reset	R/W	0x0	SC	Fiber Software Reset. Affects page 1. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation

Table 94: Fiber Control Register
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD of the internal bus is looped back to RXD of the internal bus. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in. 1000BASE-X - loopback is always in 1000Mbps. 100BASE-FX - loopback is always in 100Mbps. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	RO, R/W	0x0	Retain	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is always 1. If register 16_1.1:0 (MODE[1:0]) = 01 then this bit is always 0. If register 16_1.1:0 (MODE[1:0]) = 10 then this bit is 1 when the PHY is at 100Mb/s, else it is 0. If register 16_1.1:0 (MODE[1:0]) = 11 then this bit is R/W. bit 6,13 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
12	Auto-Negotiation Enable	R/W	See Descr	Retain	If the value of this bit is changed, the link will be broken and Auto-Negotiation Restarted This bit has no effect when in 100BASE-FX mode When this bit gets set/reset, Auto-negotiation is restarted (bit 0_1.9 is set to 1). On hardware reset this bit takes on the value of S_ANEG 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	0x0	0x0	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_1.15) and Restart Auto-Negotiation (0_1.9) are not set by the user. On hardware reset, bit 0_1.11 1 = Power down 0 = Normal operation
10	Isolate	RO	0x0	0x0	This function is not supported
9	Restart Fiber Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware, software reset (0_1.15) or change in Auto-Negotiation enable (0_1.12) regardless of whether or not the restart bit (0_1.9) is set. The bit is set when Auto-negotiation is Enabled or Disabled in 0_1.12 1 = Restart Auto-Negotiation Process 0 = Normal operation

Table 94: Fiber Control Register
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Duplex Mode	R/W	0x1	Retain	Writing this bit has no effect unless one of the following events occur: Software reset is asserted (Register 0_1.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Auto-Negotiation Enable changes (Register 0_1.12) Power down (Register 0_1.11) transitions from power down to normal operation 1 = Full-duplex 0 = Half-Duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	RO, R/W	0x1	Retain	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is always 0. If register 16_1.1:0 (MODE[1:0]) = 01 then this bit is always 1. If register 16_1.1:0 (MODE[1:0]) = 10 then this bit is 1 when the PHY is at 1000Mb/s, else it is 0. If register 16_1.1:0 (MODE[1:0]) = 11 then this bit is R/W. bit 6,13 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
5:0	Reserved	RO	Always 000000	Always 000000	Always 0.

Table 95: Fiber Status Register
Page 1, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 1, else this bit is 0. bit 6,13 1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 1, else this bit is 0. bit 6,13 1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X

Table 95: Fiber Status Register
Page 1, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
12	10 Mb/s Full Duplex	RO	Always 0	Always 0	0 = PHY not able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Must always be 0.
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed
5	Fiber Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-negotiation Bypass or if Auto-negotiation is disabled.
4	Fiber Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected This bit is always 0 in SGMII modes.
3	Auto-Negotiation Ability	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. bit 6,13 1 = PHY able to perform Auto-Negotiation 0 = PHY not able to perform Auto-Negotiation
2	Fiber Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_1.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Reserved	RO,LH	Always 0	Always 0	Must be 0
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 96: PHY Identifier
Page 1, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

Table 97: PHY Identifier
Page 1, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI Lsb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits 19:24 000011 ^.....^ bit 19...bit24
9:4	Model Number	RO	Always 011101	Always 011101	Model Number 011101
3:0	Revision Number	RO	Always 0000	0x0	Rev Number = 0000

Table 98: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_1.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised

Table 98: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01) (Continued)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Reserved	RO	Always 0	Always 0	Reserved
13:12	Remote Fault 2/ RemoteFault 1	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	Always 000	Always 000	Reserved
8:7	Pause	R/W	See Descr.	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Upon hardware reset both bits takes on the value of ENA_PAUSE. 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	R/W	See Descr.	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit takes on the value of C_ANEG[0]. 1 = Advertise 0 = Not advertised

Table 98: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01) (Continued)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
5	1000BASE-X Full-Duplex	R/W	0x1	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
4:0	Reserved	R/W	0x00	0x00	Reserved

Table 99: Fiber Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_1.1:0 = 10)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link Status	RO	0x0	0x0	0 = Link is Not up on the Copper Interface 1 = Link is up on the Copper Interface
14	Reserved	RO	Always 0	Always 0	Reserved
13	Reserved	RO	Always 0	Always 0	Reserved
12	Duplex Status	RO	0x0	0x0	0 = Interface Resolved to Half-duplex 1 = Interface Resolved to Full-duplex
11:10	Speed[1:0]	RO	0x0	0x0	00 = Interface speed is 10 Mbps 01 = Interface speed is 100 Mbps 10 = Interface speed is 1000 Mbps 11 = Reserved
9	Transmit Pause	RO	0x0	0x0	Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Disabled, 1 = Enabled
8	Receive Pause	RO	0x0	0x0	Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Disabled, 1 = Enabled
7	Fiber/Copper	RO	0x0	0x0	Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	Always 0000001	Always 0000001	Reserved

Table 100: Fiber Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_1.1:0 = 11)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RO	Always 0x0001	Always 0x0001	Reserved

Table 101: Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:12	Remote Fault 2/ Remote Fault 1	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:9
8:7	Asymmetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 6 1 = Link partner capable of 1000BASE-X half-duplex. 0 = Link partner not capable of 1000BASE-X half-duplex.

Table 101: Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
5	1000BASE-X Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 5 1 = Link partner capable of 1000BASE-X full-duplex. 0 = Link partner not capable of 1000BASE-X full-duplex.
4:0	Reserved	RO	0x00	0x00	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bits 4:0 Must be 0

Table 102: Fiber Link Partner Ability Register - SGMII (System mode) (Register 16_1.1:0 = 10)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Must be 0
14	Acknowledge	RO	0x0	0x0	Acknowledge Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:0	Reserved	RO	0x0000	0x0000	Received Code Word Bits 13:0 Must receive 00_0000_0000_0001 per SGMII spec

Table 103: Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word

Table 103: Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Reserved	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13 Must be 0
12	Duplex Status	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12 1 = Copper Interface on the link Partner is capable of Full Duplex 0 = Copper Interface on the link partner is capable of Half Duplex
11:10	Speed Status	RO	0x0	0x0	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = reserved
9	Transmit Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 9 0 = Disabled, 1 = Enabled
8	Receive Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 8 0 = Disabled, 1 = Enabled
7	Fiber/Copper Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 7 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	0x00	0x00	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bits 6:0 Must be 0000001

Table 104: Fiber Auto-Negotiation Expansion Register
Page 1, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	Reserved. Must be 00000000000.

Table 104: Fiber Auto-Negotiation Expansion Register
Page 1, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Link Partner Next page Able	RO	0x0	0x0	SGMII and 100BASE-FX modes this bit is always 0. In 1000BASE-X mode register 6_1.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	Always 1	Always 1	1 = Local Device is Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_1.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the fiber receiver has received 3 non-zero matching valid configuration code groups and Auto-negotiation is enabled in register 0_1.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 105: Fiber Next Page Transmit Register
Page 1, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_1 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Register 7_1 only has effect in the 1000BASE-X mode. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 106: Fiber Link Partner Next Page Register
Page 1, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register 8_1 only has effect in the 1000BASE-X mode. The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 107: Extended Status Register
Page 1, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. 1 = 1000BASE-X full duplex capable 0 = not 1000BASE-X full duplex capable
14	1000BASE-X Half-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. 1 = 1000BASE-X half duplex capable 0 = not 1000BASE-X half duplex capable
13	1000BASE-T Full-Duplex	RO	0x0	0x0	0 = not 1000BASE-T full duplex capable
12	1000BASE-T Half-Duplex	RO	0x0	0x0	0 = not 1000BASE-T half duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000

Table 108: Fiber Specific Control Register 1
Page 1, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Fiber Transmit FIFO Depth	R/W	0x1	Retain	00 = +/- 16 Bits 01 = +/- 24 Bits 10 = +/- 32 Bits 11 = +/- 40 Bits
13	Block Carrier Extension Bit	R/W	0x0	Retain	Carrier extension and carrier extension with error are converted to idle symbols on the RXD only during full duplex mode. 1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension
12	SERDES Loopback	R/W	0x0	0x0	Register 16_1.8 selects the line loopback path. 1 = Enable loopback from SERDES input to SERDES output 0 = Normal Operation
11	Assert CRS on Transmit	R/W	0x0	Retain	This bit has no effect in full-duplex. 1 = Assert on transmit 0 = Never assert on transmit
10	Force Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation
9	Reserved	R/W	0x0	Retain	Set to 0.
8	SERDES Loopback Type	R/W	0x0	Retain	0 = Loopback Through PCS (Tx and Rx can be asynchronous) 1 = Loopback raw 10 bit data (Tx and Rx must be synchronous)
7:6	Enhanced SGMII	R/W	0x0	Update	00 = Do not pass flow control bits through SGMII Auto-Negotiation. SGMII (System mode) registers 4_1.9:7 are always 000. EEE bits are passed per IEEE. 01 = Pass flow control bits through SGMII Auto-Negotiation using 4_1.9:7. EEE bits are passed in alternate locations. 10 = Pass flow control bits through SGMII Auto-Negotiation using bits other than 4_1.9:7. EEE bits use 9:8. 11 = Reserved
5	Marvell Remote Fault Indication Enable	R/W	0x0	Retain	0 = Disable 1 = Enable, Remote Fault is indicated to link partner in less than 2 ms, only one bit of bit 5:4 can be set to 1
4	IEEE Remote Fault Indication Enable	R/W	0x0	Retain	0 = Disable 1 = Enable, Remote Fault is indicated to link partner after 20ms according to IEEE standard, only one bit of bit 5:4 can be set to 1

Table 108: Fiber Specific Control Register 1
Page 1, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Reserved	R/W	0x1	Update	
2	Interrupt Polarity	R/W	0x1	Retain	1 = INTn active low 0 = INTn active high
1:0	MODE[1:0]	RO	See Desc.	See Desc.	These bits reflects the mode as programmed in register of 20_6.2:0 00 = 100BASE-FX 01 = 1000BASE-X 10 = SGMII System mode 11 = SGMII Media mode

Table 109: Fiber Specific Status Register
Page 1, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	Retain	These status bits are valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 01. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit follows register 0_1.8. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	In 100BASE-FX mode this bit is always 0. 1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled or in 100BASE-FX mode this bit is always 1. 1 = Resolved 0 = Not resolved If bit 26_1.5 is 1, then this bit will be 0.
10	Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9:8	Reserved	RO	Always 00	Always 00	

Table 109: Fiber Specific Status Register
Page 1, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
7:6	Remote Fault Received	RO, LH	0x0	0x0	The mapping for this status is as follows: 00 = No Fault 01 = Link Failure detected at link partner 10 = Offline 11 = Auto-neg Error
5	Sync status	RO	0x0	0x0	1 = Sync 0 = No Sync
4	Fiber Energy Detect Status	RO	0x1	0x1	1 = No energy detected 0 = Energy Detected
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 0. 1 = Transmit pause enabled 0 = Transmit pause disable
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 0. 1 = Receive pause enabled 0 = Receive pause disabled
1:0	Reserved	RO	Always 00	Always 00	00

Table 110: Fiber Interrupt Enable Register
Page 1, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	0
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 110: Fiber Interrupt Enable Register
Page 1, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	Fiber FIFO Over/ Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6	Reserved	RO	Always 0	Always 0	0
5	Remote Fault Receive Interrupt Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
4	Fiber Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3:0	Reserved	RO	Always 0000	Always 0000	0000

Table 111: Fiber Interrupt Status Register
Page 1, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	0
14	Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed

Table 111: Fiber Interrupt Status Register
Page 1, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	Fiber FIFO Over/ Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6	Reserved	RO	0x0	0x0	0
5	Remote Fault Receive Interrupt Enable	RO, LH	0x0	0x0	1 = Remote Fault received changed, read 1.17.7:6 for detail 0 = No change on remote fault received
4	Fiber Energy Detect Changed	RO,LH	0x0	0x0	1 = Energy Detect state changed 0 = No Energy Detect state change detected
3:0	Reserved	RO	Always 00000	Always 00000	00000

Table 112: Fiber Receive Error Counter Register
Page 1, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

Table 113: PRBS Control
Page 1, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Set to 0s
7	Invert Checker Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
6	Invert Generator Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
5	PRBS Lock	R/W	0x0	Retain	0 = Counter Free Runs 1 = Do not start counting until PRBS locks first

Table 113: PRBS Control
Page 1, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Clear Counter	R/W, SC	0x0	0x0	0 = Normal 1 = Clear Counter
3:2	Pattern Select	R/W	0x0	Retain	00 = PRBS 7 01 = PRBS 23 10 = PRBS 31 11 = Generate 1010101010... pattern
1	PRBS Checker Enable	R/W	0x0	0x0	0 = Disable 1 = Enable
0	PRBS Generator Enable	R/W	0x0	0x0	0 = Disable 1 = Enable

Table 114: PRBS Error Counter LSB
Page 1, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count LSB	RO	0x0000	Retain	A read to this register freezes register 25_1. Cleared only when register 23_1.4 is set to 1.

Table 115: PRBS Error Counter MSB
Page 1, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count MSB	RO	0x0000	Retain	This register does not update unless register 24_1 is read first. Cleared only when register 23_1.4 is set to 1.

Table 116: Fiber Specific Control Register 2
Page 1, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INT	R/W	0x0	Retain	1 = Force INTn to assert 0 = Normal Operation
14	1000BASE-X Noise Filtering	R/W	0x0	Retain	1 = Enable 0 = Disable
13:10	Reserved	R/W	0x0	Retain	Must set to 0

Table 116: Fiber Specific Control Register 2
Page 1, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
9	FEFI Enable	R/W	0x0	Retain	100BASE-FX FEFI 1 = Enable 0 = Disable
8:7	Reserved	R/W	0x0	Retain	Must set to 0
6	Serial Interface Auto-Negotiation bypass enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. 1 = Bypass Allowed 0 = No Bypass Allowed
5	Serial Interface Auto-Negotiation bypass status	RO	0x0	0x0	1 = Serial interface link came up because bypass mode timer timed out and fiber Auto-Negotiation was bypassed. 0 = Serial interface link came up because regular fiber Auto-Negotiation completed. If this bit is 1, then bit 17_1.11 will be 0.
4	Reserved	R/W	0x0	Update	Must set to 0
3	Fiber Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable
2:0	SGMII Output Amplitude	R/W	0x2	Retain	Differential voltage peak measured. See AC/DC section for valid VOD values. 000 = 14mV 001 = 112mV 010 = 210 mV 011 = 308mV 100 = 406mV 101 = 504mV 110 = 602mV 111 = 700mV

Table 117: MAC Specific Control Register 1
Page 2, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Copper Transmit FIFO Depth	R/W	0x1	Retain	00 = ± 16 Bits 01 = ± 24 Bits 10 = ± 32 Bits 11 = ± 40 Bits
13	Reserved	R/W	0x0	Retain	

Table 117: MAC Specific Control Register 1
Page 2, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
12	RCLK Frequency Select	R/W	0x0	Retain	Selects the frequency of RCLK (the SyncE clock that goes out of the CLK125 output pin) 0 = 25 MHz 1 = 125 MHz
11	RCLK Link Down Disable	R/W	0x0	Retain	Selects what the RCLK output is during link down and 10BT. 0 = RCLK is the 25 MHz XTAL1 clock 1 = RCLK is low
10	RCLK enable	R/W	0x1	Retain	1 = Enable RCLK 0 = Disable RCLK
9:7	Reserved	R/W	0x0	Retain	
6	Pass Odd Nibble Preambles	R/W	0x1	Update	0 = Pad odd nibble preambles in copper receive packets. 1 = Pass as is and do not pad odd nibble preambles in copper receive packets.
5	Reserved	R/W	0x0	Retain	
4	Reserved	R/W	0x0	Retain	
3	RGMII Interface Power Down	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. This bit determines whether the RGMII RX_CLK powers down when Register 0.11, 16_0.2 are used to power down the device or when the PHY enters the energy detect state. 1 = Always power up 0 = Can power down
2	Disable CLK125	R/W	0x0	Retain	0 = Enable internally generated 125 MHz clock 1 = Disable internally generated 125 MHz clock
1	CLK125 Pin Output Disable	R/W	0x0	Retain	Disables the CLK125 output pin (tristates it) regardless of the enabled clock source. 1 = Stop the current clock selected from going out the CLK125 pin and tristate the output 0 = Allow the current clock selected to go out the CLK125 pin
0	CLK125 Pin Output Source Select	R/W	0x0	Retain	Selects the clock source for the CLK125 output pin. 1 = Enable RCLK to go out the CLK125 pin 0 = Enable the internally generated 125 MHz clock to go out the CLK125 pin.

Table 118: MAC Specific Interrupt Enable Register
Page 2, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	000000000
7	Copper FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:4	Reserved	R/W	0x0	Retain	000
3	Copper FIFO Idle Inserted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	Copper FIFO Idle Deleted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1:0	Reserved	R/W	0x0	Retain	00

Table 119: MAC Specific Status Register
Page 2, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 00	Always 00	00000000
7	Copper FIFO Over/Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6:4	Reserved	RO	Always 0	Always 0	000
3	Copper FIFO Idle Inserted	RO,LH	0x0	0x0	1 = Idle Inserted 0 = No Idle Inserted
2	Copper FIFO Idle Deleted	RO,LH	0x0	0x0	1 = Idle Deleted 0 = Idle not Deleted
1:0	Reserved	RO	Always 0	Always 0	00

Table 120: Copper RX_ER Byte Capture
Page 2, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Capture Data Valid	RO	0x0	0x0	1 = Bits 14:0 Valid 0 = Bits 14:0 Invalid
14	Reserved	RO	0x0	0x0	0
13:12	Byte Number	RO	0x0	0x0	00 = 4 bytes before RX_ER asserted 01 = 3 bytes before RX_ER asserted 10 = 2 bytes before RX_ER asserted 11 = 1 byte before RX_ER asserted The byte number increments after every read when register 20_2.15 is set to 1.
11:10	Reserved	RO	0x0	0x0	000
9	RX_ER	RO	0x0	0x0	RX Error. Normally this bit will be low since the capture is triggered by RX_ER being high. However it is possible to see an RX_ER high when the capture is re-enabled after reading the fourth byte and there happens to be a long sequence of RX_ER when the capture restarts.
8	RX_DV	RO	0x0	0x0	RX Data Valid
7:0	RXD[7:0]	RO	0x00	0x00	RX Data

Table 121: MAC Specific Control Register 2
Page 2, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	0
14	Copper Line Loopback	R/W	0x0	0x0	1 = Enable Loopback of MDI to MDI 0 = Normal Operation
13	Default MAC interface speed (LSB)	R/W	0x0	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. Also, used for setting speed of MAC interface during MAC side loopback. Requires that customer set both these bits and force speed using register 0 to the same speed. MAC Interface Speed during Link down. Bits 6,13 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps

Table 121: MAC Specific Control Register 2
Page 2, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
12:7	Reserved		0x20	0x20	Reserved.
6	Default MAC interface speed (MSB)	R/W	0x1	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. Also, used for setting speed of MAC interface during MAC side loopback. Requires that customer set both these bits and force speed using register 0 to the same speed. MAC Interface Speed during Link down. Bits 6, 13 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps
5	RGMII Receive Timing Control	R/W	0x1	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Receive clock transition when data stable 0 = Receive clock transition when data transitions
4	RGMII Transmit Timing Control	R/W	0x1	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Transmit clock internally delayed 0 = Transmit clock not internally delayed
3	Block Carrier Extension Bit	R/W	0x0	Retain	1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension
2:0	Reserved	R/W	0x6	0x6	Reserved.

Table 122: RGMII Output Impedance Calibration Override
Page 2, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Restart Calibration	R/W, SC	0x0	Retain	Calibration will start once bit 15 is set to 1. 0 = Normal 1 = Restart
14	Calibration Complete	RO	0x0	Retain	Calibration is done once bit 14 becomes 1. 0 = Not done 1 = Done

Table 122: RGMII Output Impedance Calibration Override
Page 2, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
13	VDDO Level	R/W	See Descr.	Retain	VDDO level- must be programmed to indicate the VDDO supply voltage used for the E1510/E1512 parts. This value is a don't care for E1518 parts (VDDO is 1.8V). The bit mapping is: 0 = 3.3V 1 = 2.5V If the CONFIG pin input values bit 1:0 are: 00, then VDDO Level = 3.3V 11, then VDDO Level = 3.3V 10, then VDDO Level = 2.5V 01, then VDDO Level = 2.5V Note: 3.3V is assumed initially until this value is changed.
12	1.8V VDDO Used	R/O	See Descr	Retain	This bit indicates whether VDDO = 1.8V is used or not. 1 = VDDO = 1.8V 0 = VDDO = 2.5V or 3.3V
11:8	PMOS Value	R/W	See Descr	Retain	0000 = All fingers off 1111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once 24_2.6 is set to 1 the new calibration value is written into the I/O pad. The automatic calibrated value is lost.
7	Reserved	RW	0x0	Retain	Reserved.
6	Force PMOS/ NMOS	R/W	0x0	Retain	1 = Force value from 24_2.11:8 to PMOS, and 24_2.3:0 to NMOS. (Used for manual settings)
5:4	Reserved	R/O	0x0	Retain	Reserved.
3:0	NMOS value	R/W	See Descr	Retain	0000 = All fingers off 1111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once 24_2.6 is set to 1 the new calibration value is written into the I/O pad. The automatic calibrated value is lost.

Table 123: RGMII Output Impedance Target
Page 2, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x000	Retain	Reserved.

Table 123: RGMII Output Impedance Target
Page 2, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
2:0	Calibration target	RW	0x3	Retain	000 = 78.8 Ohm 001 = 64.5 Ohm 010 = 54.6 Ohm 011 = 47.3 Ohm 100 = 41.7 Ohm 101 = 37.3 Ohm 110 = 33.8 Ohm 111 = 30.9 Ohm

Table 124: LED[2:0] Function Control Register
Page 3, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x1	Retain	
11:8	LED[2] Control	R/W	0x0	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On- Full Duplex, Blink- Collision, Off- Half Duplex 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10/1000 Mbps Link, Off - Else 0111 = On - 10 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
7:4	LED[1] Control	R/W	0x1	Retain	If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On- Receive, Off- No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On- 100 Mbps Link/ Fiber Link 0110 = On - 100/1000 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved

Table 124: LED[2:0] Function Control Register
Page 3, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	LED[0] Control	R/W	0xE	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 1 blink - 10 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

Table 125: LED[2:0] Polarity Control Register
Page 3, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	LED[1] mix percentage	R/W	0x4	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
11:8	LED[0] mix percentage	R/W	0x4	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ..., 0111 = 87.5%, 1000 = 100% 1001 to 1111 = Reserved
7:6	Reserved	R/W	0x0	Retain	Reserved.

Table 125: LED[2:0] Polarity Control Register
Page 3, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
5:4	LED[2] Polarity	R/W	0x0	Retain	00 = On - drive LED[2] low, Off - drive LED[2] high 01 = On - drive LED[2] high, Off - drive LED[2] low 10 = On - drive LED[2] low, Off - tristate LED[2] 11 = On - drive LED[2] high, Off - tristate LED[2]
3:2	LED[1] Polarity	R/W	0x0	Retain	00 = On - drive LED[1] low, Off - drive LED[1] high 01 = On - drive LED[1] high, Off - drive LED[1] low 10 = On - drive LED[1] low, Off - tristate LED[1] 11 = On - drive LED[1] high, Off - tristate LED[1]
1:0	LED[0] Polarity	R/W	0x0	Retain	00 = On - drive LED[0] low, Off - drive LED[0] high 01 = On - drive LED[0] high, Off - drive LED[0] low 10 = On - drive LED[0] low, Off - tristate LED[0] 11 = On - drive LED[0] high, Off - tristate LED[0]

Table 126: LED Timer Control Register
Page 3, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INT	R/W	0x0	Retain	1 = Force INTn to assert 0 = Normal Operation
14:12	Pulse stretch duration	R/W	0x4	Retain	000 = No pulse stretching 001 = 21 ms to 42ms 010 = 42 ms to 84ms 011 = 84 ms to 170ms 100 = 170 ms to 340ms 101 = 340 ms to 670ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11	Interrupt Polarity	R/W	0x1	Retain	0 = INTn active high 1 = INTn active low
10:8	Blink Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7	Interrupt Enable	R/W	0x0	Retain	Allows the INTn output to be brought out on LED[2]. 1 = INTn is brought out LED[2] 0 = LED[2] outputs based on current LED[2] functionality
6:4	Reserved	R/W	0x0	Retain	000

Table 126: LED Timer Control Register
Page 3, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84ms 01 = 170ms 10 = 340ms 11 = 670ms

Table 127: PTP LED Function Control
Page 3, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	R/W	0x0	Retain	Reserved.
13	Block PTP Activity	R/W	0x0	Retain	1 = Block PTP activity from lighting the LEDs 0 = Allow PTP activity to light the LEDs
12:0	Reserved	R/W	0x0073	Retain	0x0000

Table 128: RGMII RX_ER Byte Capture
Page 4, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Capture Data Valid	RO	0x0	Retain	1 = Bits 14:0 Valid 0 = Bits 14:0 Invalid
14	Reserved	RO	0x0	Retain	Reserved.
13:12	Byte Number	RO	0x0	Retain	00 = 4 bytes before RX_ER asserted 01 = 3 bytes before RX_ER asserted 10 = 2 bytes before RX_ER asserted 11 = 1 byte before RX_ER asserted The byte number increments after every read when register 20_4.15 is set to 1.
11:10	Reserved	RO	0x0	Retain	Reserved.
9	RX_ER	RO	0x0	Retain	RX Error. Normally this bit will be low since the capture is triggered by RX_ER being high. However it is possible to see an RX_ER high when the capture is re-enabled after reading the fourth byte if there happens to be a long sequence of RX_ER when the capture restarts.

Table 128: RGMII RX_ER Byte Capture
Page 4, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
8	RX_DV	RO	0x0	Retain	RX Data Valid
7:0	RXD[7:0]	RO	0x00	Retain	RX Data

Table 129: Advanced VCT TX to MDI[0] Rx Coupling
Page 5, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) Each bit above represents an increase in 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 100 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 100 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Table 130: Advanced VCT TX to MDI[1] Rx Coupling
Page 5, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection

Table 130: Advanced VCT TX to MDI[1] Rx Coupling
Page 5, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 101 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 101 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Table 131: Advanced VCT TX to MDI[2] Rx Coupling
Page 5, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 110 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 110 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Table 132: Advanced VCT TX to MDI[3] Rx Coupling
Page 5, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 111 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 111 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Table 133: 1000BASE-T Pair Skew Register
Page 5, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Pair 7,8 (MDI[3]±)	RO	0x0	Retain	Skew = Bit value x 8n s. Value is correct to within ± 8 ns. The contents of 20_5.15:0 are valid only if Register 21_5.6 = 1
11:8	Pair 4,5 (MDI[2]±)	RO	0x0	Retain	Skew = bit value x 8 ns. Value is correct to within ± 8 ns.
7:4	Pair 3,6 (MDI[1]±)	RO	0x0	Retain	Skew = bit value x 8ns. Value is correct to within ± 8 ns.
3:0	Pair 1,2 (MDI[0]±)	RO	0x0	Retain	Skew = bit value x 8 ns. Value is correct to within ± 8ns.

Table 134: 1000BASE-T Pair Swap and Polarity
Page 5, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	Retain	
6	Register 20_5 and 21_5 valid	RO	0x0	Retain	The contents of 21_5.5:0 and 20_5.15:0 are valid only if Register 21_5.6 = 1 1= Valid 0 = Invalid
5	C, D Crossover	RO	0x0	Retain	1 = Channel C received on MDI[2]± Channel D received on MDI[3]± 0 = Channel D received on MDI[2]± Channel C received on MDI[3]±
4	A, B Crossover	RO	0x0	Retain	1 = Channel A received on MDI[0]± Channel B received on MDI[1]± 0 = Channel B received on MDI[0]± Channel A received on MDI[1]±
3	Pair 7,8 (MDI[3]±) Polarity	RO	0x0	Retain	1 = Negative 0 = Positive
2	Pair 4,5 (MDI[2]±) Polarity		0x0	Retain	1 = Negative 0 = Positive
1	Pair 3,6 (MDI[1]±) Polarity	RO	0x0	Retain	1 = Negative 0 = Positive
0	Pair 1,2 (MDI[0]±) Polarity	RO	0x0	Retain	1 = Negative 0 = Positive

Table 135: Advance VCT Control
Page 5, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable Test	R/W, SC	0x0	Retain	0 = Disable test 1 = Enable test This bit will self clear when the test is completed
14	Test status	RO	0x0	Retain	0 = Test not started/in progress 1 = Test completed

Table 135: Advance VCT Control
Page 5, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
13:11	Transmitter Channel Select	R/W	0x0	Retain	000 - Tx 0 => Rx 0, Tx 1 => Rx 1, Tx 2 => Rx 2, Tx 3 => Rx 3. 100 - Tx 0 => Rx 0, Tx 0 => Rx 1, Tx 0 => Rx 2, Tx 0 => Rx 3. 101 - Tx 1 => Rx 0, Tx 1 => Rx 1, Tx 1 => Rx 2, Tx 1 => Rx 3. 110 - Tx 2 => Rx 0, Tx 2 => Rx 1, Tx 2 => Rx 2, Tx 2 => Rx 3. 111 - Tx 3 => Rx 0, Tx 3 => Rx 1, Tx 3 => Rx 2, Tx 3 => Rx 3. 01x - reserved 0x1 - reserved
10:8	Number of Sample Averaged	R/W	6	Retain	0 = 2 samples 1 = 4 samples 2 = 8 samples 3 = 16 samples 4 = 32 samples 5 = 64 samples 6 = 128 samples 7 = 256 samples
7:6	Mode	R/W	0x0	Retain	00 = Maximum peak above threshold 01 = First or last peak above threshold. See register 28_5.13. 10 = Offset 11 = Sample point at distance set by 24_5.9:0
5:0	Peak Detection Hysteresis	R/W	0x03	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x3F = ± 492 mv

Table 136: Advanced VCT Sample Point Distance
Page 5, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	Retain	Reserved.
9:0	Distance to measure/ Distance to start	R/W	0x000	Retain	When 23_5.7:6 = 11 the measurement is taken at this distance. (00 to 3FF) When 23_5.7:6 = 0x any distance below this distance is not considered (00 to FF). Bit 9:8 is ignored.

Table 137: Advanced VCT Cross Pair Positive Threshold
Page 5, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	Reserved.
14:8	Cross Pair Positive Threshold > 30m	R/W	0x01	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 9.92 mV
7	Reserved	RO	0x0	Retain	Reserved.
6:0	Cross Pair Positive Threshold < 30m	R/W	0x04	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mV

Table 138: Advanced VCT Same Pair Impedance Positive Threshold 0 and 1
Page 5, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	Reserved.
14:8	Same-Pair Positive Threshold 10m - 50m	R/W	0x0F	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 9.92 mV
7	Reserved	RO	0x0	Retain	Reserved.
6:0	Same-Pair Positive Threshold < 10m	R/W	0x12	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 9.92 mV

Table 139: Advanced VCT Same Pair Impedance Positive Threshold 2 and 3
Page 5, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	Reserved.
14:8	Same-Pair Positive Threshold 110m - 140m	R/W	0x0A	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 9.92 mv
7	Reserved	RO	0x0	Retain	Reserved.

Table 139: Advanced VCT Same Pair Impedance Positive Threshold 2 and 3
Page 5, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
6:0	Same-Pair Positive Threshold 50m - 110m	R/W	0x0C	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 9.92 mv

Table 140: Advanced VCT Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control
Page 5, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	Retain	0
13	First Peak/Last Peak Select	R/W	0x0	Retain	This register takes effect only if register 23_5.7:6 = 01. 0 = First Peak 1 = Last Peak
12	Break Link Prior to Measurement	R/W	0x0	Retain	1 = Do not wait 1.5s to break link before starting VCT 0 = Wait 1.5s to break link before starting VCT
11:10	Transmit Pulse Width	R/W	0x0	Retain	00 = Full pulse (128 ns) 01 = 3/4 pulse 10 = 1/2 pulse 11 = 1/4 pulse
9:8	Transmit Amplitude	R/W	0x0	Retain	00 = Full amplitude 01 = 3/4 amplitude 10 = 1/2 amplitude 11 = 1/4 amplitude

7	Distance Measurement Point	R/W	0x0	Retain	If 23_5.7:6 = 00 then
					0 = Measure distance when amplitude drops to 50% of peak amplitude
					1 = Measure distance at actual maximum amplitude
					If 23_5.7:6 = 01 then
					0 = Measure distance when amplitude drops below hysteresis
					1 = Measure distance at actual maximum amplitude
					If 23_5.7:6 = 1X then this bit is ignored.

6:0	Same-Pair Positive Threshold > 140m	R/W	0x06	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mv

Table 141: Copper Port Packet Generation
Page 6, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7	Packet Generator Transmit Trigger	R/W	0x0	Retain	This bit is only valid when all of the following are true: bit 6 =1 bit3 =1 bit15:8 is not equal to all 0s A read of this bit gives the following: 1: Packet generator transmit done 0: Packet generator is transmitting data When this bit is 1 a write of 0 will trigger the packet generator to transmit again. When this bit is 0 a write of 0 or 1 will have no effect.
6	Packet Generator Enable Self Clear Control	R/W	0x0	Retain	0 = Bit 3 will self clear after all packets are sent 1 = Bit 3 will stay high after all packets are sent
5	Reserved	R/W	0x0	Retain	Reserved
4	Enable CRC Checker	R/W	0x0	Retain	1 = Enable 0 = Disable
3	Enable Packet Generator	R/W	0x0	Retain	1 = Enable 0 = Disable
2	Payload of Packet to Transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,...
1	Length of Packet to Transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored Packet	R/W	0x0	Retain	1 = Tx packets with CRC errors & Symbol Error 0 = No error

Table 142: Copper Port CRC Counters
Page 6, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Count	RO	0x00	Retain	0x00 = No packets received 0xFF = 256 packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00= NoCRCerrorsdetectedinthepacketsreceived. 0xFF = 256 CRC errors detected in the packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid.

Table 143: Checker Control
Page 6, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x000	Retain	Set to 0s
4	CRC Counter Reset	R/W, SC	0x0	Retain	1 = Reset This bit will self-clear after writing 1.
3	Enable Stub Test	R	0x0	Retain	1 = Enable stub test 0 = Normal Operation
2:0	Reserved	R/W	0x0	Retain	Reserved.

Table 144: Copper Port Packet Generation
Page 6, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Reserved.
7:0	IPG Length	R/W	8'd12	Retain	The number in bit [7:0]+1 is the number of bytes for IPG

Table 145: General Control Register
Page 6, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	R/W	0x00	Retain	Reserved.
9	PTP Power Down	R/W	0x1	Retain	1 = Power Down 0 = Power Up

Table 145: General Control Register
Page 6, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
8	PTP Reference Clock Source	R/W	0x0	Retain	1 = Use 125 MHz clock applied to the CONFIG pin after configuration is completed 0 = Use internal 125 MHz clock
7	PTP Input Source	R/W	0x0	Retain	1 = Use LED[1] pin for PTP input trigger pulse after configuration is completed 0 = Force input to 0
6	PTP Output Source	R/W	0x0	Retain	1 = Use LED[1] pin for PTP output trigger pulse after configuration is completed 0 = Use LED[1] for non-PTP functions
5:0	Reserved	R/W	0x00	Retain	Reserved.

Table 146: Late Collision Counters 1 & 2
Page 6, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Late Collision 97-128 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 97th to 128th bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.
7:0	Late Collision 65-96 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 65th to 96th bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.

Table 147: Late Collision Counters 3 & 4
Page 6, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Late Collision >192 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half duplex and a start of packet is received after 192 bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.

Table 147: Late Collision Counters 3 & 4
Page 6, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Late Collision 129-192 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 129th to 192nd bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.

Table 148: Late Collision Window Adjust/Link Disconnect
Page 6, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	R/W	0x0	Retain	Set to 0s
12:8	Late Collision Window Adjust	R/W	0x00	Retain	Number of bytes to advance in late collision window. 0 = start at 64th byte, 1 = start at 63rd byte, etc.
7:0	Reserved	R/W	0x00	Retain	Set to 0s

Table 149: Misc Test
Page 6, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TX_TCLK Enable	R/W	0x0	0x0	The bit enables driving the transmit clock to the HSDACP/N pin. 1 = Enable 0 = Disable
14:13	Temperature Sensor Acceleration	R/W	0x0	Retain	00 = Sample once per second 01 = Sample once per 10ms 1x = Disable Polling
12:8	Temperature Threshold	R/W	0x19	Retain	Temperature in C = 5 x 26_6.4:0 - 25 i.e. for 100C the value is 11001
7	Temperature Sensor Interrupt Enable	R/W	0x0	Retain	1 = Interrupt Enable 0 = Interrupt Disable
6	Temperature Sensor Interrupt	RO, LH	0x0	Retain	1 = Temperature Reached Threshold 0 = Temperature Below Threshold
5	Temperature Manual Control	R/W	0x0	Retain	Manual Control of temp_sense_en 1 = Temperature Acquire 0 = Temperature Read Set register 250_8.5:4 = 10 to use

Table 149: Misc Test
Page 6, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
4:0	Temperature Sensor	RO	xxxxx	xxxxx	Temperature is the 5MSBs of temperature value - Temp_val[5:1]

Table 150: Misc Test: Temperature Sensor Alternative Reading
Page 6, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	R/W	0x0	Retain	Reserved.
12:11	Temp Sensor: Number to average samples	R/W	2'b01	Retain	00: average over 2^9 samples 01: average over 2^11 samples 10: average over 2^13 samples 11: average over 2^15 samples
10:8	Temp Sensor: sampling rate	R/W	3'b100	Retain	Sampling rate 000: 28 us 001: 56 us 010: 168 us 011: 280 us 100: 816 us 101: 2.28 ms 110: 6.22 ms 111: 11.79 ms
7:0	Temperature Sensor Alternative reading	RO	xxxxx	Retain	Temperature in C = 1 x 27_6.7:0 - 25 i.e. for 100C the value is 0111_1101

Table 151: PHY Cable Diagnostics Pair 0 Length
Page 7, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Pair 0 Cable Length	RO	0x0000	Retain	Length to fault in meters or centimeters based on register 21_7.10.

Table 152: PHY Cable Diagnostics Pair 1 Length
Page 7, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Pair 1 Cable Length	RO	0x0000	Retain	Length to fault in meters or centimeters based on register 21_7.10.

Table 153: PHY Cable Diagnostics Pair 2 Length
Page 7, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Pair 2 Cable Length	RO	0x0000	Retain	Length to fault in meters or centimeters based on register 21_7.10.

Table 154: PHY Cable Diagnostics Pair 3 Length
Page 7, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Pair 3 Cable Length	RO	0x0000	Retain	Length to fault in meters or centimeters based on register 21_7.10.

Table 155: PHY Cable Diagnostics Results
Page 7, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Pair 3 Fault Code	RO	0x0	Retain	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved
11:8	Pair 2 Fault Code	RO	0x0	Retain	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved

Table 155: PHY Cable Diagnostics Results
Page 7, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	Pair 1 Fault Code	RO	0x0	Retain	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved
3:0	Pair 0 Fault Code	RO	0x0	Retain	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved

Table 156: PHY Cable Diagnostics Control
Page 7, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Run Immediately	R/W, SC	0x0	Retain	0 = No Action 1 = Run VCT Now
14	Run At Each Auto-Negotiation Cycle	R/W	0x1	Retain	0 = Do No Run At Auto-Negotiation Cycle 1 = Run At Auto-Negotiation Cycle
13	Disable Cross Pair Check	R/W	0x0	Retain	0 = Enable Cross Pair Check 1 = Disable Cross Pair Check
12	Run After Break Link	R/W, SC	0x0	Retain	0 = No Action 1 = Run VCT After Breaking Link
11	Cable Diagnos-tics Status	RO	0x0	Retain	0 = Complete 1 = In Progress
10	Cable Length Unit	R/W	0x0	Retain	0 = Centimeters 1 = Meters
9:0	Reserved	RO	0x00	Retain	Reserved.

Table 157: Advanced VCT Cross Pair Negative Threshold
Page 7, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	Reserved.
14:8	Cross Pair Negative Threshold > 30m	R/W	0x01	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV,..., 0x7F = - 992 mV
7	Reserved	RO	0x0	Retain	Reserved.
6:0	Cross Pair Negative Threshold < 30m	R/W	0x04	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV,..., 0x7F = - 992 mV

Table 158: Advanced VCT Same Pair Impedance Negative Threshold 0 and 1
Page 7, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	Reserved.
14:8	Same-Pair Negative Threshold 10m - 50m	R/W	0x0F	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV,..., 0x7F = - 992 mV
7	Reserved	RO	0x0	Retain	Reserved.
6:0	Same-Pair Negative Threshold < 10m	R/W	0x12	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV,..., 0x7F = - 992 mV

Table 159: Advanced VCT Same Pair Impedance Negative Threshold 2 and 3
Page 7, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	0
14:8	Same-Pair Negative Threshold 110m - 140m	R/W	0x0A	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV,..., 0x7F = - 992 mV
7	Reserved	RO	0x0	Retain	Reserved.
6:0	Same-Pair Negative Threshold 50m - 110m	R/W	0x0C	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV,..., 0x7F = - 992 mV

Table 160: Advanced VCT Same Pair Impedance Negative Threshold 4
Page 7, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	Reserved.
6:0	Same-Pair Negative Threshold > 140m	R/W	0x06	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV,..., 0x7F = - 992 mV

Table 161: PTP Port Configuration Register 0
Page 8, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	TransSpec	RWS	0x1	Retain	PTP Transport Specific value. The Transport Specific bits present in PTP Common header are used to differentiate between IEEE1588, IEEE802.1AS etc. frames. This is to differentiate between various timing protocols running on either Layer2 or higher protocol layers. In hardware, in addition to comparing the EtherType to determine that the incoming frame is a PTP frame, it compares the TransSpec bits to the incoming PTP common headers Transport Specific bits. If there is a match then hardware logic time stamps the frames indicated by MsdIDTSEn (Table 195: "PTP Global Configuration Register 1") and optionally interrupts the CPU. If there were to be no match then the hardware would not perform any operations in the PTP device. For IEEE 1588 networks this is expected to be configured to a 0x0 and for IEEE 802.1AS networks this is expected to be configured to 0x1.
11	DisTSpecCheck	RWR	0x0	Retain	Disable Transport Specific Check. 0x1= Disables checking for Transport Specific part of the PTP Common header between the incoming packet data and the configured TransSpec (bits 15:12) 0x0 = Enables checking for Transport Specific part of the PTP Common header between the incoming packet data and the configured TransSpec (bits 15:12).
10:2	Reserved	RES	0x000	Retain	Reserved

Table 161: PTP Port Configuration Register 0
Page 8, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
1	DisTSOverwrite	RWR	0x0	Retain	Disable Time Stamp Counter Overwriting. When set to 0x1, PTPArr0Time, PTPArr1Time and PTPDepTime values do not get overwritten until their corresponding valid bits are cleared. This situation only arises when a port based time stamp counter is written by hardware logic but software layer has not read the data. When set to 0x0, PTPArr0Time, PTPArr1Time and PTPDepTime values do get overwritten even though their corresponding valid bits (defined in PTP Port Status Data Structure below), are not cleared.
0	DisPTP	RWR	0x0	Retain	Disable Precise Time Stamp logic (per-port bit). 0x0 = PTP logic within the chip is enabled. 0x1 = PTP logic is disabled i.e., hardware logic does not recognize or timestamp PTP frames. Event interrupt generation logic is disabled.

Table 162: PTP Port Configuration Register 1
Page 8, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RES	0x0	Retain	Reserved
13:8	IPJump	RWS	0x02	Retain	Internet Protocol Jump. This field specifies to the PTP hardware logic how many bytes should it skip starting at the value specified by ETJump (bits 4:0). Note that this specifies the jump to the beginning of the IPv4 or IPv6 headers for the hardware parser. This allows flexibility in the hardware to skip past the protocol chains that are specific to customer networks including MPLS etc. For example if ETJump is programmed to 0xC and IPJump is programmed to 0x16, this indicates the hardware to skip 0x22 bytes in order to get to the IP header. It can either be IPv4 or IPv6 header.
7:5	Reserved	RES	0x0	Retain	Reserved

Table 162: PTP Port Configuration Register 1 (Continued)
Page 8, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
4:0	ETJump	RWS	0x0C	Retain	EtherType Jump. This field specifies to the PTP hardware logic how many bytes should it skip starting from MAC-DA of the frame to get to the EtherType of the frame. The hardware would skip so many bytes and then compare the next 2 bytes to the configured PTPEType (PTP Global Configuration Register 0, Page 8, Register 0). This allows flexibility in the hardware to skip past the protocol chains that are specific to customer networks including IEEE802.1q tag, Provider tag etc.

Table 163: PTP Port Configuration Register 2
Page 8, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RES	0x0000	Retain	Reserved
1	PTPDepIntEn	RWR	0x0	Retain	Precise Time Protocol Port Departure Interrupt enable. This field indicates the per-port interrupt enable for outgoing PTP frame from a given port. When a bit is enabled in this field it indicates that whenever hardware logic time stamps a PTP frame to this port, it needs to send an interrupt to the CPU. 0x0 = Disable PTP departure counter based interrupt generation. Even if the PTPDepTimeValid is set to 0x1, PTPInt is not set and interrupt doesn't get generated by hardware logic for outgoing PTP frames. 0x1 = Enable PTP departure counter based interrupt generation. If the PTPDepTimeValid is set to 0x1, PTPInt is set and interrupt gets generated by hardware logic for outgoing PTP frames. Note that hardware logic only time stamps the PTP frames when configured to do so by MsdIDTSEn field (Table 195, "PTP Global Configuration Register 1," on page 211).

Table 163: PTP Port Configuration Register 2 (Continued)
Page 8, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PTPArrIntEn	RWR	0x0	Retain	Precise Time Protocol Port Arrival Interrupt enable. This field indicates the per-port interrupt enable for incoming PTP frames from a given port. When a bit is enabled in this field it indicates that whenever hardware logic time stamps a PTP frame from this port, it needs to send an interrupt to the CPU. 0x0 = Disable PTP arrival counter based interrupt generation. Even if the PTPArr0TimeValid or PTPArr1TimeValid is set to 0x1 for that port, PTPInt is not set and interrupt doesn't get generated by hardware logic for incoming PTP frames from this port. 0x1 = Enable PTP arrival counter based interrupt generation. If the PTPArr0TimeValid or PTPArr1TimeValid is set to 0x1, PTPInt is set and interrupt gets generated by hardware logic for incoming PTP frames. Note that hardware logic only time stamps the PTP frames when configured to do so by MsdIDTSEn field (Table 195, "PTP Global Configuration Register 1," on page 211).

Table 164: PTP Port Configuration Register 3
Page 8, Register 3

Bits	Field	Type	HW Rst	SW Rst	Description
15:8	ArrLEDCtrl	RWR			LED control for packets departing the device. When 0x0, if a received frame is classified as a PTP frame, the LED does not blink. But it blinks for every non-PTP frame. When 0x1, the LED blinks for every received frame classified as a PTP frame. It also blinks for every non-PTP frame. When 0xn, the LED blinks for every n received frames classified as PTP. It also blinks for every non-PTP frame. **NOTE:** This logic tracks all received PTP frames (even though the PTP core time stamps only the PTP event messages) and not just PTP frames that need time stamping.
7:0	DepLEDCtrl	RWS 0x80			LED control for packets departing the device. When 0x0, if a transmitting frame is classified as a PTP frame, the LED does not blink. But it blinks for every non-PTP frame. When 0x1, the LED blinks for every transmitting frame classified as a PTP frame. It also blinks for every non-PTP frame. When 0xn, the LED blinks for every n transmitting frames classified as PTP. It also blinks for every non-PTP frame. **NOTE:** This logic tracks all transmitting PTP frames (even though the PTP core time stamps only the PTP event messages) and not just PTP frames that need time stamping.

Table 165: PTP Arrival 0 Time Port Status Register
Page 8, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RES	0x0000	Retain	Reserved
2:1	PTPArr0IntStatus	RWR	0x0	Retain	Precise Time Protocol Arrival 0 Time Interrupt Status The PTP Arrival 0 time Interrupt bit gets set for a given port when an incoming PTP frame is time stamped in PTPArr0Time counter. 0x0 = Normal i.e., none of the error conditions stated below are valid for this packet. 0x1 = If the PTPArr0Time counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use Arrival 0 counters arrived into the device through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = If the incoming frame could not be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPArr0TimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can happen when there is more than one PTP frame that needs time stamping into Arrival 0 counters arrives into the device before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the device for policy, CRC, queue congestion or any other reasons then one of the PTP arrival discard counters get updated (PTPNonTSArrDisCtr or PTPTSArrDisCtr). See the discard counter description for further details.

Table 165: PTP Arrival 0 Time Port Status Register (Continued)
Page 8, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PTPArr0TimeValid	RWR	0x0	Retain	Precise Time Protocol Arrival 0 Time Valid When the PTPArr0Time value is updated by hardware, this bit is set to a 0x1 validating the time counter. 0x0= PTPArr0Time is not valid. 0x1= PTPArr0Time is valid and PTPArr0IntStatus represents the status information for the PTPArr0Time counter. Note that this is set by hardware for the frames which are assured to reach the CPU. For frames with CRC error etc., this bit will not be set but either PTPNonTSArrCtr or PTPTSArrCtr is updated. **NOTE:** This valid bit needs to be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware has no way to figure out if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

Table 166: PTP Arrival 0 Time Register Bytes 1 & 0
Page 8, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	PTPArr0 Time Byte 1	RWR	0x00000000	Retain	Precise Time Protocol Arrival 0 Time counter Byte 1. These bits contain bits 15:8 of the PTP Arrival 0 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above.

Table 166: PTP Arrival 0 Time Register Bytes 1 & 0 (Continued)
Page 8, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	PTPArr0 Time Byte 0	RWR	0x00000000	Retain	Precise Time Protocol Arrival 0 Time counter Byte 0. These bits contain bits 7:0 of the PTP Arrival 0 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above.

Table 167: PTP Arrival 0 Time Register Bytes 3 & 2
Page 8, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	PTPArr0 Time Byte 3	RWR	0x00000000	Retain	Precise Time Protocol Arrival 0 Time counter Byte 3. These bits contain bits 31:24 of the PTP Arrival 0 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above.
7:0	PTPArr0 Time Byte 2	RWR	0x00000000	Retain	Precise Time Protocol Arrival 0 Time counter Byte 2. These bits contain bits 23:16 of the PTP Arrival 0 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above.

Table 168: PTP Arrival 0 Sequence Identifier Register
Page 8, Register 11

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPArr0SeqId	RWR	0x0000	Retain	Precise Time Protocol Arrival 0 Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPArr0Time register.

Table 169: PTP Arrival 1 Time Port Status Register
Page 8, Register 12

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RES	0x0000	0x0000	Reserved
2:1	PTPArr1IntStatus	RWR	0x0	Retain	Precise Time Protocol Arrival 1 Time Interrupt Status The PTP Arrival 1 time Interrupt bit gets set for a given port when an incoming PTP frame is time stamped in PTPArr1Time counter. 0x0 = Normal i.e., none of the error conditions stated below are valid for this packet. 0x1 = If the PTPArr1Time counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use Arrival 1 counters arrived into the device through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = If the incoming frame could not be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPArr1TimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can happen when there is more than one PTP frame that needs time stamping into arrival 1 counters arrives into the device before CPU clears the valid bits for the previous frame. 0x3 = Reserved Note that if the PTP frame gets discarded inside the device for policy, CRC, queue congestion or any other reasons then one of the PTP arrival discard counters get updated (PTPNonTSArrDisCtr or PTPTSArrDisCtr). See the discard counter description for further details.

Table 169: PTP Arrival 1 Time Port Status Register (Continued)
Page 8, Register 12

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PTPArr1TimeValid	RWR	0x0	Retain	Precise Time Protocol Arrival 1 Time Valid When the PTPArr1Time value is updated by hardware, this bit is set to a 0x1 validating the time counter. 0x0= PTPArr1Time is not valid. 0x1= PTPArr1Time is valid and PTPArr1IntStatus represents the status information for the PTPArr1Time counter. Note that this is set by hardware for the frames which are assured to reach the CPU. For frames with CRC error etc., this bit will not be set but either PTPNonTSArrCtr or PTPTSArrCtr is updated. Note that this valid bit needs to be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware has no way to figure out if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

Table 170: PTP Arrival 1 Time Register Bytes 1 & 0
Page 8, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	PTPArr1 Time Byte 1	RWR	0x00000000	Retain	Precise Time Protocol Arrival 1 Time counter Byte 1. These bits contain bits 15:8 of the PTP Arrival 1 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above.

Table 170: PTP Arrival 1 Time Register Bytes 1 & 0 (Continued)
Page 8, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	PTPArr1 Time Byte 0	RWR	0x00000000	Retain	Precise Time Protocol Arrival 1 Time counter Byte 0. These bits contain bits 7:0 of the PTP Arrival 1 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above.

Table 171: PTP Arrival 1 Time Register Bytes 3 & 2
Page 8, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	PTPArr1 Time Byte 3	RWR	0x00000000	Retain	Precise Time Protocol Arrival 1 Time counter Byte 3. These bits contain bits 31:24 of the PTP Arrival 1 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above.
7:0	PTPArr1 Time Byte 2	RWR	0x00000000	Retain	Precise Time Protocol Arrival 1 Time counter Byte 2. These bits contain bits 23:16 of the PTP Arrival 1 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above.

Table 172: PTP Arrival 1 Sequence Identifier Register
Page 8, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPArr1SeqId	RWR	0x0000	Retain	Precise Time Protocol Arrival 1 Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPArr1Time register.

Table 173: PTP Departure Time Port Status Register
Page 9, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RES	0x0000	Retain	Reserved
2:1	PTPDepIntStatus	RWR	0x0	Retain	Precise Time Protocol Departure Time Interrupt Status The PTP Departure time Interrupt bit gets set for a given port when an incoming PTP frame is time stamped in PTP-DepTime counter. 0x0 = Normal i.e., none of the error conditions stated below are valid for this packet. 0x1 = If the PTPDepTime counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use departure counter departed out of the device through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = If the outgoing frame could not be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPDepTimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can happen when there is more than one PTP frame that needs time stamping into departure counter leaves the device before CPU clears the valid bits for the previous frame. 0x3 = Reserved Note that if the PTP frame gets discarded inside the device for CRC reasons then the PTP departure discard counter gets updated (PTPNonTSDepDisCtr or PTPTS-DepDisCtr). See the discard counter description for further details.

Table 173: PTP Departure Time Port Status Register (Continued)
Page 9, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PTPDepTime-Valid	RWR	0x0	Retain	Precise Time Protocol Departure Time Valid When the PTPDepTime value is updated by hardware, this bit is set to a 0x1 validating the time counter. 0x0 = PTPDepTime is not valid. 0x1 = PTPDepTime is valid and PTPDepIntStatus represents the status information for the PTPDepTime counter. Note that this is set by hardware for the frames which are assured to depart the port. For frames with CRC error etc., this bit will not be set but either PTPNonTSDepCtr or PTPTSDepCtr is updated. **NOTE:** This valid bit needs to be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware has no way to figure out if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

Table 174: PTP Departure Time Register Bytes 1 & 0
Page 9, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	PTPDep Time Byte 1	RWR	0x00000000	Retain	Precise Time Protocol Departure Time counter Byte 1. This indicates the bits 15:8 of the PTP Departure time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above.

Table 174: PTP Departure Time Register Bytes 1 & 0 (Continued)
Page 9, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	PTPDep Time Byte 0	RWR	0x00000000	Retain	Precise Time Protocol Departure Time counter Byte 0. This indicates the bits 7:0 of the PTP Departure time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above.

Table 175: PTP Departure Time Register Bytes 3 & 2
Page 9, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	PTPDep Time Byte 3	RWR	0x00000000	Retain	Precise Time Protocol Departure Time counter Byte 3. This indicates the bits 31:24 of the PTP Departure time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above.
7:0	PTPDep Time Byte 2	RWR	0x00000000	Retain	Precise Time Protocol Departure Time counter Byte 2. This indicates the bits 23:16 of the PTP Departure time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a device internal clock. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above.

Table 176: PTP Departure Sequence Identifier Status Register
Page 9, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPDepSeqId	RWR	0x0000	Retain	Precise Time Protocol Departure Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPDepTime register.

Table 177: PTP Port Discard Counter Register
Page 9, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	PTPTSDepDisCtr	RWR	0x0	Retain	Precise Time Protocol Departure frame discard counter for PTP frames that need hardware time stamping. This counter is incremented by the hardware logic when ever it discards a PTP frame that needs hardware time stamping (i.e., PTPEtype is a match and MsdIDTSEn bit for the corresponding MessageID field in the outgoing PTP frame is set). The PTP frame could be discarded because of CRC reasons in egress pipe. This counter wraps around in hardware.
11:8	PTPNonTSDep-DisCtr	RWR	0x0	Retain	Precise Time Protocol Departure frame discard counter for PTP frames that do not need hardware time stamping. This counter is incremented by the hardware logic when ever it discards a PTP frame that does not need to be time stamped (i.e., PTPEtype is a match but MsdIDTSEn bit for the corresponding MessageID field in the outgoing PTP frame is not set). The PTP frame could be discarded because of CRC reasons in egress pipe. This counter wraps around in hardware.

Table 177: PTP Port Discard Counter Register (Continued)
Page 9, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	PTPTSArrDisCtr	RWR	0x0	Retain	Precise Time Protocol arrival frame discard counter for PTP frames that need hardware time stamping. This counter is incremented by the hardware logic when ever it discards a PTP frame that needs hardware time stamping (i.e., PTPEtype is a match and MsdIDTSEn bit for the corresponding MessageID field in the outgoing PTP frame is set). The PTP frame could be discarded because of CRC, Policy, Queue congestion or any other reason inside the device. This counter wraps around in hardware.
3:0	PTPNonTSAr-rDisCtr	RWR	0x0	Retain	Precise Time Protocol Non time stamp Arrival frame dis-card counter. This counter is incremented by the hardware logic when ever it discards a PTP frame that does not need hardware time stamping (i.e., PTPEtype is a match but MsdIDTSEn bit for the corresponding MessageID field in the outgoing PTP frame is not set). The PTP frame could be discarded because of CRC, Policy, Queue congestion or any other reason inside the device. This counter wraps around in hardware.

Table 178: TAI Global Configuration Register 0
Page 12, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	EventCapOv	RWR	0x0	Retain	Event Capture Overwrite When 0x1, this bit enables overwriting the EventCapRegister (Event Capture Register - Page 12, Register 10 and 11). The hardware would only overwrite the EventCapRegister if the previously captured event register has not been read by the software. When 0x0, this bit specifies to hardware logic to capture an event namely, take a snapshot of PTP Global Timer value at the rising edge of EventReq (a GPIO input into the device) and wait for software to read the EventCapRegister before capturing another event.
14	EventCtrStart	RWR	0x0	Retain	Event Counter Start When 0x1, this bit enables the hardware logic to start incrementing the EventCapCtr register (PTP Global Configuration Register 9 - Page 12, Register 9) whenever it captures a low to high transition on the EventReq signal (a GPIO input into the device). When 0x0, the EventCapCtr is not modified by hardware logic even when it captures a low to high transition on the EventReq signal.
13:10	Reserved	RES	0x0	Retain	Reserved
9	TrigGenIntEn	RWR	0x0	Retain	Trigger Generator Interrupt Enable. When 0x1, the TAI block would generate an interrupt whenever a TrigGen event has been put out on the TrigGenResp signal output. When 0x0, no interrupts are generated by the TrigGen logic.
8	EventCapIntEn	RWR	0x0	Retain	Event Capture Interrupt Enable When 0x1, the TAI block would generate an interrupt whenever an event has been captured on the EventReq signal. When 0x0, no interrupts are generated by the EventCap logic.
7:4	Reserved	RES	0x0	Retain	Reserved

Table 178: TAI Global Configuration Register 0 (Continued)
Page 12, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
3	TimeIncDecEn	SC	0x0	Retain	Time Increment Decrement Enable This is used to adjust the PTP Global Time counter value with respect to the phase offset computed by the PTP firmware using the PTP control messages like Sync, PDelayReq, PDelayResp etc. The assumption here is that the software maintains the 64-bit seconds field of the PTP time of day and hardware maintains the 32-bit field (in PTP clock increments) in PTP Global Time counter (PTP Global Time Register - Page 12, Registers 14 and 15). When 0x1, this bit enables the hardware logic to increment or decrement the PTP Global Time counter by the value specified by TimeIncDecAmt TAI Global Configuration Register 5, Page 12, Register 5). When 0x0, the hardware logic does not modify the PTP Global Time counter value. **NOTE:** This function is executed once by the hardware and upon execution this bit is cleared to 0x0.
2	MultiPTPSync-Mode	RWR	0x0	Retain	Multiple PTP devices sync mode. Used in cases when multiple PTP core enabled devices' PTP Global Time (PTP Global Time Register Byte 1&2 and PTP Global Time Register Byte 3&4 – Page 12, Register 14 and 15) need to be synchronized. When 0x1, the logic detects a low to high transition on the EventRequest and transfers the value in TrigGenAmt[31:0] (TAI Global Configuration Register 2 and TAI Global Configuration Register 3 - Page 12, Register 2 and 3) into the PTP Global Time Register[31:0]. The EventCapRegister[31:0] (Event Capture Register Byte 1&0 and Event Capture Register Byte 3&2 – Page 12, Register 10 and 11) is also updated at that instant. When 0x0, the EventReq and TrigGenResp interfaces operate normally. **NOTE:** When this bit is 0x1, the TrigGenReq and TrigMode is are inoperational and are expected to be set to a 0x0. **NOTE:** When this bit is 0x1, the TimeIncDecEn is non-operational and expected to be set to a 0x0.

Table 178: TAI Global Configuration Register 0 (Continued)
Page 12, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
1	TrigMode	RWR	0x0	Retain	Trigger Mode When 0x1, the hardware logic matches the PTP Global Timer (PTP Global Time Register - Page 12, Registers 14 and 15) with the TrigGenAmt (TAI Global Configuration Register - Page 12, Registers 2 and 3) and generates a pulse on the TrigGenResp output signal. The pulse width for this is specified by PulseWidth (TAI Global Configuration Register 5 - Page 12, Register 5). Note that the minimum pulse width that can be generated is one TSClkPer amount and the maximum pulse width is 15 times the TSClkPer. When 0x0, the hardware logic uses the value specified in the TrigGenAmt as the period for generating periodic pulses on TrigGenResp signal with a 50% duty cycle clock. Note that the minimum clock period that can be generated on the TrigGenResp output signal is 2 times the TSClkPer amount. For example if a 1 pps signal needs to be generated, the TrigMode is set to 0x0, if TSClkPer is set to 8 ns and TrigGenAmt is set to 125 x 10^6 cycles **NOTE:** When MultiPTPSyncMode bit is 0x1, this bit is non-operational.
0	TrigGenReq	RWR	0x0	Retain	Trigger Generation Request When 0x1, it validates the TrigGenAmt, TrigMode and TrigClkComp fields. This enables the hardware logic to generate either a trigger based on the TrigGenAmt or a clock based on the period specified in TrigGenAmt. **NOTE:** When MultiPTPSyncMode bit is 0x1, this bit is non-operational.

Table 179: TAI Global Configuration Register 1
Page 12, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TSClkPer	RWS	0x1F40	Retain	Time Stamping Clock Period in pico seconds. This field specifies the clock period for the time stamping clock supplied to the PTP hardware logic. This is the clock that is used by the hardware logic to update the PTP Global Time counter (PTP Global Time Register - Page 12, Registers 14 and 15). The default is calculated based on 125 MHz period clock.

Table 180: TAI Global Configuration Register 2
Page 12, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TrigGenAmt[15:0]	RWR	0x0000	Retain	Trigger Generation Amount [15:0] This field specifies the PTP Time Application Interface trigger generation time amount. When TrigMode is 0x1, the value specified in this field is compared with the PTP Global Timer (PTP Global Time Register - Page 12, Registers 14 and 15) and whenever it matches. A pulse is generated whose width is configured using PulseWidth (TAI Global Configuration Register 5 - Page 12, Register 5). When TrigMode is 0x0, the value is used as a clock period in TSClkPer increments to generate an output clock on the TrigGenResp signal. When TrigMode is 0x0, the TrigClkComp amount constantly gets accumulated internally and when this accumulated value exceeds the value specified in TSClkPer, a TSClkPer amount gets added to the clock output momentarily.

Table 181: TAI Global Configuration Register 3
Page 12, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TrigGenAmt[31:16]	RWR	0x0000	Retain	Trigger Generation Amount [31:16] This field specifies the PTP Time Application Interface trigger generation time amount. When TrigMode is 0x1, the value specified in this field is compared with the PTP Global Timer (PTP Global Time register - Page 12 Registers 14 and 15) and whenever it matches. A pulse is generated whose width is configured using PulseWidth (TAI Global Configuration Register 5 - Page 12, Register 5). When TrigMode is 0x0, the value is used as a clock period in TSClkPer increments to generate an output clock on the TrigGenResp signal. When TrigMode is 0x0, the TrigClkComp amount constantly gets accumulated internally and when this accumulated value exceeds the value specified in TSClkPer, a TSClkPer amount gets added to the clock output momentarily.

Table 182: TAI Global Configuration Register 4
Page 12, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TrigClkComp	RWR	0x0000	Retain	Trigger mode Clock Compensation Amount in pico seconds This field is valid only when TrigGenReq is 0x1 and TrigMode is set to 0x0. The field specifies the remainder amount for the clock that is being generated with a period specified by the TrigGenAmt. When TrigMode is 0x0, the TrigClkComp amount constantly gets accumulated internally and when this accumulated value exceeds the value specified in TSClkPer, a TSClkPer amount gets added to the clock output momentarily.

Table 183: TAI Global Configuration Register 5
Page 12, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	PulseWidth	RWS	0xF	Retain	Clock high pulse width in units of TSClkPer. This specifies the pulse width of the clock that gets generated on the TrigGenResp when TrigMode is 0x1 in units defined by TSClkPer. **NOTE:** When configured to a 0x0, the results are un-deterministic. Thus it is expected that this field be never programmed to a 0x0.
11	TimeIncDecOp	RWR	0	Retain	Time increment decrement operation. When 0x0, TimeIncDecAmt is considered as an increment amount that needs to be added to the PTP Global Time Counter when TimeIncDecEn is 0x1. When 0x1, TimeIncDecAmt is considered as a decrement amount that needs to be subtracted from the PTP Global Time Counter when TimeIncDecEn is 0x1. All updates are completed within the same cycle of TimeIncDecEn changing state from 0x0 to 0x1.
10:0	TimeIncDecAmt	RWR	0x000	Retain	Time Increment Decrement amount. This field is valid only when TimeIncDecEn is 0x1. This field specifies the number of units of PTP Global Time that need to be incremented or decremented based upon TimeIncDecOp. This is used for adjusting the PTP Global Time counter value by a certain amount.

Table 184: TAI Global Configuration Register 6
Page 12, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	RES			Reserved.
8:0	SoCClkPer	RWS			System on a chip Clock Period. This specifies the clock period for the clock that gets generated from the PTP block to the rest of the SoC. The period is specified in TSClkPer increments. For example, if the TSClkPer is 8 ns, and the SoC clock needs to be toggling every 3.125 us period, then SoCClkPer needs to be programmed to 0x186 and SoCClkComp needs to be programmed to 0x1388. For 100 MHz: 3125 ns / 10 ns = 312.5 TSClkPer cycles Decimal 312 in hexadecimal is 0x138 and 0.5 x 10000 ps = 0x1388 ps. For 125 MHz: 3125 ns / 8 ns = 390.625 TSClkPer cycles Decimal 390 in hexadecimal is 0x186 and 0.625 x 8000 ps = 0x1388 ps. For 200 MHz: 3125 ns / 5 ns = 625 TSClkPer cycles Decimal 625 in hexadecimal is 0x271 and 0.0 x 5000 ps = 0x0000 ps.

Table 185: TAI Global Configuration Register 7
Page 12, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	SoCClkComp	RWS			System on a Chip Clock Compensation Amount in pico seconds. The field specifies the remainder amount for when the clock is being generated with a period specified by the SoCClkPer. The hardware logic keeps track of the remainder for every clock tick generation and compensates for it.

Table 186: TAI Global Configuration Register 8
Page 12, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TrigGenInt	RWR	0x0	Retain	Trigger generate mode Interrupt. The TrigGenInt bit gets set by the TAI block when the TrigGenIntEn is 0x1 and when the hardware logic captures a trigger on the TrigGenResp signal. This interrupt gets tied to the PHY interrupt pin.
14:0	Reserved	RES	0x0000	Retain	Reserved

Table 187: TAI Global Configuration Register 9
Page 12, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15	EventInt	RWR	0x0	Retain	Event Capture Interrupt. This bit gets set by the TAI block when the EventCapIntEn is 0x1 and when the hardware logic captures an Event in the EventCapRegister. This interrupt gets tied to the PHY interrupt pin.
14:10	Reserved	RES	0x00	Retain	Reserved
9	EventCapErr	RWR	0x0	Retain	Event Capture Error. This bit gets set by the hardware logic when an event has been observed on the EventReq signal but the Event-CapValid is already set to a 0x1. This condition could hap-pen if the Events are being observed on the EventReq signal faster than the local CPU reading the captured event related counter values.
8	EventCapValid	RWR	0x0	Retain	Event Capture Valid. This bit when 0x1 validates the EventCapRegister.
7:0	EventCapCtr	RES	0x00	Retain	Event Capture Counter. This field is incremented by TAI block when EventCtrStart is set to 0x1. This field is incremented whenever an event (a low to high transition) has been registered on the Even-tReq signal. Note that there is no special logic provided to detect this counter wrap arounds.

Table 188: Event Capture Register Byte 1 & 0
Page 12, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	EventCapRegis-ter Byte 1	RWR	0x00000000	Retain	Event Capture Register Byte 1 These bits contain bits 15:8 of the PTP Global Timer that capture the value of the Event Capture logic when an event (a low to high transition) has been registered by the TAI block on the EventReq signal. If the EventCapOv is 0x1, then this register indicates the time captured for the last event in the hardware. When EventCapErr is 0x1, the contents in this register are invalid. Note that the maximum jitter for the EventCapRegister time amount with respect to the rising edge of the EventReq input signal is one TSClkPer amount. Note that the minimum EventReq input signal high or low width has to be equal to or greater than 1.5 times the TSClkPer amount. **NOTE:** In order for hardware to capture the Event request on the EventReq input signal, the minimum gap between two consecutive events has to be 150 ns plus 5 times TSClkPer amount.

Table 188: Event Capture Register Byte 1 & 0 (Continued)
Page 12, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	EventCapRegis-ter Byte 0	RWR	0x00000000	Retain	Event Capture Register Byte 0 These bits contain bits 7:0 of the PTP Global Timer that capture the value of the Event Capture logic when an event (a low to high transition) has been registered by the TAI block on the EventReq signal. If the EventCapOv is 0x1, then this register indicates the time captured for the last event in the hardware. When EventCapErr is 0x1, the contents in this register are invalid. **NOTE:** The maximum jitter for the EventCapRegister time amount with respect to the rising edge of the EventReq input signal is one TSClkPer amount. Note that the minimum EventReq input signal high or low width has to be equal to or greater than 1.5 times the TSClkPer amount. Note that in order for hardware to capture the Event request on the EventReq input signal, the minimum gap between two consecutive events has to be 150 ns plus 5 times TSClkPer amount.

Table 189: Event Capture Register Byte 3 & 2
Page 12, Register 11

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	EventCap Register Byte 3	RWR	0x00000000	Retain	Event Capture Register Byte 3 These bits contain bits 31:24 of the PTP Global Timer that capture the value of the Event Capture logic when an event (a low to high transition) has been registered by the TAI block on the EventReq signal. If the EventCapOv is 0x1, then this register indicates the time captured for the last event in the hardware. When EventCapErr is 0x1, the contents in this register are invalid. **NOTE:** The maximum jitter for the EventCapRegister time amount with respect to the rising edge of the EventReq input signal is one TSClkPer amount. **NOTE:** The minimum EventReq input signal high or low width has to be equal to or greater than 1.5 times the TSClkPer amount. **NOTE:** In order for hardware to capture the Event request on the EventReq input signal, the minimum gap between two consecutive events has to be 150 ns plus 5 times TSClkPer amount.

Table 189: Event Capture Register Byte 3 & 2 (Continued)
Page 12, Register 11

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	EventCapRegister Byte 2	RWR	0x00000000	Retain	Event Capture Register Byte 2 These bits contain bits 23:16 of the PTP Global Timer that capture the value of the Event Capture logic when an event (a low to high transition) has been registered by the TAI block on the EventReq signal. If the EventCapOv is 0x1, then this register indicates the time captured for the last event in the hardware. When EventCapErr is 0x1, the contents in this register are invalid. Note that the maximum jitter for the EventCapRegister time amount with respect to the rising edge of the EventReq input signal is one TSClkPer amount. **NOTE:** The minimum EventReq input signal high or low width has to be equal to or greater than 1.5 times the TSClkPer amount. **NOTE:** In order for hardware to capture the Event request on the EventReq input signal, the minimum gap between two consecutive events has to be 150 ns plus 5 times TSClkPer amount.

Table 190: TAI Global Configuration Register 12
Page 12, Register 12

Bits	Field	Mode	HW Rst	SW Rst	Description
31:0	Reserved	RES	0x00000000	Retain	Reserved

Table 191: TAI Global Configuration Register 13
Page 12, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
31:0	Reserved	RES	0x00000000	Retain	Reserved

Note

The PTP Global Time Register Bytes 1 & 0 Register (Page 12, Register 14) and the PTP Global Time Register Bytes 3 & 2 Register (Page 12, Register 15) must be read by using the ReadPlus Command. See Section 2.28.4 for details.

Table 192: PTP Global Time Register Bytes 1 & 0
Page 12, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	PTPGlobal Time Byte 1	RWR	0x00000000	Retain	Precise Time Protocol Global Timer Byte 1. These bits contain bits 15:8 of the global timer value that is running off of the free running PHY clock. Based on PTP protocol time of day computations, this field can be either incremented or decremented using the TimeIncDecAmt (TAI Global Config Register 5 - Page 12, Register 5) and by turning on TimeIncDecEn (TAI Global Config Register 0 - Page 12, Register 0) to 0x1 and by selecting an increment or a decrement operation using TimeIncDecOp (TAI Global Config Register 5 - Page 12, Register 5). **NOTE:** This register is updated in the same cycle as when TimeIncDecEn goes high. **NOTE:** This register gets updated with the value specified in TrigGenAmt (TAI Global Config Register 2 and 3 - Page 12, Register 2 and 3) when MultiPTPSyncMode (TAI Global Config Register 0 - Page 12, Register 0)is 0x1 and a low to high transition is detected on the EventReq signal. This counter wraps around in hardware.

Table 192: PTP Global Time Register Bytes 1 & 0
Page 12, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	PTPGlobal Time Byte 0	RWR	0x00000000	Retain	Precise Time Protocol Global Timer Byte 0. These bits contain bits 7:0 of the global timer value that is running off of the free running PHY clock. Based on PTP protocol time of day computations, this field can be either incremented or decremented using the TimeIncDecAmt (TAI Global Config Register 5 - Page 12, Register 5) and by turning on TimeIncDecEn (TAI Global Config Register 0 - Page 12, Register 0) to 0x1 and by selecting an increment or a decrement operation using TimeIncDecOp (TAI Global Config Register 5 - Page 12, Register 5). **NOTE:** This register is updated in the same cycle as when TimeIncDecEn goes high. **NOTE:** This register gets updated with the value specified in TrigGenAmt (TAI Global Config Register 2 and 3 - Page 12, Register 2 and 3) when MultiPTPSyncMode (TAI Global Config Register 0 - Page 12, Register 0)is 0x1 and a low to high transition is detected on the EventReq signal. This counter wraps around in hardware.

Table 193: PTP Global Time Register Bytes 3 & 2
Page 12, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	PTPGlobal Time Byte 3	RWR	0x00000000	Retain	Precise Time Protocol Global Timer Byte 3. These bits contain bits 31:24 of the global timer value that is running off of the free running PHY clock. Based on PTP protocol time of day computations, this field can be either incremented or decremented using the TimeIncDecAmt (TAI Global Config Register 5 - Page 12, Register 5) and by turning on TimeIncDecEn (TAI Global Config Register 0 - Page 12, Register 0) to 0x1 and by selecting an increment or a decrement operation using TimeIncDecOp (TAI Global Config Register 5 - Page 12, Register 5). **NOTE:** This register is updated in the same cycle as when TimeIncDecEn goes high. **NOTE:** This register gets updated with the value specified in TrigGenAmt (TAI Global Config Register 2 and 3 - Page 12, Register 2 and 3) when MultiPTPSyncMode (TAI Global Config Register 0 - Page 12, Register 0)is 0x1 and a low to high transition is detected on the EventReq signal. This counter wraps around in hardware.
7:0	PTPGlobal Time Byte 2	RWR	0x00000000	Retain	Precise Time Protocol Global Timer Byte 2. These bits contain bits 23:16 of the global timer value that is running off of the free running PHY clock. Based on PTP protocol time of day computations, this field can be either incremented or decremented using the TimeIncDecAmt (TAI Global Config Register 5 - Page 12, Register 5) and by turning on TimeIncDecEn (TAI Global Config Register 0 - Page 12, Register 0) to 0x1 and by selecting an increment or a decrement operation using TimeIncDecOp (TAI Global Config Register 5 - Page 12, Register 5). **NOTE:** This register is updated in the same cycle as when TimeIncDecEn goes high. **NOTE:** This register gets updated with the value specified in TrigGenAmt (TAI Global Config Register 2 and 3 - Page 12, Register 2 and 3) when MultiPTPSyncMode (TAI Global Config Register 0 - Page 12, Register 0)is 0x1 and a low to high transition is detected on the EventReq signal. This counter wraps around in hardware.

Table 194: PTP Global Configuration Register 0
Page 14, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPEType	RWR	0x88F7	0x88F7	Precise Time Protocol Ether Type. All PTP frames are recognized using a combination of a specific EtherType and MessageID values (part of the PTP Common Header). The actual numeric value is not yet defined in the IEEE802.1AS standard. It is possible that all IEEE1588 time sync frames and IEEE802.11 wireless LAN location estimation time sync messages follow the same EtherType but varying Ether subtypes (aka messageID). The MsgIDTSEn (specified below) qualifies the types of frames that the hardware needs to time stamp.

Table 195: PTP Global Configuration Register 1
Page 14, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MsdIDTSEn	RWR	0x0000	Retain	Message Identifier Time Stamp Enable. MessageID is part of the PTP common header for time sync frames. There are PTP frames which need to be time stamped by hardware and some that do not need to be. This field identifies the PTP frame types that need to be time stamped by the hardware. Some of the PTP frames may need to be time stamped only when they enter the device and not when they are either being sent to or received from the CPU (assuming an external CPU in the system). The MsdIDTSEn refers to the bit mask enables where each bit indicates whether the vectorized[1] MessageID value needs to be time stamped or not. 0x0 = Indicates to hardware to NOT time stamp both incoming and/or outgoing PTP frames which match the MessageID. 0x1= Indicates to hardware to time stamp both incoming and/or outgoing PTP frames which match the MessageID. For example, if MessageID field (in the PTP common header) with a value of 0x4 ought to be time stamped in hardware then MsdIDTSEn[4] should be configured to a 0x1. Then for the incoming PTP frame with the MessageID field of 0x4 one of the two arrival counters get updated (PTPArr0Time or PTPArr1Time. The exact time counter is identified by TSArrPtr field below). For an outgoing PTP frame with the MessageID field of 0x4 PTPDepTime counter gets updated for an outgoing frame with the MessageId field from the PTPCommon header matching 0x4.

1. The term vectorized refers to converting the hexadecimal MessageID field into a 16-bit binary number.

Table 196: PTP Global Configuration Register 2
Page 14, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TSArrPtr	RWR	0x0000	Retain	Time Stamp Arrival Time Counter Pointer. If the incoming PTP frame needs to be time stamped (based on MsdIDTSEn), this field determines whether the hardware logic should use PTPArr0Time or PTPArr1Time for storing the arriving frame's time stamp information. Each bit in this field corresponds to the sixteen combinations of the vectorized[1] MessageID field. For example if TSArrPtr[2] is set to a 0x1 it indicates to the hardware that if MsdIDTSEn[2] is set then use PTPArr1Time counter for storing the incoming PTP frame's time stamp. On the contrary if TSArrPtr[2] is set to a 0x0 that indicates to the hardware that if MsdIDTSEn[2] is set then use PTPArr0Time counter for storing the incoming PTP frame's time stamp.

1. The term vectorized refers to converting the hexadecimal MessageID field into a 16-bit binary number.

Table 197: PTP Global Configuration Register 3
Page 14, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RES	0x0000	Retain	Reserved.
0	TSAtSFD	RWS	0x1	Retain	Time Stamp At Start of Frame Delimiter. 0x1 = Specifies to the PTP hardware that the incoming frames need to be time stamped at SFD of the Ethernet Frame. 0x0 = Specifies to the PTP hardware that the incoming frames can be time stamped at a fixed reference point which may not be at SFD of the Ethernet frame. In our current implementation, this is at the beginning of the Ethernet DA.

Table 198: PTP Global Status Register
Page 14, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RES	0x000	0x000	Reserved.
3:0	PTPInt	RWR	0x0	Retain	Precise Time Protocol Interrupt The PTP Interrupt bit gets set for a given port when an incoming PTP frame is time stamped and PTPArrIntEn for that port is set to 0x1. Similarly PTP Interrupt bit gets set for a given port when an outgoing PTP frame is time stamped and PTPDepIntEn for that port is set to 0x1. The hardware logic sets this per port bit based on above criteria and gets cleared upon software reading and clearing the corresponding time counter valid bits that are valid for that port.

Table 199: ReadPlus Command Register
Page 14, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15	ReadPlusEnable	R/W	0	Retain	ReadPlus Enable 1 = Enable 0 = Disable
14:12	Reserved	RES	0	Retain	Reserved.
11:8	PTPReg	R/W	0	Retain	PTP Registers 0xE = Page 12 (TAI Registers, Event Capture Registers, PTP Global Time Registers)
7:5	Reserved	RES	0	Retain	Reserved.
4:0	PTPAddr	R/W	0	Retain	PTP Address This is the starting address of the PTP Registers to be read.

Table 200: ReadPlus Data Register
Page 14, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	ReadPlusData	R/W	0	0	ReadPlus Data This register is used to read out the ReadPlus Data. To read 32-bit wide PTP Registers, read from this register back-to-back.

Table 201: WOL Control
Page 17, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SRAM Packet Match Enable	R/W	0x0	Retain	Allows for matching received packets with SRAM packets to assert WOL detection logic. 1 = Enable SRAM packet matching for WOL detection 0 = Disable SRAM packet matching for WOL detection
14	Magic Packet Match Enable	R/W	0x0	Retain	Allows matching received packets with a Magic Packet (packet containing 6 bytes of FF followed by 16 instances of the destination address) to assert the WOL detection logic 1 = Enable Magic Packet matching for WOL detection 0 = Disable Magic Packet matching for WOL detection
13	Link Up Enable	R/W	0x0	Retain	Allows link up event to assert the WOL detection logic 1 = Enable link up event for WOL detection 0 = Disable link up event for WOL detection
12	Clear WOL Status	R/W, SC	0x0	Retain	1 = Clear status in 17_17 0 = Retain status in 17_17
11:9	Reserved	R/W	0x0	Retain	
8	10BT Low Power Mode Select	R/W	0x0	Retain	1 = 10BT Low Power mode enabled. The transmitter is powered down in between transmitted link pulses. 10BT packets cannot be transmitted when this mode is enabled. 0 = Normal Operation This feature may be enabled when WOL event detection is enabled during 10BT operation for lower power.
7	SRAM Packet Match Packet 7 Enable	R/W	0x0	Retain	1 = Enable received packet matching to SRAM's Packet 7 0 = Disable received packet matching to SRAM's Packet 7
6	SRAM Packet Match Packet 6 Enable	R/W	0x0	Retain	1 = Enable received packet matching to SRAM's Packet 6 0 = Disable received packet matching to SRAM's Packet 6
5	SRAM Packet Match Packet 5 Enable	R/W	0x0	Retain	1 = Enable received packet matching to SRAM's Packet 5 0 = Disable received packet matching to SRAM's Packet 5

Table 201: WOL Control
Page 17, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
4	SRAM Packet Match Packet 4 Enable	R/W	0x0	Retain	1 = Enable received packet matching to SRAM's Packet 4 0 = Disable received packet matching to SRAM's Packet 4
3	SRAM Packet Match Packet 3 Enable	R/W	0x0	Retain	1 = Enable received packet matching to SRAM's Packet 3 0 = Disable received packet matching to SRAM's Packet 3
2	SRAM Packet Match Packet 2 Enable	R/W	0x0	Retain	1 = Enable received packet matching to SRAM's Packet 2 0 = Disable received packet matching to SRAM's Packet 2
1	SRAM Packet Match Packet 1 Enable	R/W	0x0	Retain	1 = Enable received packet matching to SRAM's Packet 1 0 = Disable received packet matching to SRAM's Packet 1
0	SRAM Packet Match Packet 0 Enable	R/W	0x0	Retain	1 = Enable received packet matching to SRAM's Packet 0 0 = Disable received packet matching to SRAM's Packet 0

Table 202: WOL Status
Page 17, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SRAM Packet Match Detected	RO,LH	0x0	0x0	1 = At least 1 SRAM packet matched a received packet 0 = No SRAM packets have matched with a received packet
14	Magic Packet Match Detected	RO,LH	0x0	0x0	1 = At least 1 received packet contained the Magic Packet data 0 = No received packets contained the Magic Packet data
13	Link Change Detected	RO,LH	0x0	0x0	1 = Link status changed from down to up 0 = Link status did not change from down to up
12:8	Reserved	R/W	0x00	Retain	Reserved.
7	SRAM Packet Match With Packet 7 Detected	RO,LH	0x0	0x0	1 = At least 1 received packet matched SRAM's Packet 7 0 = No received packets matched SRAM's Packet 7
6	SRAM Packet Match With Packet 6 Detected	RO,LH	0x0	0x0	1 = At least 1 received packet matched SRAM's Packet 6 0 = No received packets matched SRAM's Packet 6

Table 202: WOL Status (Continued)
Page 17, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
5	SRAM Packet Match With Packet 5 Detected	RO,LH	0x0	0x0	1 = At least 1 received packet matched SRAM's Packet 5 0 = No received packets matched SRAM's Packet 5
4	SRAM Packet Match With Packet 4 Detected	RO,LH	0x0	0x0	1 = At least 1 received packet matched SRAM's Packet 4 0 = No received packets matched SRAM's Packet 4
3	SRAM Packet Match With Packet 3 Detected	RO,LH	0x0	0x0	1 = At least 1 received packet matched SRAM's Packet 3 0 = No received packets matched SRAM's Packet 3
2	SRAM Packet Match With Packet 2 Detected	RO,LH	0x0	0x0	1 = At least 1 received packet matched SRAM's Packet 2 0 = No received packets matched SRAM's Packet 2
1	SRAM Packet Match With Packet 1 Detected	RO,LH	0x0	0x0	1 = At least 1 received packet matched SRAM's Packet 1 0 = No received packets matched SRAM's Packet 1
0	SRAM Packet Match With Packet 0 Detected	RO,LH	0x0	0x0	1 = At least 1 received packet matched SRAM's Packet 0 0 = No received packets matched SRAM's Packet 0

Table 203: SRAM Packets 7/6 Length
Page 17, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	R/W	0x0	Retain	Reserved.
13:7	SRAM Packet 7 Length	RW	111_1111	Retain	Number of bytes (including byte 0) that a received packet must have in order to match Packet 7. Note that this matching requirement is in addition to matching the bytes that need to be matched.
6:0	SRAM Packet 6 Length	RW	111_1111	Retain	Number of bytes (including byte 0) that a received packet must have in order to match Packet 6. Note that this matching requirement is in addition to matching the bytes that need to be matched.

Table 204: SRAM Packets 5/4 Length
Page 17, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	R/W	0x0	Retain	Reserved.
13:7	SRAM Packet 5 Length	RW	111_1111	Retain	Number of bytes (including byte 0) that a received packet must have in order to match Packet 5. Note that this matching requirement is in addition to matching the bytes that need to be matched.
6:0	SRAM Packet 4 Length	RW	111_1111	Retain	Number of bytes (including byte 0) that a received packet must have in order to match Packet 4. Note that this matching requirement is in addition to matching the bytes that need to be matched.

Table 205: SRAM Packets 3/2 Length
Page 17, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	R/W	0x0	Retain	Reserved.
13:7	SRAM Packet 3 Length	RW	111_1111	Retain	Number of bytes (including byte 0) that a received packet must have in order to match Packet 3. Note that this matching requirement is in addition to matching the bytes that need to be matched.
6:0	SRAM Packet 2 Length	RW	111_1111	Retain	Number of bytes (including byte 0) that a received packet must have in order to match Packet 2. Note that this matching requirement is in addition to matching the bytes that need to be matched.

Table 206: SRAM Packets 1/0 Length
Page 17, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	R/W	0x0	Retain	Reserved.
13:7	SRAM Packet 1 Length	RW	111_1111	Retain	Number of bytes (including byte 0) that a received packet must have in order to match Packet 1. Note that this matching requirement is in addition to matching the bytes that need to be matched.

Table 206: SRAM Packets 1/0 Length (Continued)
Page 17, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
6:0	SRAM Packet 0 Length	RW	111_1111	Retain	Number of bytes (including byte 0) that a received packet must have in order to match Packet 0. Note that this matching requirement is in addition to matching the bytes that need to be matched.

Table 207: Magic Packet Destination Address Word 2
Page 17, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Destination Address {7:0,15:8}	R/W	0x0000	Retain	This data is the upper 47:32 bits of the destination address that must be seen repeated 16 times in a received packet in order for it to be a Magic Packet. This must be programmed since the PHY has no other way of knowing what the Destination Address is.

Table 208: Magic Packet Destination Address Word 1
Page 17, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Destination Address {23:16,31:24}	R/W	0x0000	Retain	This data is the middle 31:16 bits of the destination address that must be seen repeated 16 times in a received packet in order for it to be a Magic Packet. This must be programmed since the PHY has no other way of knowing what the Destination Address is.

Table 209: Magic Packet Destination Address Word 0
Page 17, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Destination Address {39:32,47:40}	R/W	0x0000	Retain	This data is the lower 15:0 bits of the destination address that must be seen repeated 16 times in a received packet in order for it to be a Magic Packet. This must be programmed since the PHY has no other way of knowing what the Destination Address is.

Table 210: SRAM Byte Address Control
Page 17, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	
11	Read Enable	R/W	0x0	Retain	Enables reading the mask byte bit and data stored at SRAM Byte Address (indicated by 26_17.9:7) and SRAM Row Address (indicated by 26_17.6:0) and placed in 28_17.8:0. This completes DMA capability (writing is already advertised). 1 = read SRAM mask byte bit and data 0 = do not read SRAM mask byte bit and data Note that this bit must be set to 1 only after 26_17.9:0 have been written with the address of data to be read from the SRAM.
10	Write Enable	R/W, SC	0x0	Retain	When a 1 is written to this bit, Byte Data and Mask Byte Data are written to the location in the SRAM addressed by 26_17.9:0.
9:7	SRAM Byte Address	R/W	0x0	Retain	Indicates the byte address for a given SRAM row that should store Byte Data (27_17.7:0) from 000 (bits 7:0) up to 111 (bits 63:56). Mask Byte Data (27_17.8) is stored in the most significant byte location in the bit corresponding to the Packet number (bit 64 for Packet 0's mask bit up to bit 71 for Packet 7's mask bit). Note that this must be programmed before 26_17.10 is set to 1.
6:0	SRAM Row Address	R/W	0x00	Retain	Indicates the Row number of the 128 row X 72 bit SRAM used for the SRAM Packet Matching where Byte Data (27_17.7:0) is to be stored. Note that this must be programmed before 26_17.10 is set to 1.

Table 211: SRAM Byte Data Control
Page 17, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0x00	Retain	Reserved.
8	Mask Byte Data	R/W	0x0	Retain	Programmed with Byte Data (27_17.7:0). Indicates if Byte Data should be compared or not in the SRAM packet matching. 1 = compare Byte Data with the corresponding byte of a received packet (do not mask the comparison) 0 = do not compare Byte Data with the corresponding byte of a received packet (mask the comparison) Note that this must be programmed before 26_17.10 is set to 1.
7:0	Byte Data	R/W	0x00	Retain	Data to be stored in the SRAM at the address indicated by 26_17.9:0. Note that this must be programmed before 26_17.10 is set to 1.

Table 212: SRAM Read Control
Page 17, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0x00	Retain	Reserved.
8:0	SRAM Read Data	R/W	0x000	Retain	WOL SRAM DMA Read Data where bit 8 is the byte mask bit and 7:0 are the byte data.

Table 213: EEE Buffer Control Register 1
Page 18, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	IPG Length	R/W	0xC	Retain	Minimum Number of IPGs in bytes
7:1	Reserved	R/W	0x00	Retain	Reserved.
0	EEE Buffer enable	R/W	0x0	Retain	1 = Enable EEE Buffer, and EEE Buffer will initiate LPI_IDLE based on TX traffic 0 = Disable EEE Buffer, EEE buffer pass LPI_IDLE in both directions

Table 214: EEE Buffer Control Register 2
Page 18, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Fast_exit_time	R/W	0x11	Retain	LPI exit timer when port speed is 1000 Mbps default is 17 us. Each increment in the register corresponds to 1 us.
7:0	Slow_exit_time	R/W	0x1E	Retain	LPI exit timer when port speed is 100 Mbps default is 30 us. Each increment in the register corresponds to 1 us.

Table 215: EEE Buffer Control Register 3
Page 18, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Fast_enter_time	R/W	0x11	Retain	LPI enter timer when port speed is 1000 Mbps default is 17 us. Each increment in the register corresponds to 1 us.
7:0	Slow_enter_time	R/W	0x1E	Retain	LPI enter timer when port speed is 100 Mbps default is 30 us. Each increment in the register corresponds to 1 us.

Table 216: Packet Generation
Page 18, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7:5	Enable Packet Generator	R/W, SC	0x0	Retain	000 = Normal Operation 010 = Generate Packets on Copper Interface 100 = Generate Packets on SGMII Interface 101 = Reserved 110 = Generate Packets on RGMII Interface 111 = Reserved else = Reserved

Table 216: Packet Generation (Continued)
Page 18, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Packet Generator Transmit Trigger	R/W	0x0	Retain	This bit is only valid when all of the following are true: bit 7:5 are not equal to 000 bit3 =1 bit15:8 is not equal to all 0s A read of this bit gives the following: 1: Packet generator transmit done 0: Packet generator is transmitting data When this bit is 1 a write of 0 will trigger the packet generator to transmit again. When this bit is 0 a write of 0 or 1 will have no effect.
3	Packet Generator Enable Self Clear Control	R/W	0x0	Retain	0 = Bit 7:5 will self clear after all packets are sent 1 = Bit 7:5 will stay at the current value after all packets are sent
2	Payload of packet to transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,...
1	Length of packet to transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored packet	R/W	0x0	Retain	1 = Tx packets with CRC errors & Symbol Error 0 = No error

Table 217: CRC Counters
Page 18, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Count	RO	0x00	Retain	0x00 = No packets received 0xFF = 256 packets received (max count). Bit 18_18.2:0. must not be all 0 in order for these bits to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00 = No CRC errors detected in the packets received 0xFF = 256 CRC errors detected in the packets received (max count) Bit 18_18.2:0. must not be all 0 in order for these bits to be valid.

Table 218: Checker Control
Page 18, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x000	Retain	Set to 0s
4	CRC Counter Reset	R/W, SC	0x0	Retain	1 = Reset This bit will self-clear after writing 1.
3	Reserved	R/W	0x0	Retain	Reserved.
2:0	Enable CRC Checker	R/W	0x0	Retain	000 = Disable/reset CRC checker 010 = Check data from Copper Interface 100 = Check data from SGMII Interface 101 = Reserved 110 = Check data from RGMII Interface 111 = Reserved else = Reserved

Table 219: Packet Generation
Page 18, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Reserved.
7:0	IPG Length	R/W	0xC	Retain	The number in bit 7:0+1 is the number of bytes for IPG

Table 220: General Control Register 1
Page 18, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	SC	Mode Software Reset. Affects page 6 and 18 Writing a 1 to this bit causes the main PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14:13	Reserved	R/W	0x0	Retain	Set to 0s.
12:10	Reserved	R/W	0x0	Retain	Reserved for future use.
9:7	Reserved	R/W	0x4	Retain	Set to 100
6	Auto-Media Detect (AMD) 100BASE-FX/ 1000BASE-X	R/W	0x0	Retain	This bit selects the fiber auto-media modes as follows: 1 = mode 011 is AMD between copper and 100BASE-FX 0 = mode 111 is AMD between copper and 1000BASE-X
5:4	Auto Media Detect Preferred Media	R/W	0x0	Retain	00 = Link on first media 01 = Copper Preferred 10 = Fiber Preferred 11 = Reserved
3	Reserved	R/W	0x0	Update	Set to 0
2:0	MODE[2:0]	R/W	See Descr.	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 1512 device comes up in MODE[2:0] =0x7 on hardware reset. 000 = RGMII (System mode) to Copper 001 = SGMII (System mode) to Copper 010 = RGMII (System mode) to 1000BASE-X 011 = RGMII (System mode) to 100BASE-FX 100 = RGMII (System mode) to SGMII (Media mode) 101 = Reserved 110 = RGMII (System mode) to Auto Media Detect Copper/SGMII (Media mode) 111 = RGMII (System mode) to Auto Media Detect Copper/1000BASE-X/100BASE-FX (see 20_18.6)

Table 221: Link Disconnect count
Page 18, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Set to 0s
7:0	Link Disconnect	RO, SC	0x00	Retain	This counter counts the number of times link status changed from up to down. The counter will not roll over and will clear on read.

Table 222: SERDES RX_ER Byte Capture
Page 18, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Capture Data Valid	RO	0x0	0x0	1 = Bits 14:0 Valid 0 = Bits 14:0 Invalid
14	Reserved	RO	0x0	0x0	Reserved.
13:12	Byte Number	RO	0x0	0x0	00 = 4 bytes before RX_ER asserted 01 = 3 bytes before RX_ER asserted 10 = 2 bytes before RX_ER asserted 11 = 1 byte before RX_ER asserted The byte number increments after every read when register 26_18.15 is set to 1.
11:10	Reserved	RO	0x0	0x0	Reserved.
9	RX_ER	RO	0x0	0x0	RX Error. Normally this bit will be low since the capture is triggered by RX_ER being high. However it is possible to see RX_ER high when the capture is re-enabled after reading the fourth byte and there happens to be a long sequence of RX_ER when the capture restarts.
8	RX_DV	RO	0x0	0x0	RX Data Valid
7:0	RXD[7:0]	RO	0x00	0x00	RX Data

3.2 PHY XMDIO Register Description

88E1510/88E1518/88E1512/88E1514 supports Clause 22 MMD extension registers to access Clause 45 MMD registers, using register 13 and 14, as specified in the IEEE Annex 22D.

Table 223: XMDIO MMD Control Register
Device 0 Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0	0	11 = Data, post increments on writes only 10 =Data, post increment on reads and writes 01= Data, no post increment 00 = Address
13:5	Reserved	RO	0	0	Reserved.
4:0	DEVAD	RO	0	0	Device Address.

Table 224: XMDIO MMD Address Data Register
Device 0 Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0	0	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register

For example, to write single Clause 45 register, perform the following accesses:

1. To Register 13, write 00 (address) to bit 15:14 and the device address value to bit 4:0;
2. To Register 14, write the address value;
3. To Register 13, write 01 (Data, no post increment) to bit 15:14 and the same device address value to bit 4:0;
4. To Register 14, write the content of the MMD's selected register.

Step 1 and Step 2 can be skipped if the MMD's address register was previously configured.

For example, to read single Clause 45 register, perform the following accesses:

1. To Register 13, write 00 (address) to bit 15:14 and the device address value to bit 4:0;
2. To Register 14, write the address value;
3. To Register 13, write 01 (Data, no post increment) to bit 15:14 and the same device address value to bit 4:0;
4. From Register 14, read the content of the MMD's selected register.

Step 1 and Step 2 can be skipped if the MMD's address register was previously configured.

Table 225: 88E1510/88E1518/88E1512 Register Map

Register Name	Register Address	Table and Page
PCS Control 1 Register	Device 3 Register 0	Table 226 on page 227
PCS Status 1 Register	Device 3 Register 1	Table 227 on page 227
PCS EEE Capability Register	Device 3 Register 20	Table 228 on page 228
PCS EEE Wake Error Counter	Device 3 Register 22	Table 229 on page 228
EEE Advertisement Register	Device 7 Register 60	Table 230 on page 228
EEE Link Partner Advertisement Register	Device 7 Register 61	Table 231 on page 229

Table 226: PCS Control 1 Register
Device 3 Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	R	0	Retain	Set to 0s.
10	Clock Stoppable	R/W	0	Retain	1 = Clock stoppable during LPI 0 = Clock not stoppable
9:0	Reserved	R	0	Retain	Set to 0s.

Table 227: PCS Status 1 Register
Device 3 Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R	0	Retain	Set to 0s.
11	Tx LP idle received	RO/LH	0	Retain	1 = Tx PCS has received LP idle 0 = LP Idle not received
10	Rx LP idle received	RO/LH	0	Retain	1 = Rx PCS has received LP idle 0 = LP Idle not received
9	Tx LP idle indication	RO	0	Retain	1 = Tx PCS is currently receiving LP idle 0 = PCS is not currently receiving LP idle
8	Rx LP idle indication	RO	0	Retain	1 = Rx PCS is currently receiving LP idle 0 = PCS is not currently receiving LP idle
7:3	Reserved	R	0	Retain	Set to 0s.
2	PCS receive link status	R	0	Retain	1 = PCS receive link up 0 = PCS receive link down
1	Low-power ability	R	0	Retain	1 = PCS supports low-power mode 0 = PCS does not support low-power mode
0	Reserved	R	0	Retain	Set to 0.

Table 228: PCS EEE Capability Register
Device 3 Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	R	0	Retain	Set to 0s.
6	10GBASE-KR EEE	R	0	Retain	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR
5	10GBASE-KX4 EEE	R	0	Retain	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4
4	1000BASE-KX EEE	R	0	Retain	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX
3	10GBASE-T EEE	R	0	Retain	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T
2	1000BASE-T EEE	R	1	Retain	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T
1	100BASE-TX EEE	R	1	Retain	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX
0	Reserved	R	0	Retain	Set to 0.

Table 229: PCS EEE Wake Error Counter
Device 3 Register 22

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	EEE Wake Error Counter	R, NR	0	Retain	This counter is incremented for each transition of lpi_wake_timer_done from FALSE to TRUE

Table 230: EEE Advertisement Register
Device 7 Register 60

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	R	0	Retain	Set to 0s.
6	10GBASE-KR EEE	R	0	Retain	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR
5	10GBASE-KX4 EEE	R	0	Retain	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4
4	1000BASE-KX EEE	R	0	Retain	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX
3	10GBASE-T EEE	R	0	Retain	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T

Table 230: EEE Advertisement Register (Continued)
Device 7 Register 60

Bits	Field	Mode	HW Rst	SW Rst	Description
2	1000BASE-T EEE	R/W	0	Retain	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect.
1	100BASE-TX EEE	R/W	0	Retain	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect.
0	Reserved	R	0	Retain	Set to 0.

Table 231: EEE Link Partner Advertisement Register
Device 7 Register 61

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	R	0	Retain	Set to 0s.
6	LP 10GBASE-KR EEE	R	0	Retain	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR
5	LP 10GBASE-KX4 EEE	R	0	Retain	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4
4	LP 1000BASE-KX	R	0	Retain	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX
3	LP 10GBASE-T EEE	R	0	Retain	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T
2	LP 1000BASE-T EEE	R	0	Retain	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T
1	LP 100BASE-TX EEE	R	0	Retain	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX
0	Reserved	R	0	Retain	Set to 0.

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDA}	Power Supply Voltage on AVDD18 with respect to VSS	-0.5		2.5	V
V_{DDAC}	Power Supply Voltage on AVDDC18 with respect to VSS	-0.5		2.5	V
V_{DDAR}	Power Supply Voltage on AVDD33 with respect to VSS	-0.5		3.6	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	-0.5		1.5	V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS	-0.5		3.6	V
V_{PIN}	Voltage applied to any digital input pin	-0.5		3.6V or VDDO + 0.7 whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[1]	°C

1. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (e.g weeks or longer) should be kept at 85 °C or lower.

4.2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDA}[1]	AVDD18 supply	For AVDD18	1.71	1.8	1.995	V
V_{DDAC}[1]	AVDDC18 supply	For AVDDC18	1.71	1.8	1.995	V
V_{DDAR}[1]	AVDD33 supply	For AVDD33	3.14	3.3	3.46	V
V_{DD}[1]	DVDD supply	For DVDD	0.95	1.0	1.05	V
V_{DDO}[1]	VDDO supply	For VDDO at 1.8V (88E1518/88E1512/ 88E1514)	1.71	1.8	1.995	V
		For VDDO at 2.5V	2.38	2.5	2.62	V
		For VDDO at 3.3V	3.14	3.3	3.46	V
RSET	Internal bias reference	Resistor connected to V_{SS}		4990 ± 1% Tolerance		Ω
T_A	Ambient operating temperature	Commercial Grade	0		70[2]	°C
		Industrial Grade	-40		+85	°C
T_J	Maximum junction temperature	Commercial Grade	0		125[3]	°C
		Industrial Grade	0		125	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.
2. Commercial operating temperatures are typically below 70 °C, e.g, 45 °C ~55 °C. The 70°C max is Marvell® specification limit
3. Refer to white paper on TJ Thermal Calculations for more information.

4.3 Package Thermal Information

4.3.1 Thermal Conditions for 88E1510/88E1518 48-pin, QFN Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient for the device 48-Pin, QFN package $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		35.2		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		30.5		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		29.3		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		28.4		°C/W
ψ_{JT}	Thermal characteristic parameter[a] - junction to top center of the device 48-Pin, QFN package $\psi_{JT} = (T_J - T_{top})/P$. P = Total power dissipation, T_{top}: Temperature on the top center of the package.	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.63		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		1.07		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		1.36		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		1.52		°C/W
θ_{JC}	Thermal resistance[1] - junction to case for the device 48-Pin, QFN package $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow		18.6		°C/W
θ_{JB}	Thermal resistance[1] - junction to board for the device 48-Pin, QFN package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		22.7		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

4.3.2 Thermal Conditions for 88E1512/88E1514 56-pin, QFN Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient for the device 56-Pin QFN package $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		33.1		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		28.7		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		27.6		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		26.7		°C/W
ψ_{JT}	Thermal characteristic parameter[a] - junction to top center of the device 56-Pin QFN package $\psi_{JT} = (T_J - T_{top})/P$. P = Total power dissipation $T_{top:}$ Temperature on the top center of the package.	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.54		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.92		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		1.17		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		1.31		°C/W
θ_{JC}	Thermal resistance[1] - junction to case for the device 56-Pin QFN package $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow		17.8		°C/W
θ_{JB}	Thermal resistance[1] - junction to board for the device 56-Pin QFN package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		20.7		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

4.4 88E1510/88E1518 Current Consumption

Note

The following current consumption numbers are shown when external supplies are used. If internal regulators are used, the current consumption will not change; however, the power consumed inside the package will increase. Care must be exercised when calculating the total current drawn on a rail when internal regulators are used. If the 1.0V and 1.8V internal regulators are used, the 1.0V and 1.8V current must be multiplied by 3.3V for power consumption calculation.

4.4.1 Current Consumption AVDD18 + AVDDC18

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{AVDD}	1.8V Power to analog core	AVDD18	RGMII over 1000BASE-T with traffic		63		mA
			RGMII over 100BASE-TX with traffic		25		mA
			RGMII over 10BASE-T with traffic		17		mA
			RGMII over 1000BASE-T with EEE		35		mA
			RGMII over 100BASE-TX with EEE		30		mA
			Energy Detect		10		mA
			IEEE Power Down		4		mA

4.4.2 Current Consumption AVDD33[1]

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{AVDDR}	Analog 3.3V supply	AVDD33	RGMII over 1000BASE-T with traffic		50		mA
			RGMII over 100BASE-TX with traffic		12		mA
			RGMII over 10BASE-T with traffic		30		mA
			RGMII over 1000BASE-T with EEE		7		mA
			RGMII over 100BASE-TX with EEE		2		mA
			Energy Detect		2		mA
			IEEE Power Down		1		mA

1. AVDD33 current shown assumes no internal regulator are used.

4.4.3 Current Consumption DVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{VDD}	1.0V Power to digital core	DVDD	RGMII over 1000BASE-T with traffic		72		mA
			RGMII over 100BASE-TX with traffic		14		mA
			RGMII over 10BASE-T with traffic		9		mA
			RGMII over 1000BASE-T with EEE		14		mA
			RGMII over 100BASE-TX with EEE		10		mA
			Energy Detect		7		mA
			IEEE Power Down		7		mA

4.4.4 Current Consumption VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Units
I_{VDDO}	Power to the digital I/Os	VDDO	RGMII over 1000BASE-T with traffic	VDDO = 3.3V		45		mA
				VDDO = 2.5V		36		mA
				VDDO = 1.8V		27		mA
			RGMII over 100BASE-TX with traffic	VDDO = 3.3V		14		mA
				VDDO = 2.5V		10		mA
				VDDO = 1.8V		8		mA
			RGMII over 10BASE-T with traffic	VDDO = 3.3V		9		mA
				VDDO = 2.5V		7		mA
				VDDO = 1.8V		6		mA
			RGMII over 1000BASE-T with EEE[1]	VDDO = 3.3V		7		mA
				VDDO = 2.5V		6		mA
				VDDO = 1.8V		5		mA
			RGMII over 100BASE-TX with EEE	VDDO = 3.3V		6		mA
				VDDO = 2.5V		5		mA
				VDDO = 1.8V		4		mA
			Energy Detect	VDDO = 3.3V		9		mA
				VDDO = 2.5V		7		mA
				VDDO = 1.8V		6		mA
			IEEE Power Down	VDDO = 3.3V		9		mA
				VDDO = 2.5V		7		mA
				VDDO = 1.8V		6		mA

1. VDDO EEE current consumption is measured with clock-stoppable bit enabled, wherein the RX_CLK is powered down after 9 clock cycles after entering EEE LPI state using Device 3 Register 0 bit 10.

4.5 88E1512 Current Consumption

Note

The following current consumption numbers are shown when external supplies are used. If internal regulators are used, the current consumption will not change; however, the power consumed inside the package will increase. Care must be exercised when calculating the total current drawn on a rail when internal regulators are used. If the 1.0V and 1.8V internal regulators are used, the 1.0V and 1.8V current must be multiplied by 3.3V for power consumption calculation.

4.5.1 Current Consumption AVDD18 + AVDDC18

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{AVDD}	1.8V Power to analog core	AVDD18	SGMII over 1000BASE-T with traffic		84		mA
			SGMII over 100BASE-TX with traffic		49		mA
			SGMII over 10BASE-T with traffic		35		mA
			RGMII to SGMII over 1000BASE-T with traffic		25		mA
			RGMII to SGMII over 100BASE-TX with traffic		25		mA
			RGMII to SGMII over 10BASE-T with traffic		25		mA
			SGMII over 1000BASE-T with EEE		35		mA
			SGMII over 100BASE-TX with EEE		30		mA
			Energy Detect		10		mA
			IEEE Power Down		4		mA

4.5.2 Current Consumption AVDD33[1]

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{AVDDR}	Analog 3.3V supply	AVDD33	SGMII over 1000BASE-T with traffic		52		mA
			SGMII over 100BASE-TX with traffic		13		mA
			SGMII over 10BASE-T with traffic		26		mA
			RGMII to SGMII over 1000BASE-T with traffic		0		mA
			RGMII to SGMII over 100BASE-TX with traffic		0		mA
			RGMII to SGMII over 10BASE-T with traffic		0		mA
			SGMII over 1000BASE-T with EEE		4		mA
			SGMII over 100BASE-TX with EEE		4		mA
			Energy Detect		2		mA
			IEEE Power Down		1		mA

1. AVDD33 current shown assumes no internal regulator are used.

4.5.3 Current Consumption DVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{VDD}	1.0V Power to digital core	DVDD	SGMII over 1000BASE-T with traffic		73		mA
			SGMII over 100BASE-TX with traffic		16		mA
			SGMII over 10BASE-T with traffic		9		mA
			RGMII to SGMII over 1000BASE-T with traffic		14		mA
			RGMII to SGMII over 100BASE-TX with traffic		11		mA
			RGMII to SGMII over 10BASE-T with traffic		10		mA
			SGMII over 1000BASE-T with EEE		35		mA
			SGMII over 100BASE-TX with EEE		30		mA
			Energy Detect		7		mA
			IEEE Power Down		7		mA

4.5.4 Current Consumption VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Units
I_{VDDO}	Power to the digital I/Os	VDDO	SGMII over 1000BASE-T with traffic	VDDO = 3.3V		4		mA
			SGMII over 100BASE-TX with traffic	VDDO = 2.5V		4		mA
			SGMII over 10BASE-T with traffic	VDDO = 1.8V		4		mA
			RGMII to SGMII over 1000BASE-T with traffic	VDDO = 3.3V		44		mA
				VDDO = 2.5V		36		mA
				VDDO = 1.8V		27		mA
			RGMII to SGMII over 100BASE-TX with traffic	VDDO = 3.3V		12		mA
				VDDO = 2.5V		10		mA
				VDDO = 1.8V		9		mA
			RGMII to SGMII over 10BASE-T with traffic	VDDO = 3.3V		7		mA
				VDDO = 2.5V		7		mA
				VDDO = 1.8V		7		mA
			SGMII over 1000BASE-T with EEE[1]	VDDO = 3.3V		4		mA
				VDDO = 2.5V		4		mA
				VDDO = 1.8V		4		mA
			SGMII over 100BASE-TX with EEE	VDDO = 3.3V		4		mA
				VDDO = 2.5V		4		mA
				VDDO = 1.8V		4		mA
			Energy Detect	VDDO = 3.3V		9		mA
				VDDO = 2.5V		7		mA
				VDDO = 1.8V		6		mA
			IEEE Power Down	VDDO = 3.3V		9		mA
				VDDO = 2.5V		7		mA
				VDDO = 1.8V		6		mA

1. VDDO EEE current consumption is measured with clock-stoppable bit enabled, wherein the RX_CLK is powered down after 9 clock cycles after entering EEE LPI state using Device 3 Register 0 bit 10.

4.6 DC Operating Conditions

4.6.1 Digital Pins

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins[1]	Condition	Min	Typ	Max	Units
VIH	Input high voltage	All digital inputs	VDDO = 3.3V	2.0			V
			VDDO = 2.5V	1.75			V
			VDDO = 1.8V	1.26		VDDO+ 0.6V	V
VIL	Input low voltage	All digital inputs	VDDO = 3.3V			0.8	V
			VDDO = 2.5V			0.75	V
			VDDO = 1.8V (88E1518/ 88E1512/ 88E1514)	-0.3		0.54	V
VOH	High level output voltage	All digital outputs		VDDO - 0.4V			V
VOL	Low level output voltage	All digital outputs				0.4	V
I_{ILK}	Input leakage current					10	uA
C_{IN}	Input capacitance	All pins				5	pF

1. VDDO supplies the CLK125, MDC, MDIO, RESETn, LED[2:0], CONFIG, TX_CLK, TX_CTRL, TXD[3:0], RX_CLK, RX_CTRL, and RXD[3:0].

4.6.2 IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.
-10BASE-T IEEE 802.3 Clause 14
-100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	MDIP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		MDIP/N[1:0]	10BASE-T cable model	585[1]			mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	1.0	1.050	V
		MDIP/N[3:0]	1000BASE-T[2]	0.67	0.75	0.82	V
	Overshoot[2]	MDIP/N[:0]	100BASE-TX mode	0		5%	V
	Amplitude Sym-metry (positive/ negative)	MDIP/N[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDIP/N[:0]	10BASE-T mode	585[3]			mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	1000	460[4]		mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360[5]		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test ; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The device will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The Alaska® Quad will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

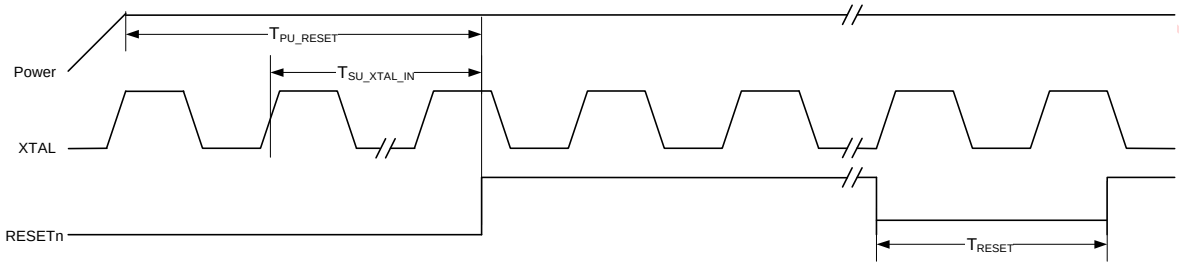
4.7 AC Electrical Specifications

4.7.1 Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted		10			ms
$T_{SU\_XTAL\_IN}$	Number of valid XTAL_IN cycles prior to RESETn de-asserted		10			clks
T_{RESET}	Minimum reset pulse width during normal operation		10			ms

Figure 27: Reset Timing



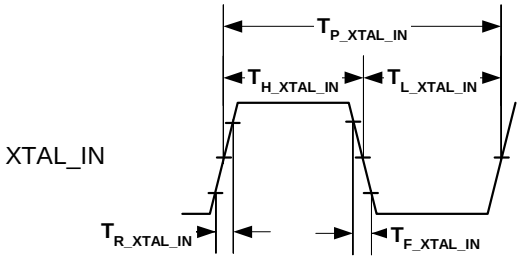
4.7.2 XTAL_IN/XTAL_OUT Timing[1]

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_XTAL\_IN}$	XTAL_IN Period		40 -50 ppm	40	40 +50 ppm	ns
$T_{H\_XTAL\_IN}$	XTAL_IN High time		13	20	27	ns
$T_{L\_XTAL\_IN}$	XTAL_IN Low time		13	20	27	ns
$T_{R\_XTAL\_IN}$	XTAL_IN Rise	10% to 90%	-	3.0	-	ns
$T_{F\_XTAL\_IN}$	XTAL_IN Fall	90% to 10%	-	3.0	-	ns
$T_{J\_XTAL\_IN}$	XTAL_IN total jitter[2]		-	-	200	ps[3]
XTAL_ESR	Crystal ESR[4]		-	30	50	Ω

1. If the crystal option is used, ensure that the frequency is 25 MHz ± 50 ppm. Capacitors must be chosen carefully - see application note supplied by the crystal vendor.
2. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
3. 12 kHz to 20 MHz rms jitter on XTAL_IN = 4 ps.
4. See “How to use Crystals as Clock Sources” application note for details.

Figure 28: XTAL_IN/XTAL_OUT Timing

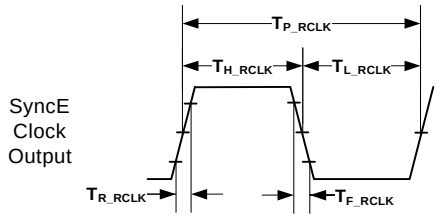


4.7.3 SyncE Recovered Clock Output Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_RCLK}	Period	125 MHz		8		ns
		25 MHz		40		ns
T_{H_RCLK}	High Time	125 MHz		4		ns
		25 MHz		20		ns
T_{L_RCLK}	Low Time	125 MHz		4		ns
		25 MHz		20		ns
T_{R_RCLK}	Rise Time	125 MHz		0.9		ns
		25 MHz		0.9		ns
T_{F_RCLK}	Fall Time	125 MHz		0.5		ns
		25 MHz		0.5		ns
T_{J_RCLK}	Total Jitter	125 MHz				ps
		25 MHz				ps
T	Duty Cycle	125 MHz	45	50	55	%
		25 MHz	45	50	55	%

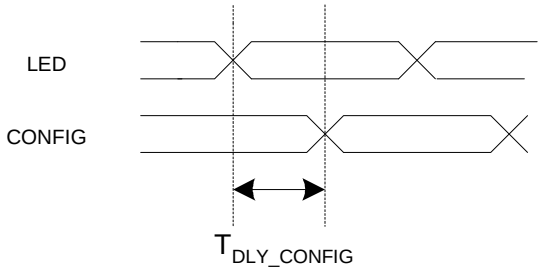
Figure 29: SyncE Clock Output Timing



4.7.4 LED to CONFIG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_CONFIG}	LED to CONFIG Delay		0		25	ns

Figure 30: LED to CONFIG Timing



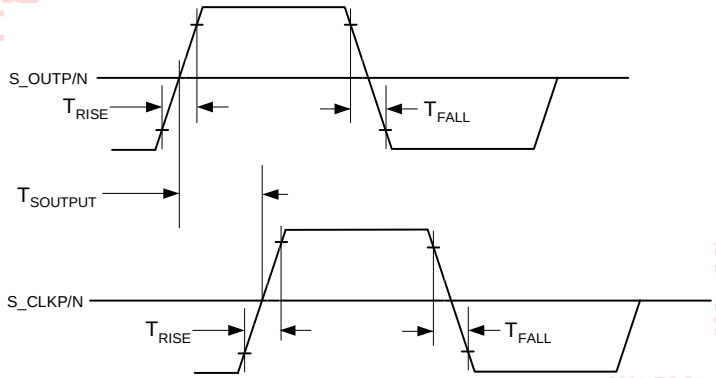
4.8 SGMII Interface Timing

4.8.1 SGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	V_{OD} Fall time (20% - 80%)	100		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	100		200	ps
CLOCK	Clock signal duty cycle @ 625 MHz	48		52	%
T_{SKEW1}[1]	Skew between two members of a differential pair			20	ps
$T_{SOUTPUT}$[2]	SERDES output to RxClk_P/N	360	400	440	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14*rms Random)		127		ps

1. Skew measured at 50% of the transition.
2. Measured at 50% of the transition.

Figure 31: Serial Interface Rise and Fall Times



4.8.2 SGMII Input AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14*rms Random)			599	ps

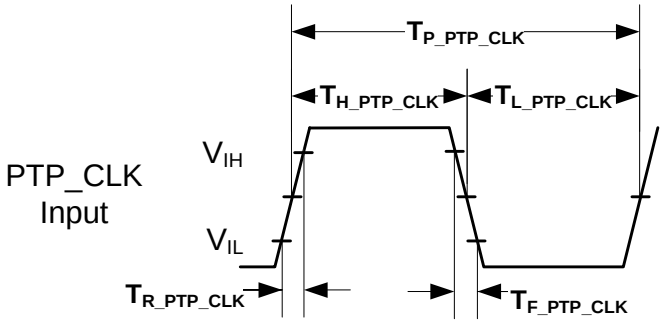
4.9 PTP Interface Timing

4.9.1 PTP Clock Input Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_PTP\_CLK}$	PTP Clock Period	125 MHz	8 -50 ppm	8	8 +50 ppm	ns
$T_{H\_PTP\_CLK}$	PTP Clock High time	125 MHz	2.8	4	5.2	ns
$T_{L\_PTP\_CLK}$	PTP Clock Low time	125 MHz	2.8	4	5.2	ns
$T_{R\_PTP\_CLK}$	PTP Clock Rise	V_{IL}(max) to V_{IH}(min) - 125 MHz		0.6		ns
$T_{F\_PTP\_CLK}$	PTP Clock Fall	V_{IH}(min) to V_{IL}(max) - 125 MHz		0.6		ns
$T_{J\_PTP\_CLK}$	PTP Clock jitter total					ps

Figure 32: PTP Clock Input Timing



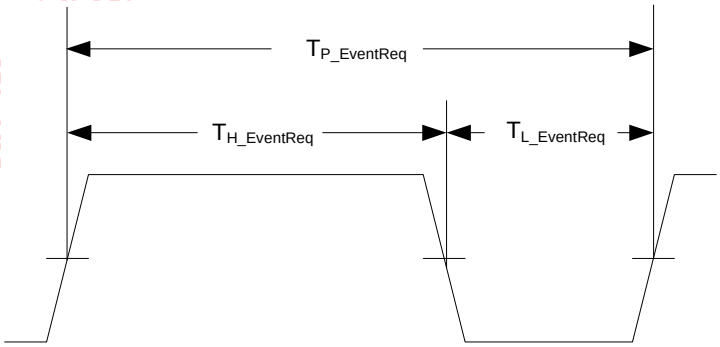
4.9.2 PTP Event Request Input AC Timing (LED[1])

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_EventReq}$	Minimum gap between two PTP Event Request		280 ns + 5*TSClk-Per			ns, TSClk-Per[1]
$T_{H\_EventReq}$	PTP Event Request Pulse Width		1.5 * TSClkPer			TSClkPer
$T_{L\_EventReq}$	PTP Event Request Low Time		1.5 * TSClkPer			TSClkPer

1. TSClkPer is specified by bit[15:0] of the TAI Global Configuration Register 1 – Page 12, Register 1. The default value is 0x1F40 (8ns)

Figure 33: PTP Event Request Input Timing



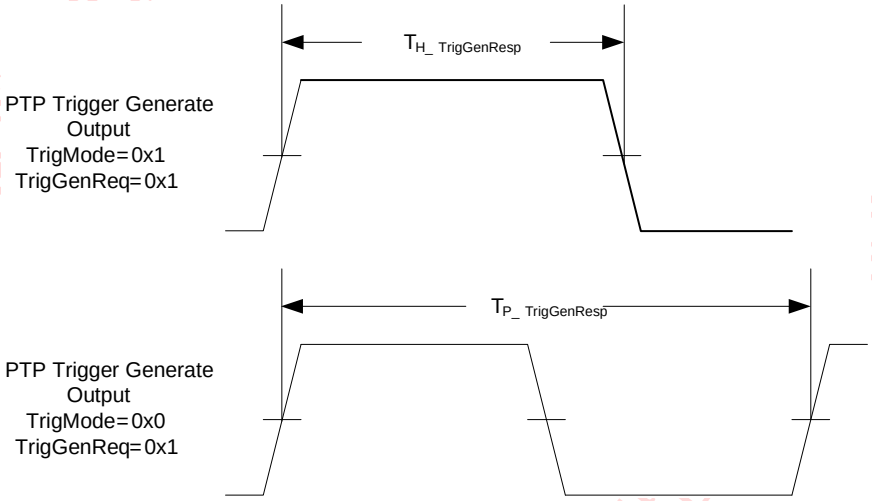
4.9.3 PTP Trigger Generate Output AC Timing (LED[1])

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{H\_TrigGenResp}$	PTP Trigger Generate Output Pulse Width[1]		1*TSClkPer	PulseWidth[2]	15*TSClkPer	TSClkPer[3]
$T_{P\_TrigGenResp}$	PTP Trigger Generate Output Clock Period[4]		2*TSClkPer	TrigGenAMT[5]		TSClkPer ns
$T_{P\_TrigGenResp\_DC}$	PTP Trigger Generate Output Clock Period Duty Cycle		40		60	%

1. The PTP Trigger Generate Output is used to generate a pulse when TrigMode is set to '1' and TrigGenReq is set to '1'
2. The Pulse Width is specified by bit[15:12] of the TAI Global Configuration Register 5 – Page 12, Register 5 in increments of TSClkPer
3. TSClkPer is specified by bit[15:0] of the TAI Global Configuration Register 1 – Page 12, Register 1. The default value is 0x1F40 (8ns)
4. The PTP Trigger Generate Output is used to generate a periodic clock when TrigMode is set to '0' and TrigGenReq is set to '1'.
5. The Output Period is specified by bit[15:0] of the TAI Global Configuration Register 2 – Page 12, Register 2 and bit[15:0] of the TAI Global Configuration Register 3 – Page 12, Register 3 in increments of TSClkPer. If the TrigGenAmt is not set in TSClkPer increments, the TrigClkComp, which is specified by bit[15:0] of the TAI Global Configuration Register 4 – Page 12, Register 4, gets accumulated internally and when this accumulated value exceeds the TSClkPer, a TSCLKPer amount will be added to the clock output.

Figure 34: PTP Trigger Generate Output Timing



4.10 RGMII Interface Timing

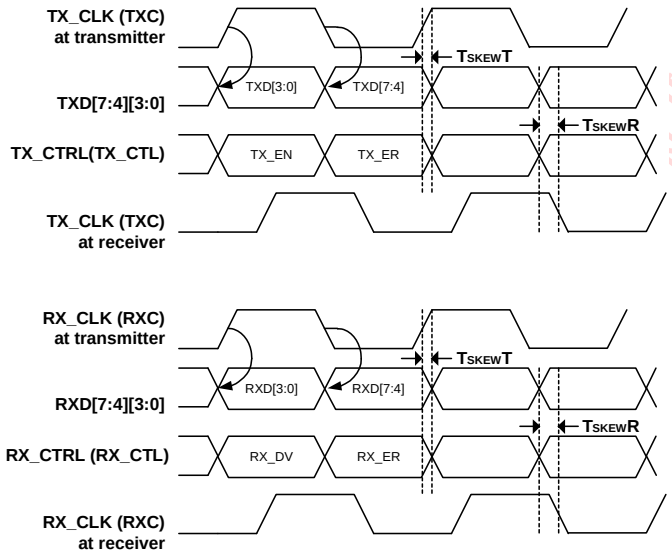
4.10.1 RGMII AC Characteristics

(This table is copied from the RGMII Specification. See Application Note “RGMII Timing Modes” for details of how to convert the timings in this table to the four timing modes discussed in Section 4.10.2 "RGMII Delay Timing for different RGMII Modes" on page 252).

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.8	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
$T_{CYCLE\_HIGH100}$	High Time for 100BASE-T[1]	16	20	24	ns
T_{CYCLE_HIGH10}	High Time for 10BASE-T[1]	160	200	240	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)			0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet’s clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three TCYCLE of the lowest speed transitioned between.

Figure 35: RGMII Multiplexing and Timing



This figure is copied from the RGMII Specification. See Application Note “RGMII Timing Modes” for details of how to convert the timings in this table to the four timing modes discussed in Section 4.10.2 "RGMII Delay Timing for different RGMII Modes" on page 252

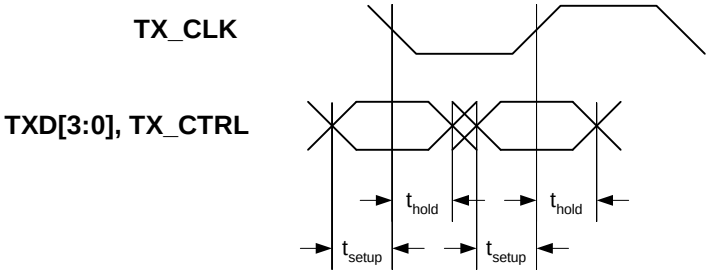
4.10.2 RGMII Delay Timing for different RGMII Modes

4.10.2.1 PHY Input - TX_CLK Delay when Register 21_2.4 = 0

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 21_2.4 = 0	1.0			ns
t_{hold}		0.8			ns

Figure 36: TX_CLK Delay Timing - Register 21_2.4 = 0

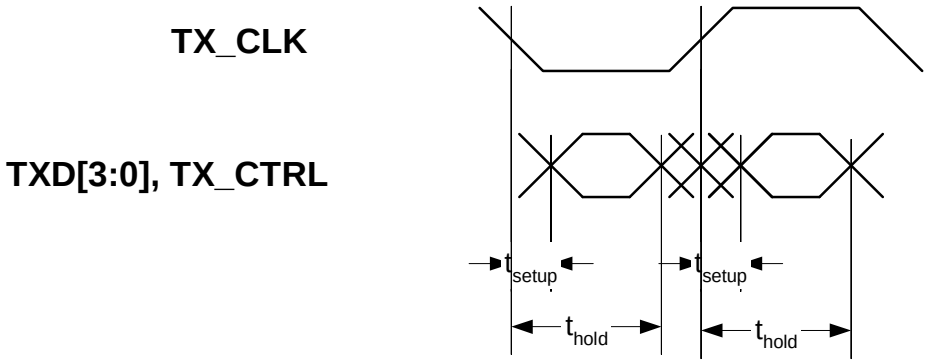


4.10.2.2 PHY Input - TX_CLK Delay when Register 21_2.4 = 1

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 21_2.4 = 1 (add delay)	-0.9			ns
t_{hold}		2.7			ns

Figure 37: TX_CLK Delay Timing - Register 21_2.4 = 1 (add delay)

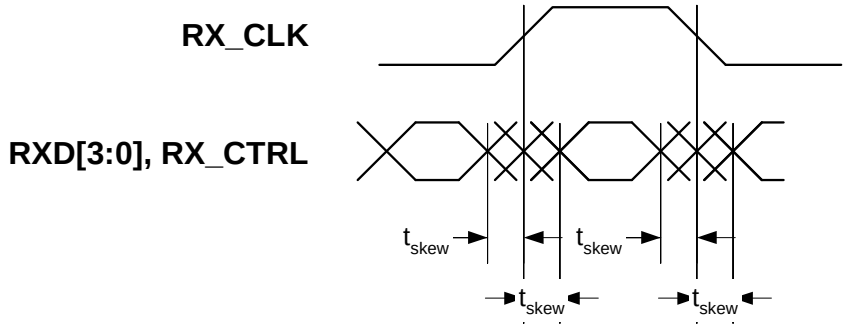


4.10.2.3 PHY Output - RX_CLK Delay

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{skew}	Register 21_2.5 = 0	- 0.5		0.5	ns

Figure 38: RGMII RX_CLK Delay Timing - Register 21_2.5 = 0

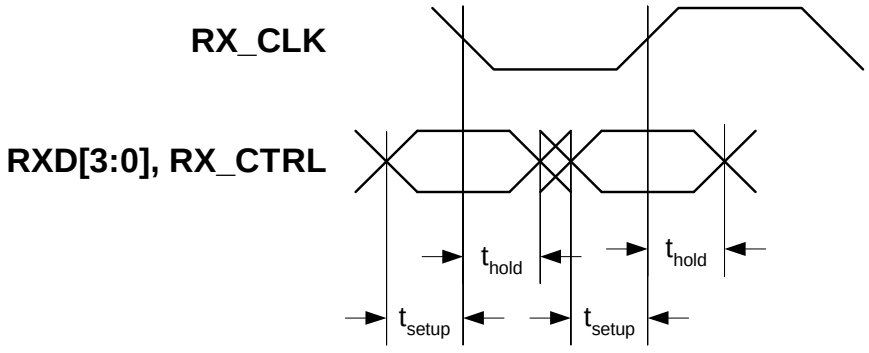


4.10.2.4 PHY Output - RX_CLK Delay

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 21_2.5 = 1 (add delay)	1.2			ns
t_{hold}		1.2			ns

Figure 39: RGMII RX_CLK Delay Timing - Register 21_2.5 = 1 (add delay)



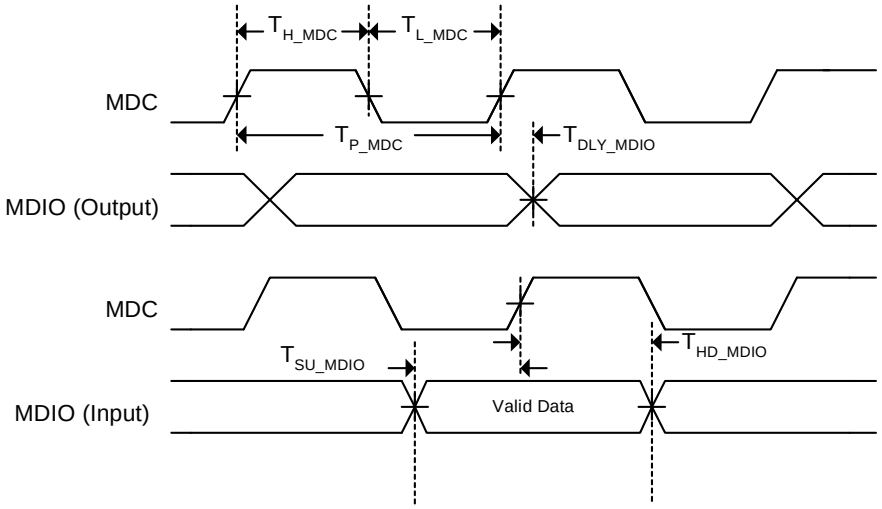
4.11 MDC/MDIO Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time		0		20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		10			ns
T_{P_MDC}	MDC Period		83.3			ns[1]
T_{H_MDC}	MDC High		30			ns
T_{L_MDC}	MDC Low		30			ns

1. Maximum frequency = 12 MHz.

Figure 40: MDC/MDIO Timing



4.12 IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14-2000
-100BASE-TX ANSI X3.263-1995
-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{RISE}/ T_{FALL} Symmetry		MDIP/N[1:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[1:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		MDIP/N[1:0]	100BASE-TX	0		1.4	ns, peak-peak

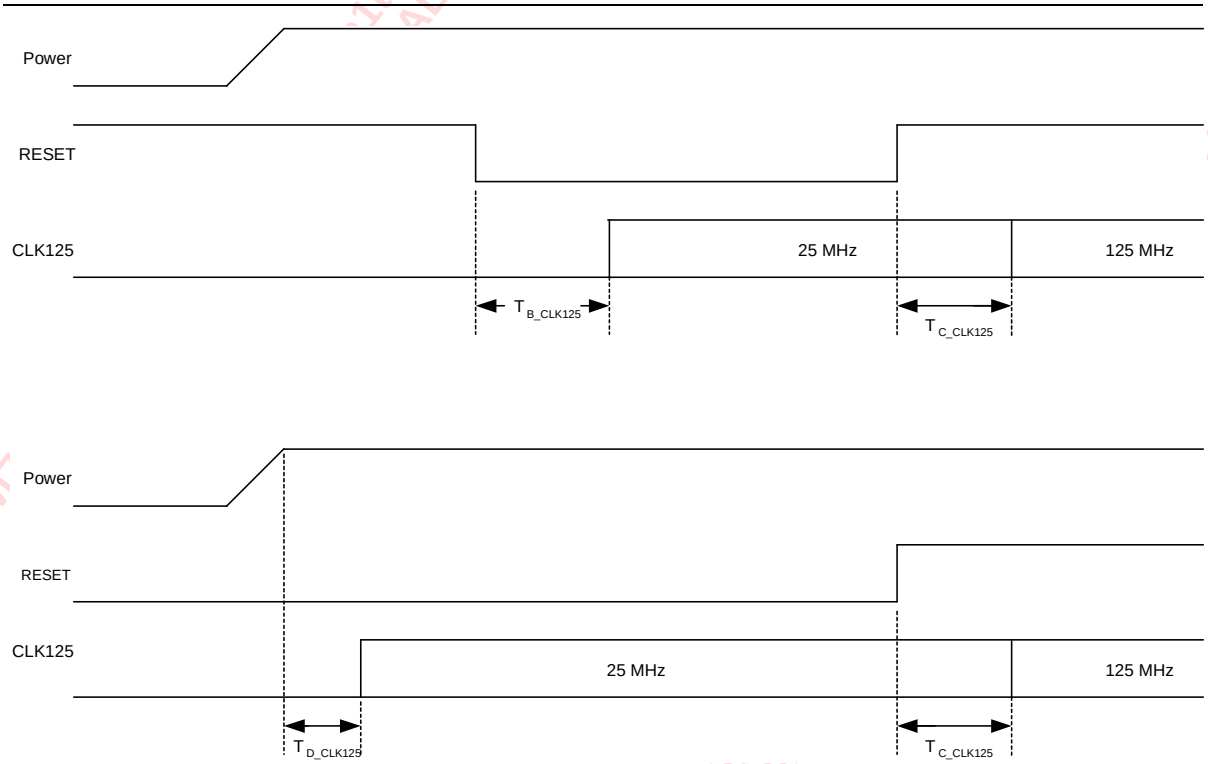
1. ANSI X3.263-1995 Figure 9-3

4.13 CLK125

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{J_CLK125}	CLK125 Total Jitter			500		ps
T_{B_CLK125}	RESETn Assert to 25 MHz					ns
T_{C_CLK125}	RESETn De-assert to 125 MHz					µs
T_{D_CLK125}	Power ON to 25 MHz					ns
Duty	Duty Cycle		40	50	60	%

Figure 41: Transition Timing



4.14 Latency Timing

4.14.1 RGMII to 1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_MDI\_1000}$	1000BASE-T TX_CTRL Asserted to MDI SSD1			161		ns
$T_{DA\_TXC\_MDI\_1000}$	1000BASE-T TX_CTRL De-asserted to MDI CSReset, CSExtend, CSExtend_Err			161		ns

4.14.2 RGMII to 100BASE-TX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified

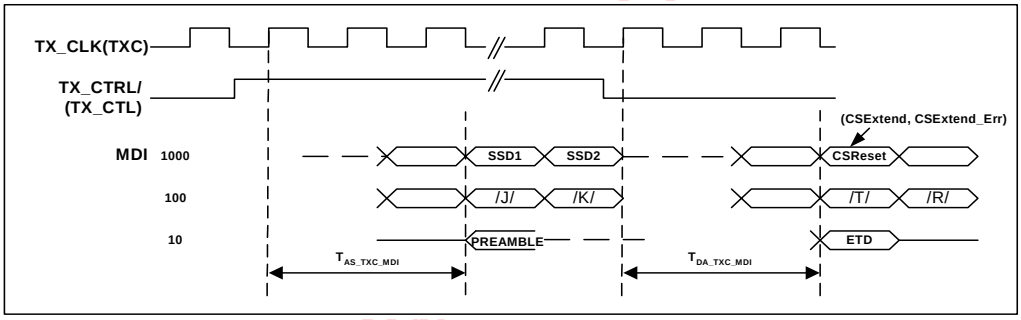
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_MDI\_100}$	100BASE-TX TX_CTRL Asserted to /J/			686		ns
$T_{DA\_TXC\_MDI\_100}$	100BASE-TX TX_CTRL De-asserted to /T/			686		ns

4.14.3 RGMII to 10BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_MDI\_10}$	10BASE-T TX_CTRL Asserted to Preamble			6.16		µs
$T_{DA\_TXC\_MDI\_10}$	10BASE-T TX_CTRL De-asserted to ETD			6.16		µs

Figure 42: RGMII/MII to 10/100/1000BASE-T Transmit Latency Timing



4.14.4 1000BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXC\_1000}$	1000BASE-T MDI start of Packet to RX_CTRL Asserted			236		ns
$T_{DA\_MDI\_RXC\_1000}$	1000BASE-T MDI CSReset, CSExtend, CSExtend_Err to RX_CTRL De-asserted			236		ns

4.14.5 100BASE-TX to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

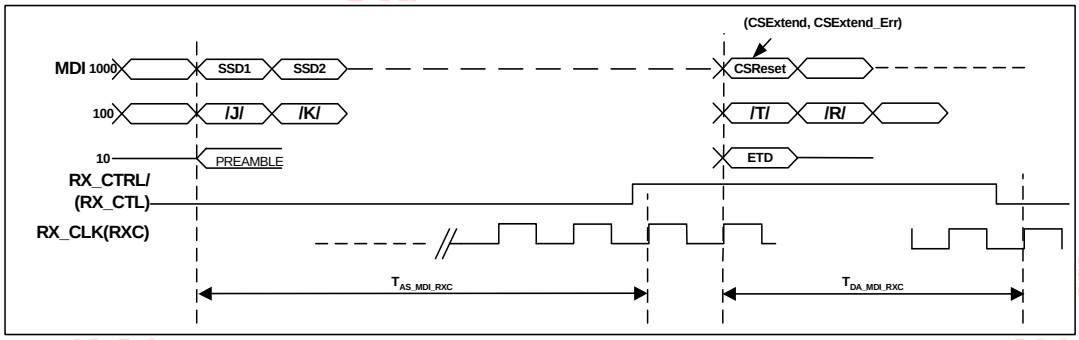
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXC\_100}$	100BASE-TX MDI start of Packet to RX_CTRL Asserted			357		ns
$T_{DA\_MDI\_RXC\_100}$	100BASE-TX MDI /T/ to RX_CTRL De-asserted			357		ns

4.14.6 10BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXC\_10}$	10BASE-T MDI start of Packet to RX_CTRL Asserted			2.18		µs
$T_{DA\_MDI\_RXC\_10}$	10BASE-T MDI ETD to RX_CTRL De-asserted			2.18		µs

Figure 43: 10/100/1000BASE-T to RGMII Receive Latency Timing



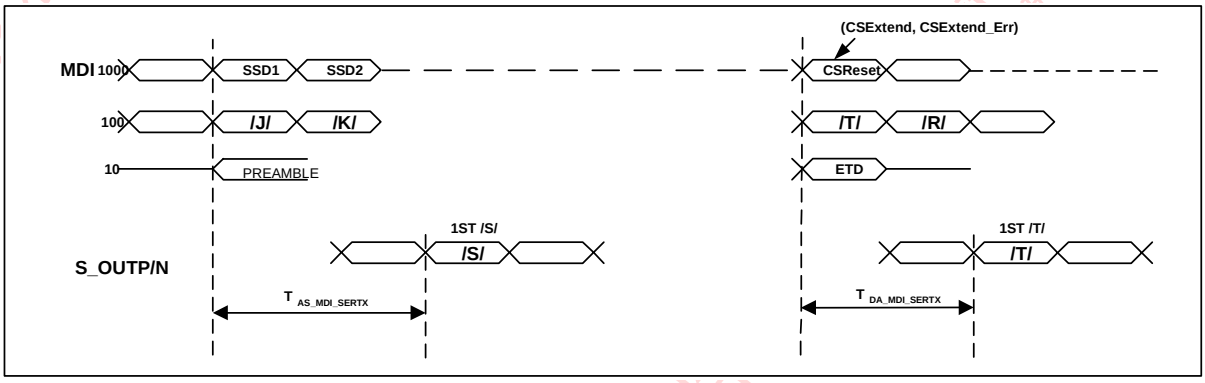
4.14.7 10/100/1000BASE-T to SGMII Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_SERTX\_1000}$[1,2]	MDI SSD1 to S_OUTP/N Start of Packet			340		ns
$T_{DA\_MDI\_SERTX\_1000}$[1,2,3]	MDI CSReset, CSExtend, CSExtend_Err to S_OUTP/N /T/			340		ns
$T_{AS\_MDI\_SERTX\_100}$[2]	MDI /J/ to S_OUTP/N Start of Packet			728		ns
$T_{DA\_MDI\_SERTX\_100}$[2,3]	MDI /T/ to S_OUTP/N /T/			728		ns
$T_{AS\_MDI\_SERTX\_10}$[2,4]	MDI Preamble to S_OUTP/N Start of Packet			5.39		us
$T_{DA\_MDI\_SERTX\_10}$[2,3,4]	MDI ETD to S_OUTP/N /T/			5.39		us

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDIP/N[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16_1.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and S_OUTP/N. The worst case variation will be outside these limits if there is a frequency difference.
4. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 44: 10/100/1000BASE-T to SGMII Latency Timing



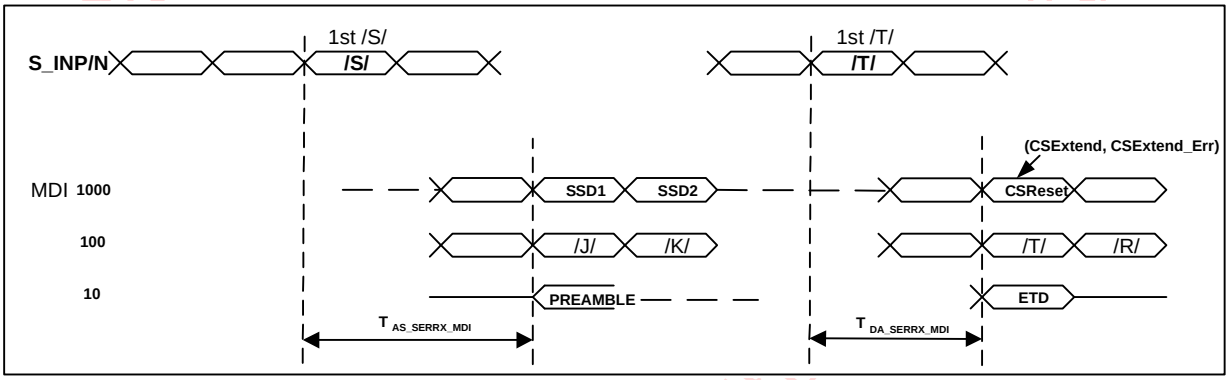
4.14.8 SGMII to 10/100/1000BASE-T Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERRX\_MDI\_1000}$[1]	S_INP/N Start of Packet /S/ to MDI SSD1			206		ns
$T_{DA\_SERRX\_MDI\_1000}$[1,2]	S_INP/N /T/ to MDI CSReset, CSExtend, CSExtend_Err			206		ns
$T_{AS\_SERRX\_MDI\_100}$[1]	S_INP/N Start of Packet /S/ to MDI /J/			633		ns
$T_{DA\_SERRX\_MDI\_100}$[1,2]	S_INP/N /T/ to MDI /T/			633		ns
$T_{AS\_SERRX\_MDI\_10}$[1]	S_INP/N Start of Packet /S/ to MDI Preamble			4.62		us
$T_{DA\_SERRX\_MDI\_10}$[1,2]	S_INP/N /T/ to MDI ETD			4.62		us

1. Assumes register 16_2.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on S_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

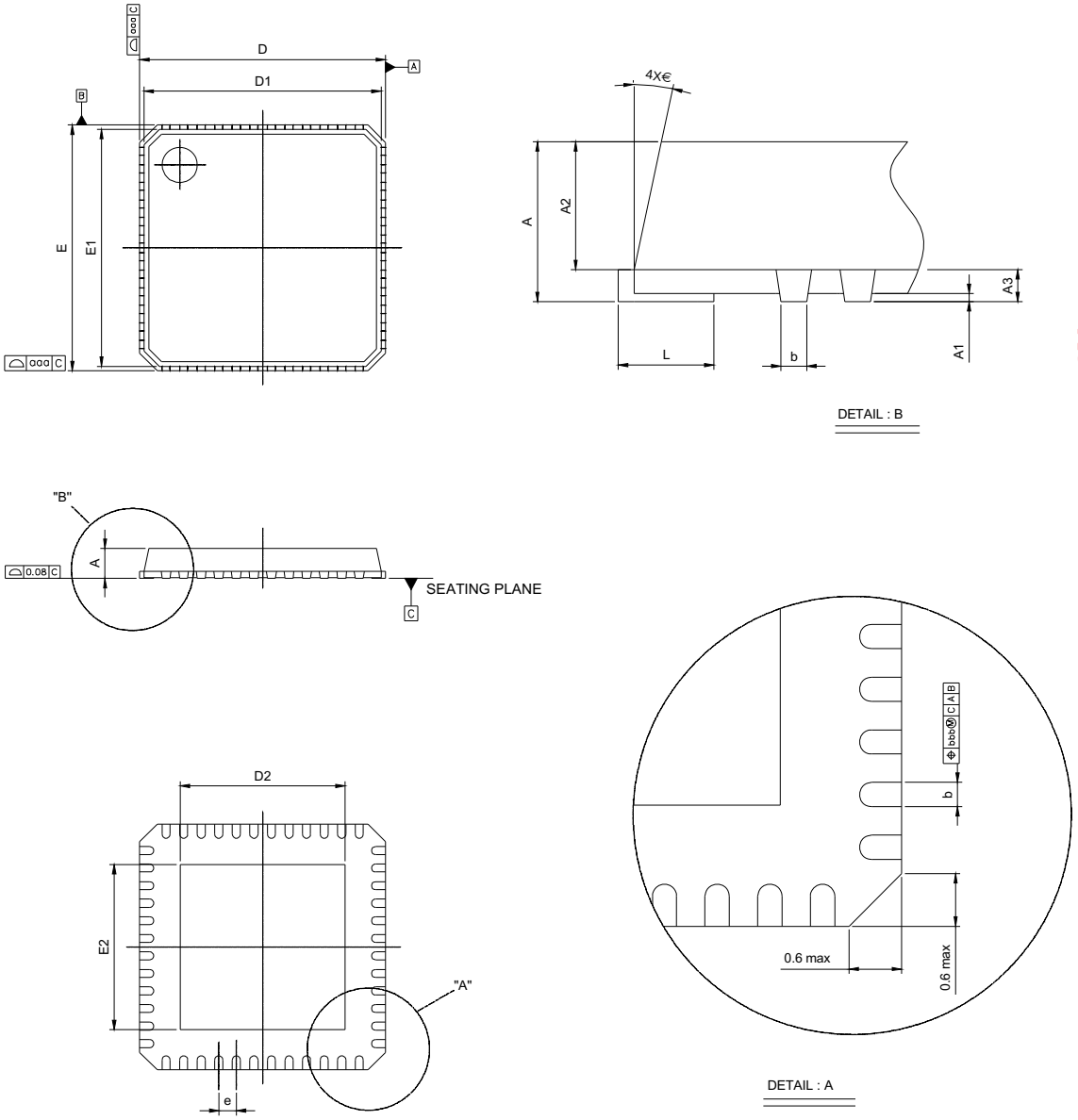
Figure 45: SGMII to 10/100/1000BASE-T Latency Timing



5 Package Mechanical Dimensions

5.1 48-Pin QFN Package

Figure 46: 88E1510/88E1518 48-pin QFN Package Mechanical Drawings



NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

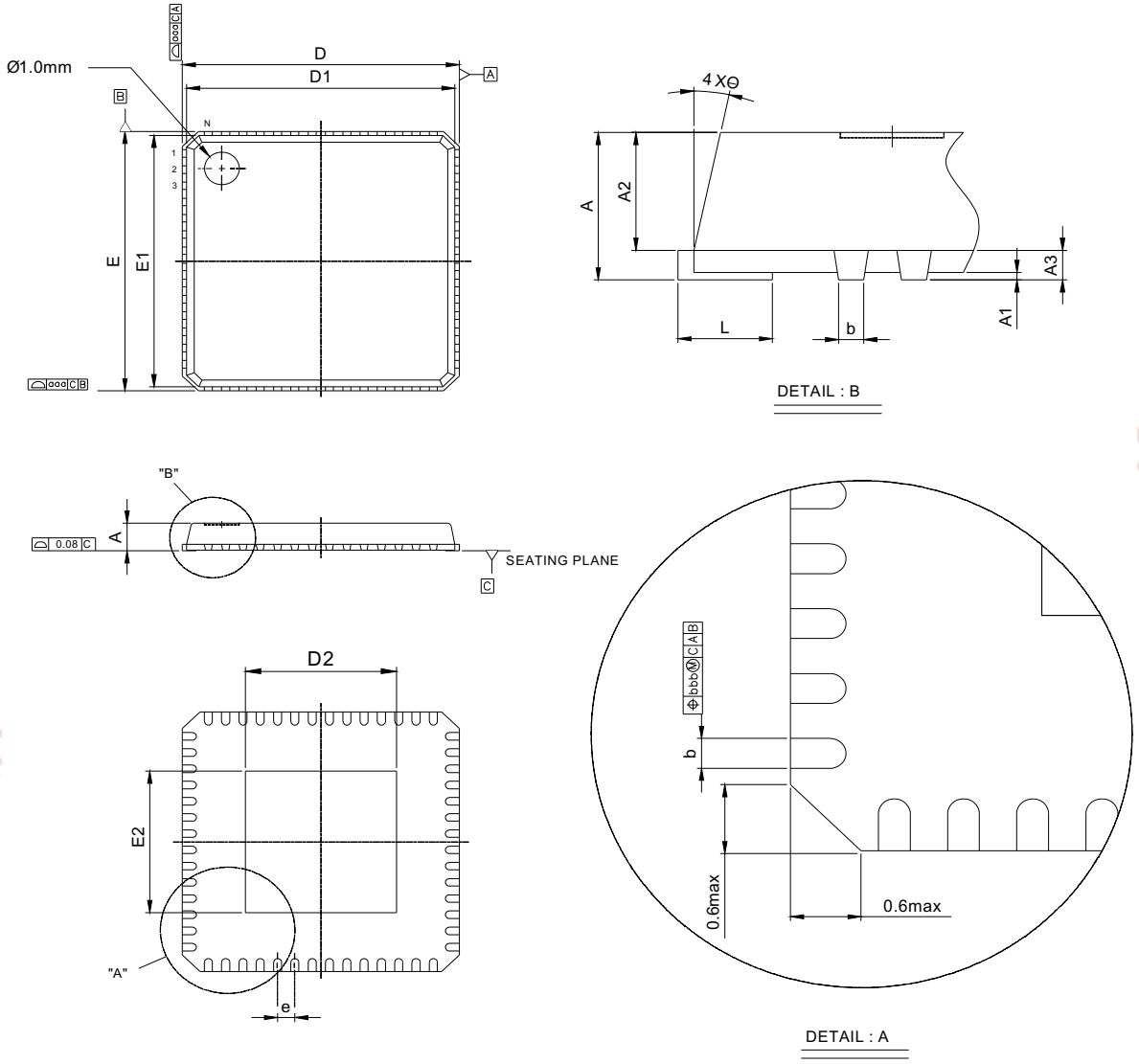
Table 232: 48-Pin QFN Mechanical Dimensions

	Dimensions in mm		
Symbol	**MIN**	**NOM**	**MAX**
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	--	0.65	1.00
A3		0.20 REF	
b	0.18	0.23	0.30
D		7.00 BSC	
D1		6.75 BSC	
E		7.00 BSC	
E1		6.75 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
θ	0°	--	12°
aaa	--	--	0.25
bbb	--	--	0.10
chamfer	--	--	0.60

Die Pad Size	
Symbol	**Dimension in mm**
D_2	3.10
E_2	3.10

5.2 56-Pin QFN Package

Figure 47: 88E1512/88E1514 56-pin QFN Package Mechanical Drawings



(All dimensions in mm.)

Table 233: 56-Pin QFN Mechanical Dimensions

Dimensions in mm			
Symbol	**MIN**	**NOM**	**MAX**
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	--	0.65	1.00
A3	0.20 REF		
b	0.18	0.23	0.30
D	8.00 BSC		
D1	7.75 BSC		
E	8.00 BSC		
E1	7.75 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
θ	0°	--	12°
aaa	--	--	0.15
bbb	--	--	0.10
chamfer	--	--	0.60

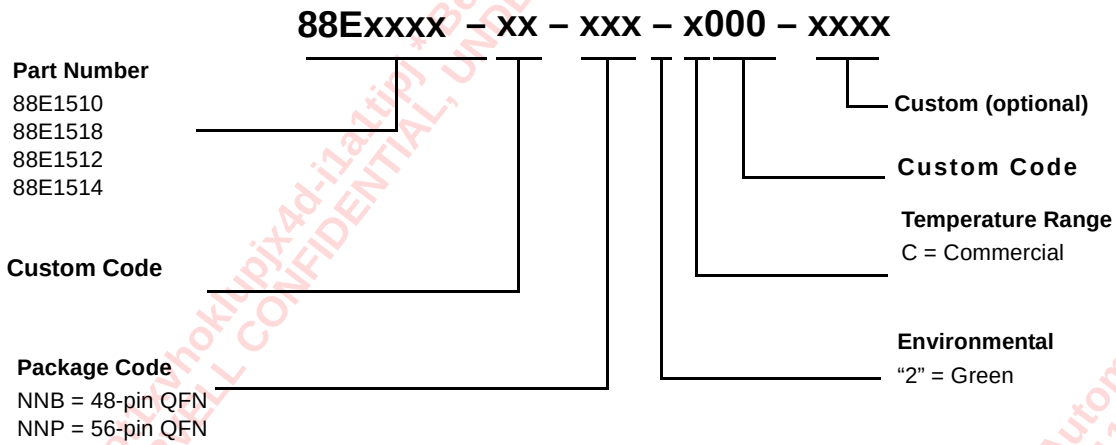
Die Pad Size	
Symbol	**Dimension in mm**
D_2	4.37
E_2	4.37

6 Order Information

6.1 Ordering Part Numbers and Package Markings

Figure 48 shows the ordering part numbering scheme for the device. Refer to the relevant release notes on the Marvell® extranet for the latest revision and complete part ordering information.

Figure 48: Sample Part Number



6.1.1 Package Marking Examples

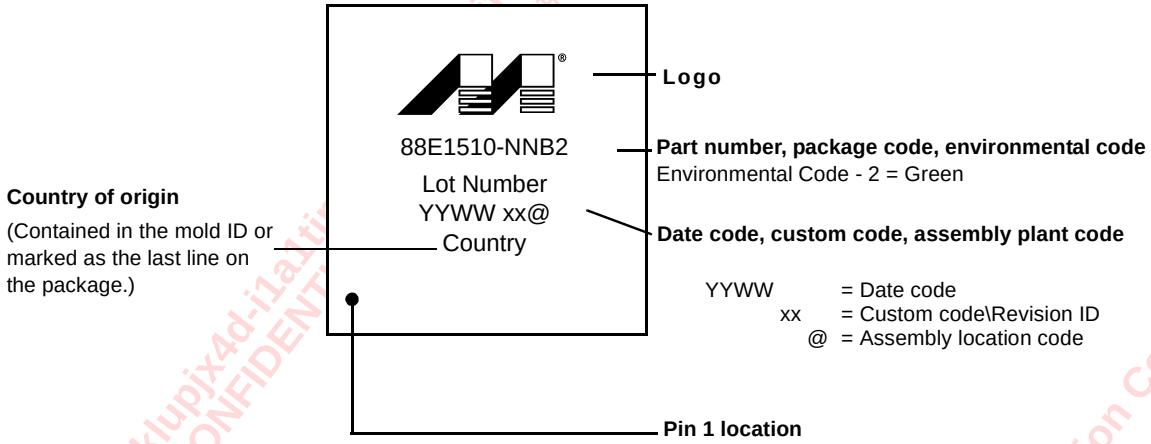
Table 234: Part Order Options

Package Type	Part Order Number
88E1510 48-pin QFN - Green - Commercial	88E1510-XX-NNB2C000
88E1510 48-pin QFN - Green - Industrial	88E1510-XX-NNB2I000
88E1518 48-pin QFN - Green - Commercial	88E1518-XX-NNB2C000
88E1512 56-pin QFN - Green - Commercial	88E1512-XX-NNP2C000
88E1512 56-pin QFN - Green - Industrial	88E1512-XX-NNP2I000
88E1514 56-pin QFN - Green - Commercial	88E1514-XX-NNP2C000

6.1.2 Package Marking Samples

Figure 49 is an example of the package marking and pin 1 location for the 88E1510 48-pin QFN commercial Green compliant package. The 88E1518 device package marking is similar.

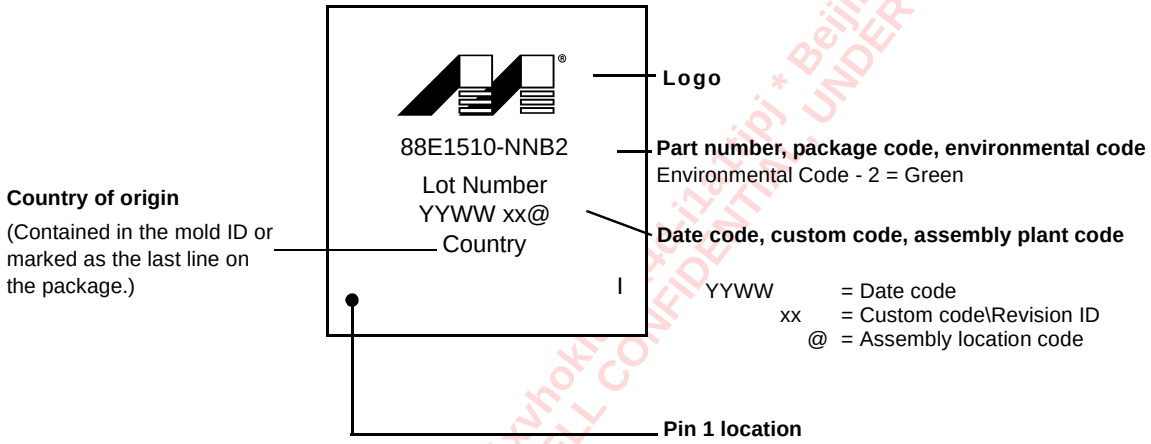
Figure 49: 88E1510 48-pin QFN Commercial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 50 is an example of the package marking and pin 1 location for the 88E1510 48-pin QFN industrial green compliant package. The 88E1518 and 88E1512 device package marking is similar.

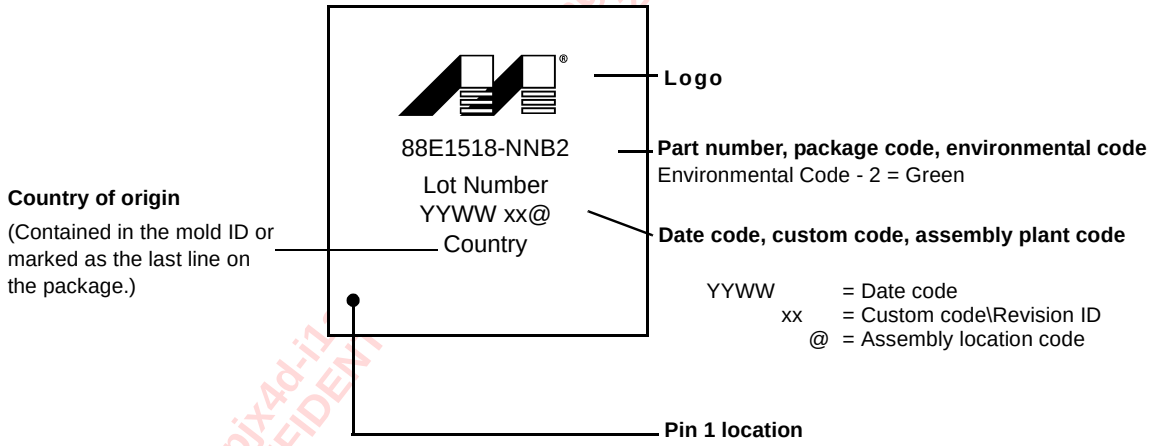
Figure 50: 88E1510 48-pin QFN Industrial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 51 is an example of the package marking and pin 1 location for the 88E1518 48-pin QFN commercial green compliant package.

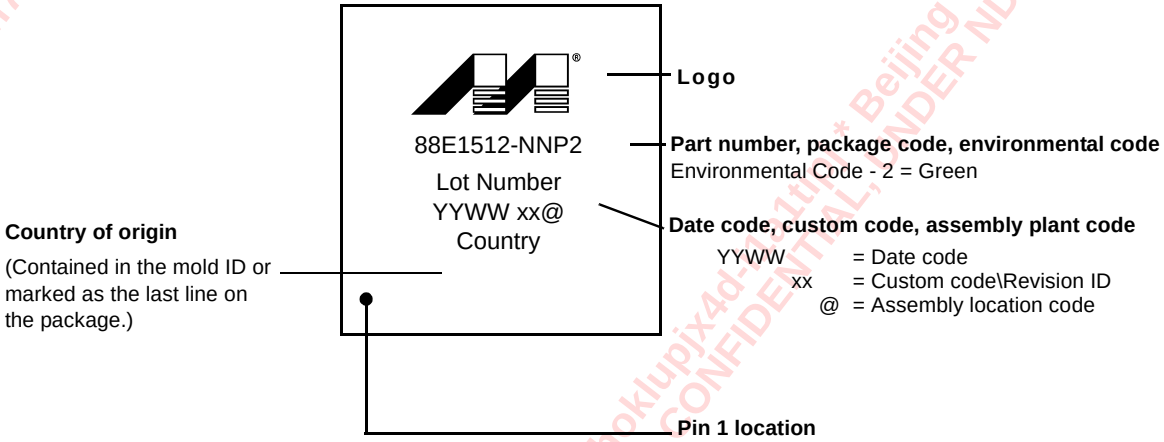
Figure 51: 88E1518 48-pin QFN Commercial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 52 is an example of the package marking and pin 1 location for the 88E1512 56-pin QFN commercial Green compliant package.

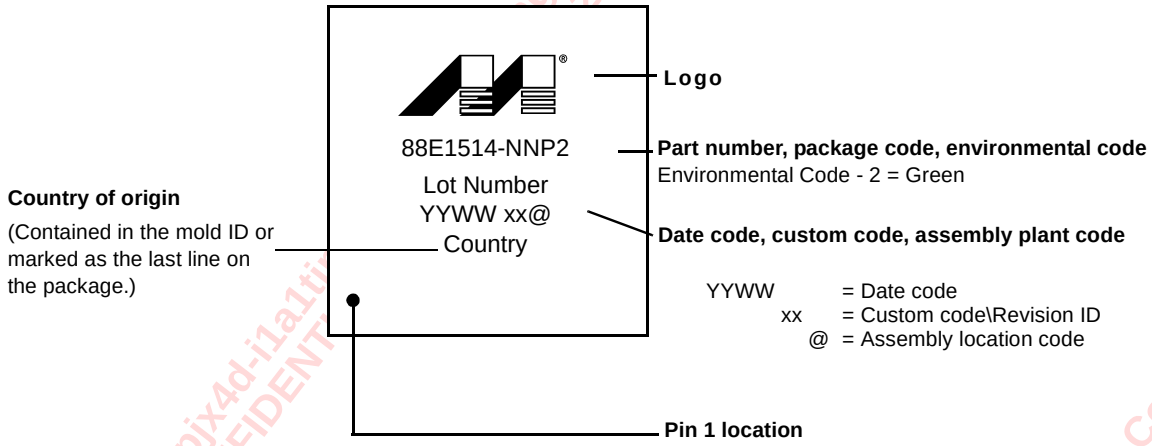
Figure 52: 88E1512 56-pin QFN Commercial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 53 is an example of the package marking and pin 1 location for the 88E1514 56-pin QFN commercial Green compliant package.

Figure 53: 88E1514 56-pin QFN Commercial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

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