ECE 341 Digital Systems Design
Test 1 (Section 3)

October 14, 2020

Instructions:

For this section, you will use Aldec Active-HDL to complete this assignment.

You are permitted to use the required textbook for this course (*Digital Systems Design using VHDL* by Roth & John, third edition).

You are permitted to use the course notes from Chapter 2 for this course.

Other than Dr. Belfore, you may not consult any other sources or persons unless otherwise directed in the problem statement.

If you have a question, send me an email with your question. Each person is permitted a maximum of one question.

In the event the problem requires a written response, follow the instructions given with Sections 1&2.

Upload a zip file containing your workspace and any other responses by 5:35pm on Oct 15 using the following link:

https://www.dropbox.com/request/kGjwI8YeoT6MXkta5Cv5

Good Luck!

I pledge to support the Honor System at Old Dominion University. I will refrain from any form of dishonesty or deception, such as lying, cheating, or plagiarizing, which are Honor violations. I am further aware that as a member of the academic community, it is my responsibility to turn in all suspected violators of the Honor System. I will report to an Honor Council hearing if summoned.

(Print name)	(Sign here or write out pledge on your submission and sign)

Section 3: Aldec Problem (25 points)

A1 (25 points) Aldec Programming Problem.

You are designing an electronic combination lock. To open the combination lock, you enter 8 BCD digits in succession. When the correct combination is entered, the lock opens by turning on the output Z.

Your combination will be determined at random. To determine the combination for your lock, go to www.random.org. In the box with "Generator" in the title, enter a minimum value of 0 and a maximum value of 99999999 and click "Generate". The "Result" is your combination. In your code, include this combination in a comment.

The combination lock model is implemented using a two process state machine model. For this problem, the first process is organized a little differently compared with the approach in your text book. Please use the decision framework in the code provided to implement your combination lock.

A zipped archive for an Aldec workspace is provided that includes a partial VHDL model and test bench in the class Dropbox folder ece341_f20/Tests. In addition, here is a separate web link to this same Dropbox folder ece341_f20/Tests.

Complete the combination lock model in the VHDL file problem4.vhd. Further, complete the test bench in the VHDL file problem4_TB.vhd to include a test of the combination being successfully input and also an incorrect combination. Be sure your timing diagram is saved and clearly shows both the successful and unsuccessful combinations.

When you have completed this problem, create a zip archive for your workspace and upload it using the link on the first page of this document.