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Computer Organization 2 Project

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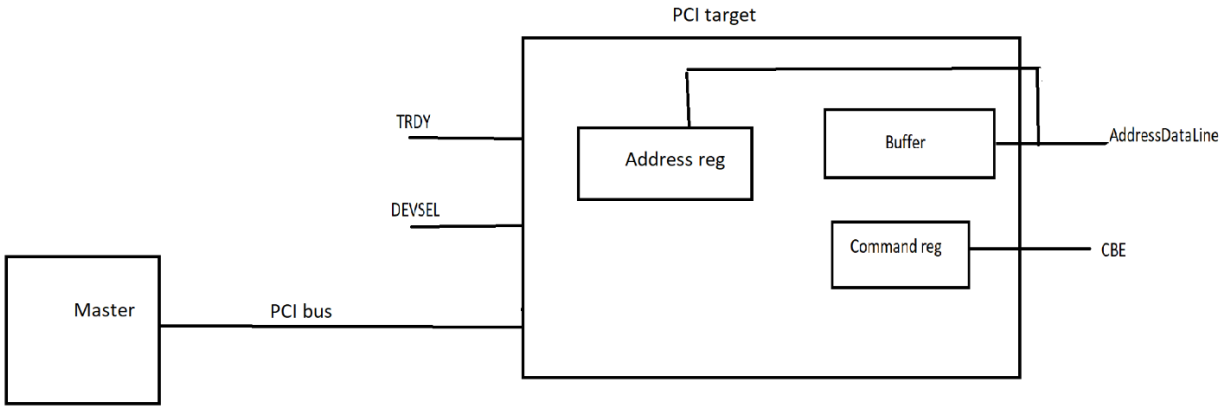

Figure 1:Block diagram

2. Description of all signals.

Signal	Description
Frame	• Initiates the start and duration of the transaction • Active Low
AddressDataLine	• In the first cycle it is the address phase where the address exists on this signal • Then it is the data phase where the data exists on this signal • Inout signal
oe	• To define the state of the AddressDataLine wire if it is input or output • When oe = 0 then the AddressDataLine is an output • When oe = 1 then the AddressDataLine is an input
RST	• Resets the target • Makes the TRDY and DEVSEL high
CBE	• To send the control signal (read or write) to the target in address phase • Then send the byte enable signals in data phase that modifies the data
IRDY	• It indicates that the Initiator is available to send or receive data. • In the write operation it means that a valid data is now on data lines • In the read operation it means that Initiator is ready to receive data

	• Active Low
TRDY	• It indicates that the target is available to complete the transaction • Active Low
DEVSEL	• It Is asserted by target when it has recognized its address. • Active Low
CLK	• Generated clock

3. Brief description for different read/write scenarios associated with waveform screenshots.

First Scenario: (Write &read 4 data starting from address zero)

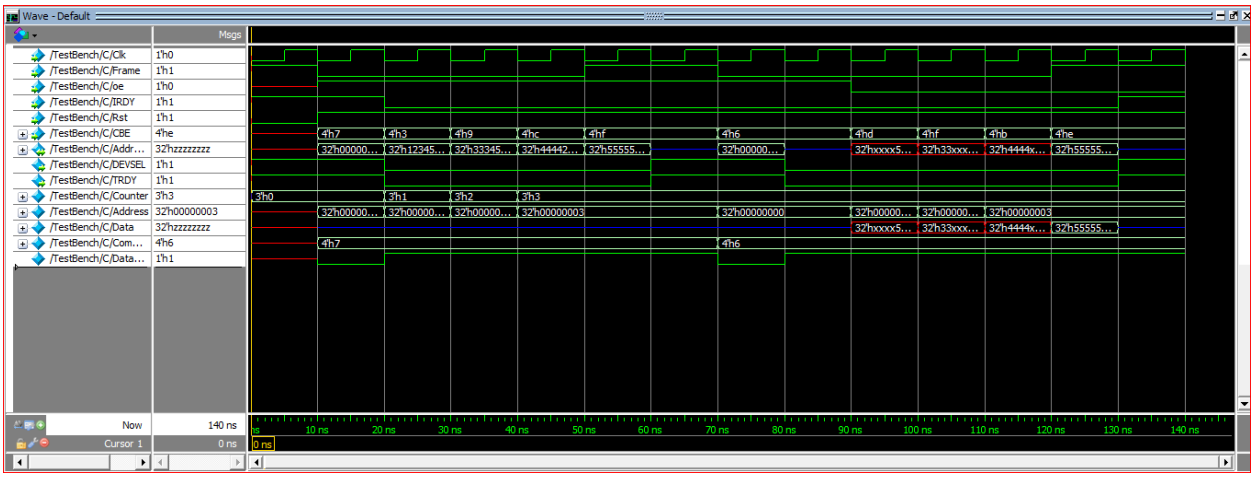

Figure 2: The full process of writing and reading 4 data starting from address 0

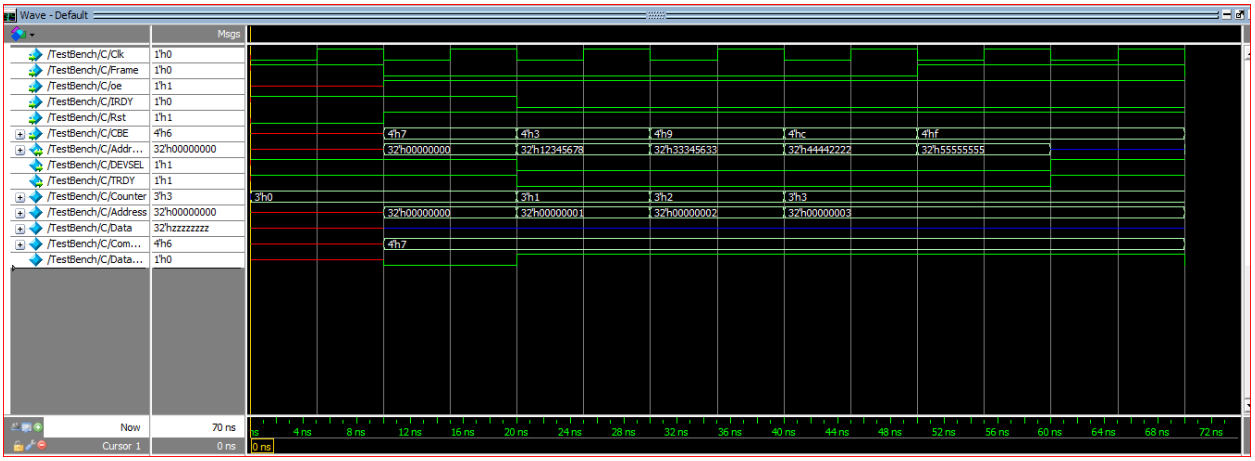

Figure 3: Writing 4 data in the buffer from address zero

1st Cycle :

- As we didn't initialize the address data line so in the first Clock cycle the address data line and the control line take (32'hX)
- Since the initiator is not ready yet to send data so (IRDY=1)
- Frame=1
- TRDY and DEVSEL are still =1

2nd Cycle:

- We controlled the address data line to be an input signal to our target by using a flag which we named (oe)
- The frame will be 0 with the negative edge of clock cycle as we start the write transaction
- The address data line takes the value of the address we want to start writing in, which is zero in this scenario
- The control line (CBE) takes the value of the write command which is assigned by (4'b0111)
- But the target is not ready yet to receive the data (TRDY=1 & DEVSEL=1)

3rd Cycle:

- The initiator now starts sending the data
- The initiator activates IRDY signal (IRDY=0)
- Since we assume that our Target is (**FAST**), so our target will be ready to write the data (TRDY=0 & DEVSEL=0)
- Starting to take the byte enable on the Control line from the initiator for the first data (4'b0011)
- The initiator sends the first data on the address data line which is 32'h12345678
- The target starts writing the first data in the buffer in address 0 , this data will be 32'hXXXX5678 because of the byte enable

4th Cycle:

- The address will increment to be 1
- Then the initiator sends the byte enable on the Control line for the second data (CBE = 4'b1001)

- The initiator sends the second data on the address data line which is 32'h33345633
- The Target will write the second data in address 1 in the buffer which is= 32'h33XXXX33

5th Cycle:

- The address will increment to be 2
- Then the initiator sends the byte enable on the Control line for the third data (CBE = 4'b1100)
- The initiator sends the third data on the address data line which is 32'h44442222
- The Target will write the third data in address 2 in the buffer which is 32'h4444XXXX

6th Cycle:

- The Frame will be 1 as there is the one last data remaining
- The address will increment to be 3
- Then the initiator sends the byte enable on the Control line for the fourth data (CBE = 4'b1111)
- The initiator sends the third data on the address data line which is 32'h55555555
- The Target will write the third data in address 2 in the buffer which is 32'h55555555

7th Cycle:

- Now the writing process has ended
- We are having a turnaround cycle
- IRDY will be 1
- TRDY and DEVSEL =1

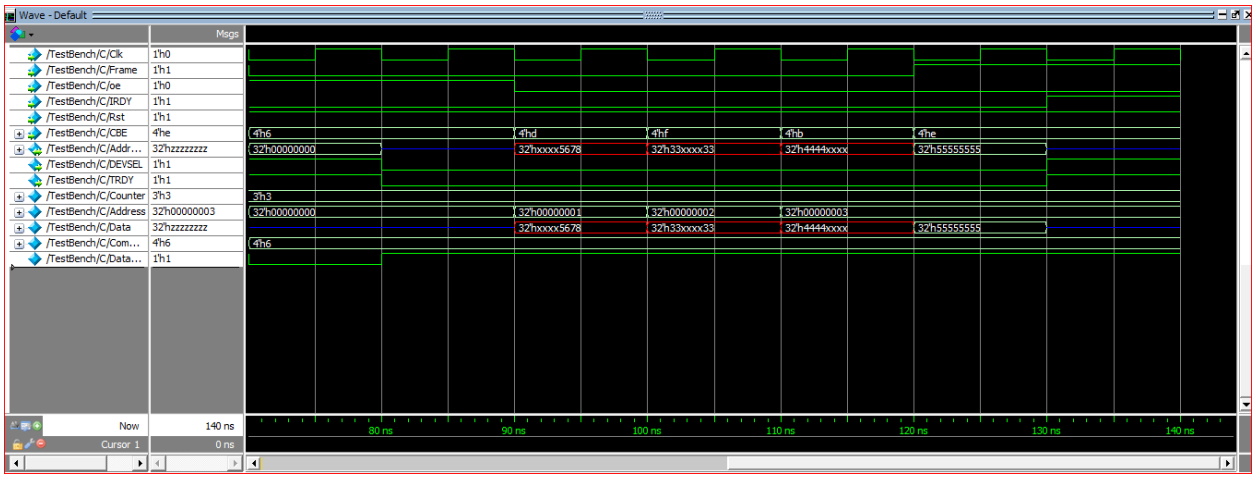

Figure 4: Reading the Data from the buffer from address zero

Note: In the read process we neglect the byte enable

8th Cycle:

- The Frame will be 0
- The Control line will be assigned by 4'b0110 which is assigned it to read command
- The address data line will be assigned by the first address we want to start reading from, which in our case 32'h00000000

9th Cycle:

- The initiator activates IRDY signal (IRDY=0)
- And the target will be ready to receive the address (TRDY & DEVSEL=0)
- But a turnaround cycle will occur before reading the data

10th Cycle:

- The Address data line will change from input to output(oe=0)
- The target starts to read from address 32'h00000000 the first data in the buffer which is 32'hXXXX5678

11th Cycle:

- The target will read from address 32'h00000001 the second data in the buffer which is 32'h33XXXX33

12th Cycle:

- The target will read from address 32’h00000002 the Third data in the buffer which is=32'h4444XXXX

13th Cycle:

- The target will read from address 32’h00000003 the Third data in the buffer which is=32'h55555555
- The Frame will be 1 because there is one last data to read

14th Cycle :

- The read transaction has ended
- Turnaround Cycle
- TRDY=1, DEVSEL=1, IRDY=1

Second scenario: (Write 4 data starting from address 3 & reading 4 words from address 2)

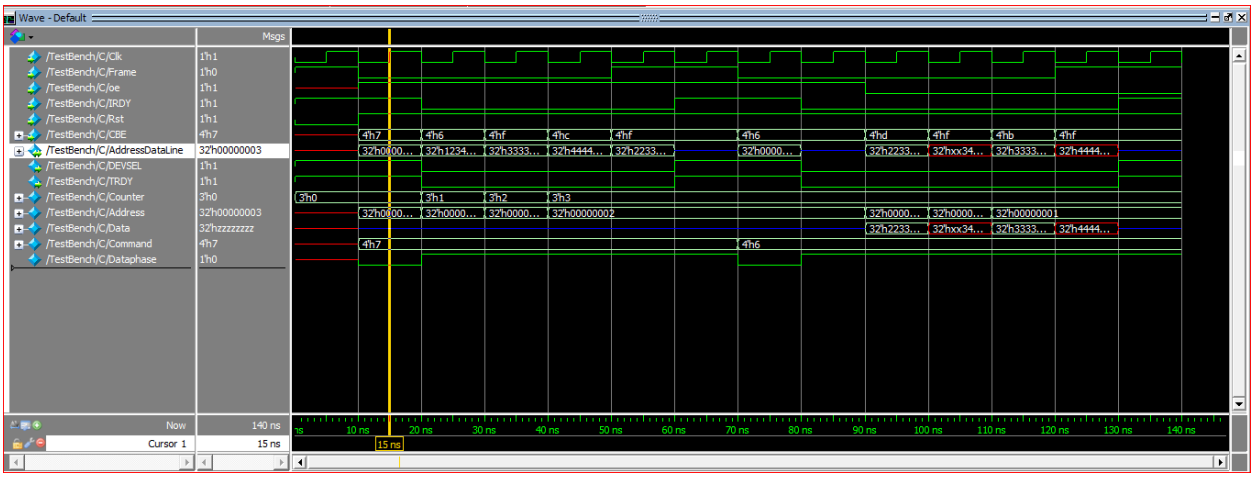

Figure 5: The full process of writing and reading 4 data starting from address not 0

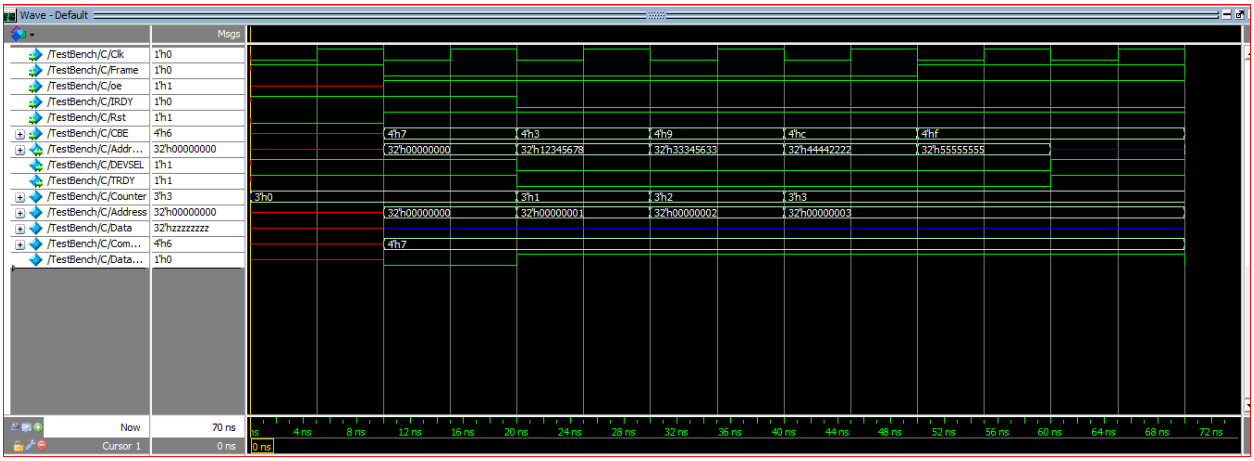

Figure 6: The full process of writing and reading 4 data starting from address 32’d3

Write Process:

1st Cycle :

- As we didn't initialize the address data line so in the first Clock cycle the address data line and the control line take (32'hX)
- (IRDY=1) ,Frame=1, TRDY and DEVSEL are still =1

2nd Cycle:

- We controlled the address data line to be an input signal to our target by using a flag which we named (oe) and it the address data line takes the value of the address which is 3
- And the frame will be 0 with the negative edge of clock cycle starting the write transaction
- At the same cycle, the control line takes the value of the write command which is assigned by (4'b0111)
- But the target is not ready yet to receive the data (TRDY=1 & DEVSEL=1)

3rd Cycle:

- The initiator is now ready to send the data (IRDY=0)
- Since we assume that our Target is (**FAST**), so our target will be ready to write the data (TRDY=0 & DEVSEL=0)

Then:

- The initiator starts to send the data to the target to be written starting by the data which will be written in the buffer starting from the data of address 32'd3.
- Then the target starts to write the first data in address 32'd3 in the buffer.
- And in every cycle the initiator sends new data and new byte enable.
- **Since our buffer is just 4 addresses so when the initiator sends the next data the target writes it in address 32'd0 as we don't have address called 32'd4**
- The next data received by the target, is written in the next address automatically as the address increment to write the new data in the buffer.
- The frame changed from 0 to1 then last data is written

- Then writing transaction is ended and a turnaround cycle occurs and (IRDY, TRDY & DEVSEL=1)

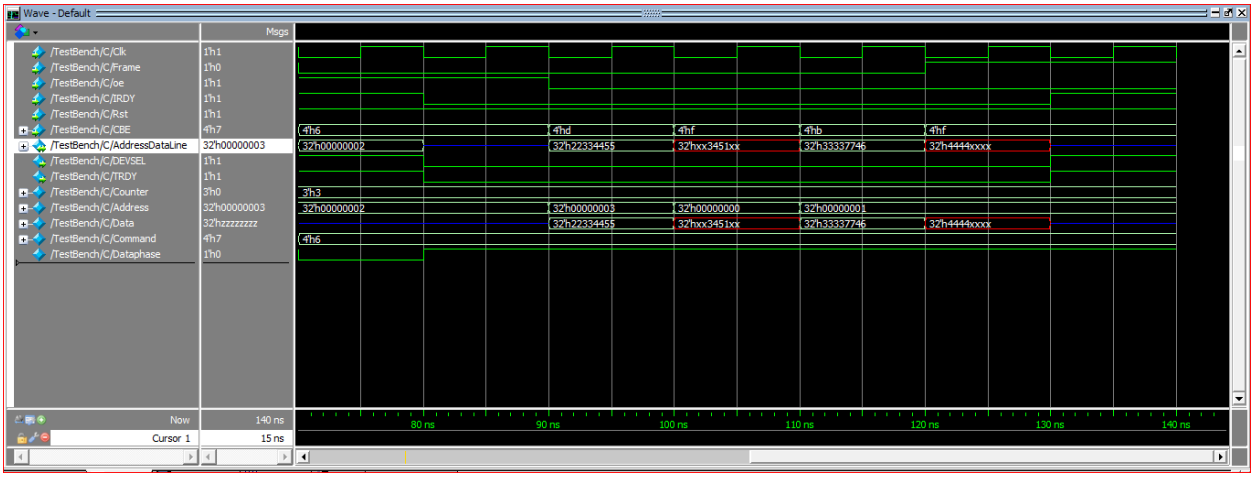

Figure 7: Reading the Data from the buffer from address 32'd2

Read Process:

- After the end of the write transaction and the turnaround cycle the frame changed from 1 to 0 as an indication for read transactions starting now .
- The initiator sends the command of read on control line which is =4'h6
- **And the initiator starts to send the address which is 32'd2 in our case which mean the target will start reading from the buffer from address 32'd2**
- So now the Target and the initiator are ready to receive and send data (IRDY=0,TRDY=0 &DEVSEL=0)
- And by each cycle the address which the target will read from is incremented
- New data is continued to be read until the address reaches 32'd3 which is the maximum address in the buffer, so the target starts to read from the first address in the buffer which is 32'd0
- The frame changed from 0 to1 then last data is read
- The reading transaction is ended, and a turnaround cycle occurs and (IRDY&TRDY&DEVSEL=1)

Third Scenario : ((IRDY=1):The IRDY is de-activated in the middle of the read transaction)

Figure 8: The full process of writing and reading 4 data starting but the initiator is interrupted in the middle

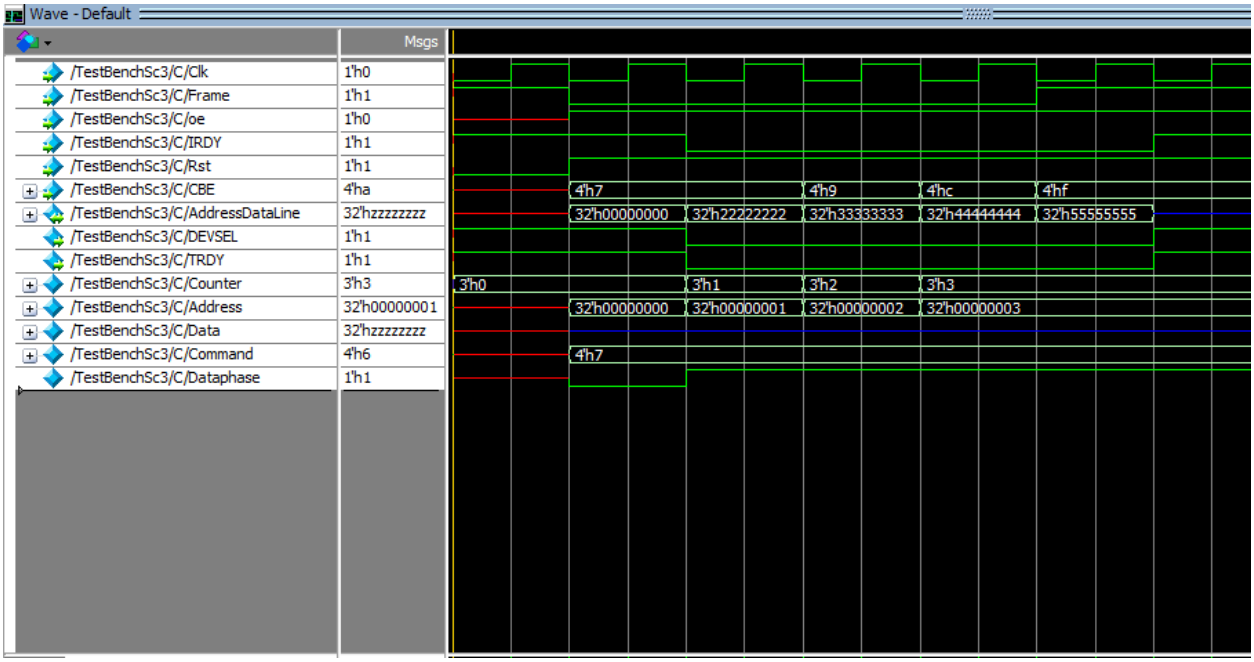

Figure 9: Writing 4 data in the buffer from address zero

Write Process:

1st Cycle :

- As we didn't initialize the address data line so in the first Clock cycle the address data line and the control line take (32'hX)
- (IRDY=1), Frame=1, TRDY and DEVSEl =1

2nd Cycle:

- we controlled the address data line to be an input signal to our target by using a flag which we named (oe) and it takes the value of the address which is 0 in this scenario and the control line take the value of the write command which is assigned by (4'b0111)
- And the frame will be 0 with the negative clock cycle as we start the write transaction
- But the target is not ready yet to receive the data (TRDY=1 & DEVSEL=1)

3rd Cycle:

- The initiator is now ready to send the data (IRDY=0)
- Since we assume that our Target is (**FAST**), so our target will be ready to write the data (TRDY=0 & DEVSEL=0)

Then:

- The initiator starts to send the data to the target to be written starting by the data which will be written in the buffer starting from the data of address 32'd0.
- The target starts to write the first data in address 32'd0 .
- In every cycle the initiator sends new data and new byte enable and the address is incremented by 1 so the next data received by the target is written in the next address automatically
- The frame changed from 0 to1 then last data is written
- The writing transaction is ended, and a turnaround cycle occurs and (IRDY, TRDY & DEVSEL=1)

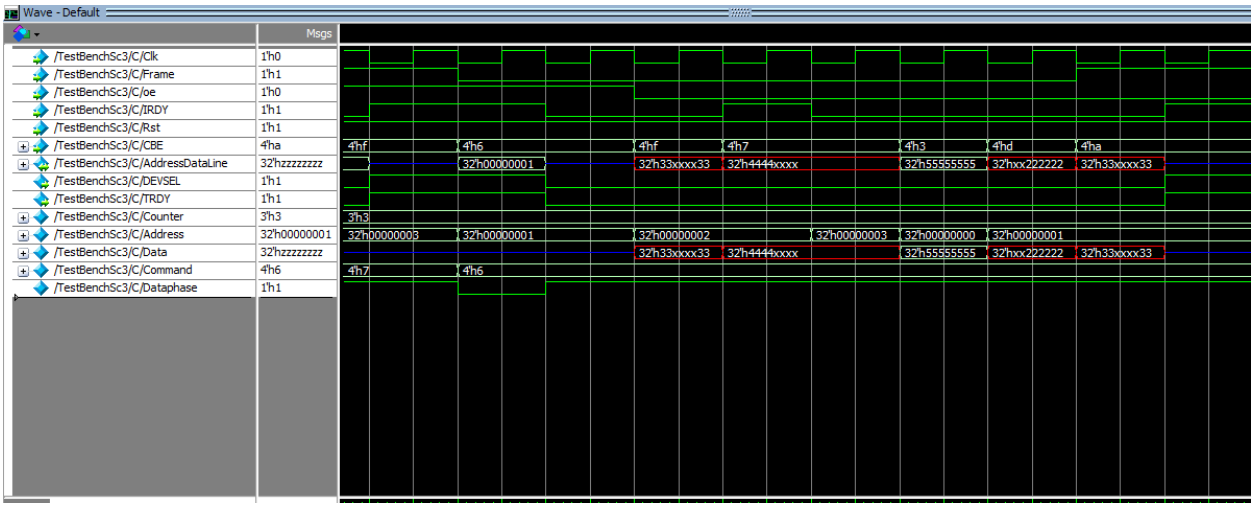

Figure 10: Reading the Data and the IRDY=1in the middle

Read Process:

- After the end of the write transaction and the turnaround cycle the frame changed from 1 to 0 as an indication for read transactions starting now.
- The initiator sends the command of read on control line which is =4'h6
- The initiator starts to send the address which is 32'd1 in our case which mean the target will start reading from the buffer from address 32'd1
- So now the Target and the initiator are ready to receive and send data (IRDY=0, TRDY=0 & DEVSEL=0)
- And by each cycle the address which the target will read from in the buffer is incremented

In the 11th Cycle :

- **IRDY is de-activated (IRDY=1) so the data remains for an extra cycle until the next data sent.**

Then:

- New data is continued to be read until the address reaches 32'd3 which is the maximum address in the buffer, so the target starts reading from 32'd0
- The frame changed from 0 to1 then last data is read
- Then reading transaction is ended and a turnaround cycle occurs and (IRDY, TRDY & DEVSEL=1)

Fourth scenario: (Writing more than 4 words which is the total memory of the buffer which leads to make the TRDY=1 in the middle of the write transection)

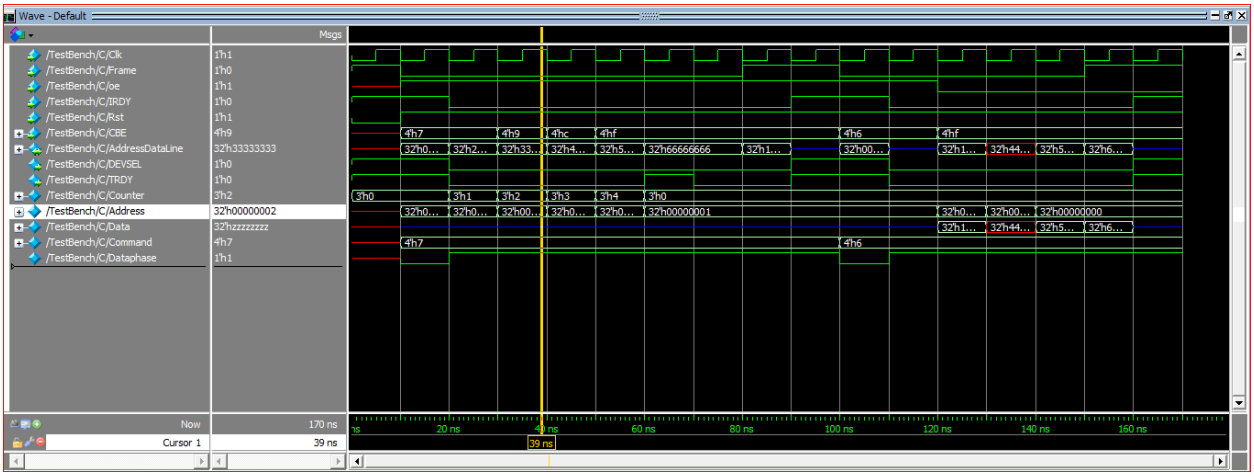

Figure 11: The full process of writing more than 4 data and reading 4 words (TRDY=1in the middle)

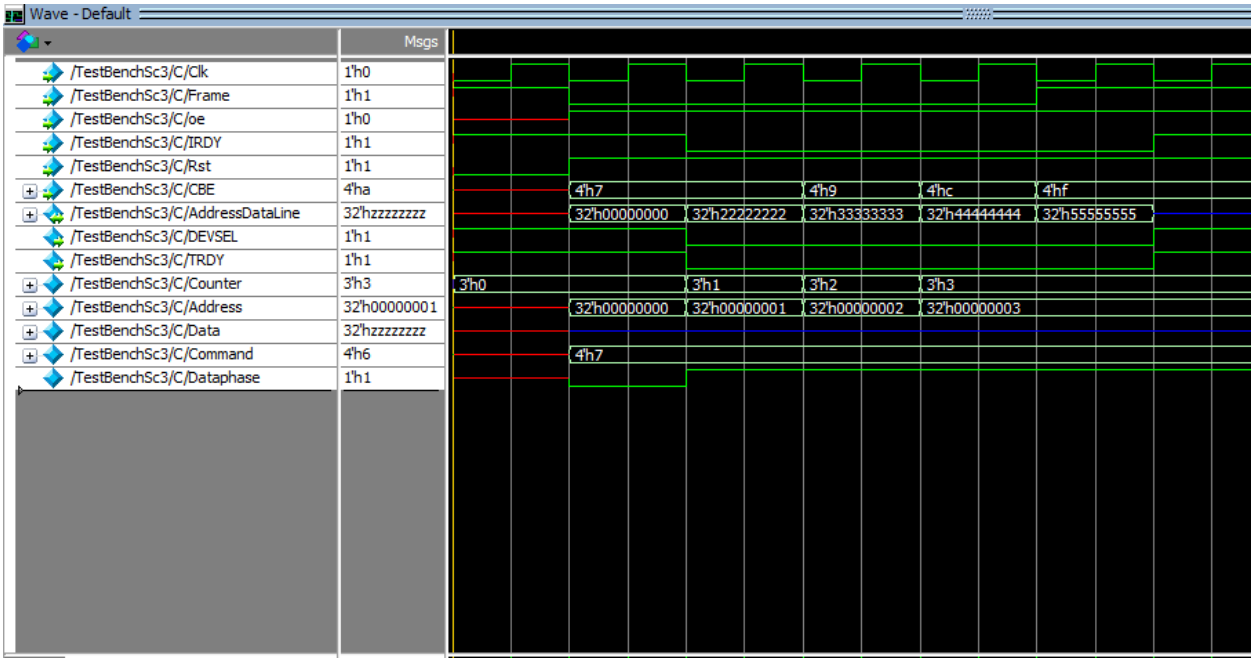

Figure 12: Writing more than 4 data in the buffer from address zero (TRDY=1in the middle)

Write Process:

1st Cycle :

- As we didn't initialize the address data line so in the first Clock cycle the address data line and the control line takes (32'hX)
- (IRDY=1), Frame=1, TRDY and DEVSEl =1

2nd Cycle:

- we controlled the address data line to be an input signal to our target by using a flag which we named (oe) and it takes the value of the address which is 0 in this scenario and the control line take the value of the write command which is assigned by (4'b0111)
- And the frame will be 0 with the negative clock cycle as we start the write transection
- But the target is not ready yet to receive the data (TRDY=1 & DEVSEL=1)

3rd Cycle:

- The initiator is now read to send the data (IRDY=0)
- since we assume that our Target is (**FAST**), so our target will be ready to write the data (TRDY=0 & DEVSEL=0)

Then:

- The initiator starts to send the data to the target to be written starting by the data which will be written in the buffer starting from the data of address 32'd0 .
- In every cycle the initiator sends new data and new byte enable and the address is incremented by 1 so the next data received by the target is written in the next address automatically
- Until the initiator sent more than 4 addresses, **so all the data in the buffer "the memory which the target write in it "transfer to a larger memory in the system called "MEMORY"**
  *** Note:(Our buffer is designed to store only 4 data , but in this case the initiator sent two extra data , so prevent the overwrite we transfer the data from the buffer to another big memory called (MEMORY) it can store till 6 addresses)**
- At the same time the data is transferring TRDY will be =1 for one cycle which means it cannot receive any data this time
- After one cycle , now the buffer can receive any data
- And TRDY returns 0
- so the target can write 32'h66666666 & 32'h11111111
- The frame changed from 0 to 1 then last data is written

- Then writing transaction is ended and a turnaround cycle occurs and (IRDY&TRDY&DEVSEL=1)

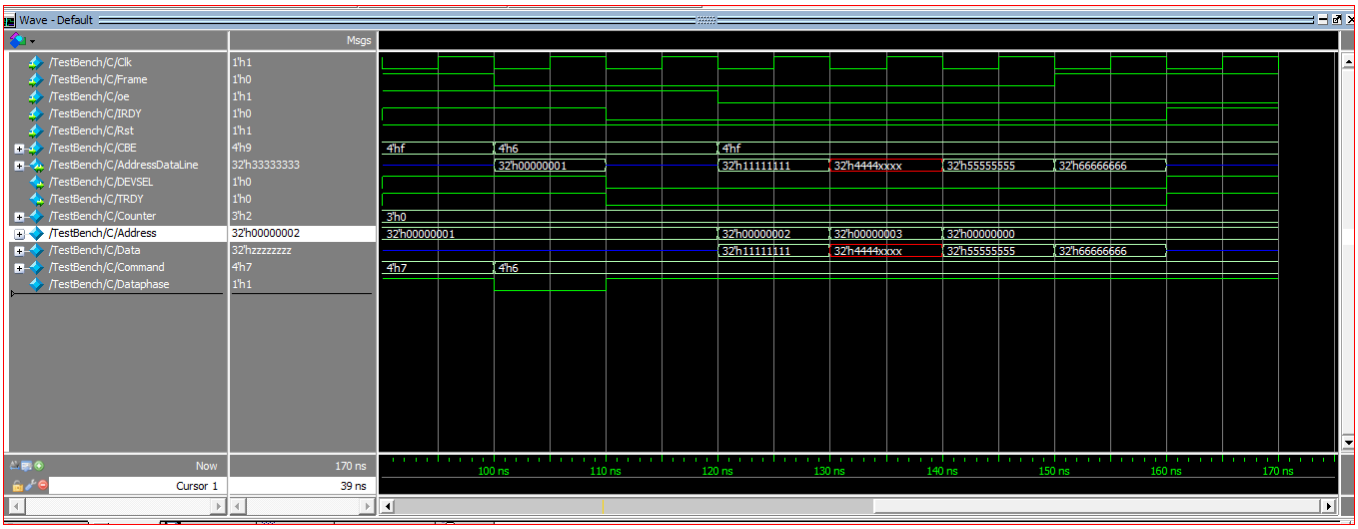

Figure 13: Reading the Data from the buffer from address 1

Read Process:

- After the end of the write transaction and the turnaround cycle the frame changed from 1 to 0 as an indication for read transactions starting now .
- And the initiator send the command of read on control line which is =4'h6
- And the initiator start to send the address which is 32'd1 in our case which mean the target will start reading from the buffer from address 32'd1
- So now the Target and the initiator are ready to receive and send data (IRDY=0, TRDY=0 & Devsel=0)
- And by each cycle the address which the target will read from in the buffer is increment
- And new data is reed until the address reaches 32'd3 which is the maximum address in the buffer, so the target start to read from the first address in the buffer which is 32'd0
- The frame changed from 0 to1 then the last data is read
- The reading transaction is ended, and a turnaround cycle occurs and (IRDY, TRDY & DEVSEL=1)

Fifth Scenario: (Write 4 data starting from address 2& reading 5 words from address location 1)

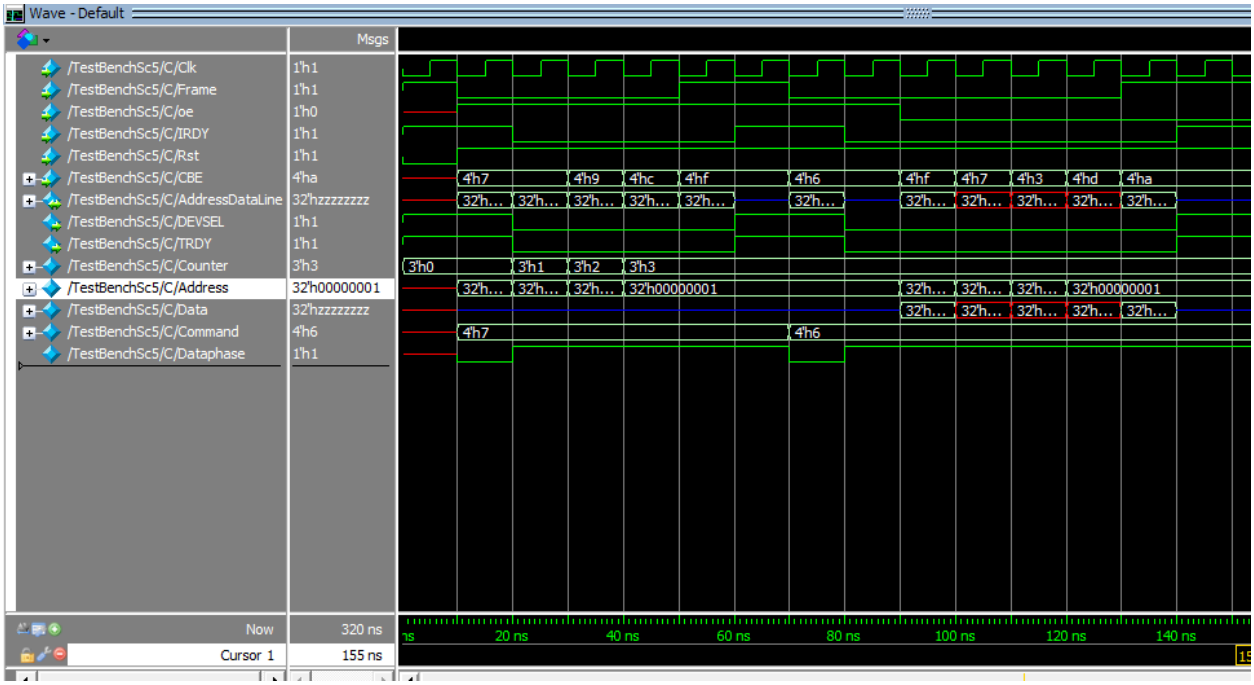

Figure 14: The full process of writing 4 data from address 2 and reading 5 data starting from address 1

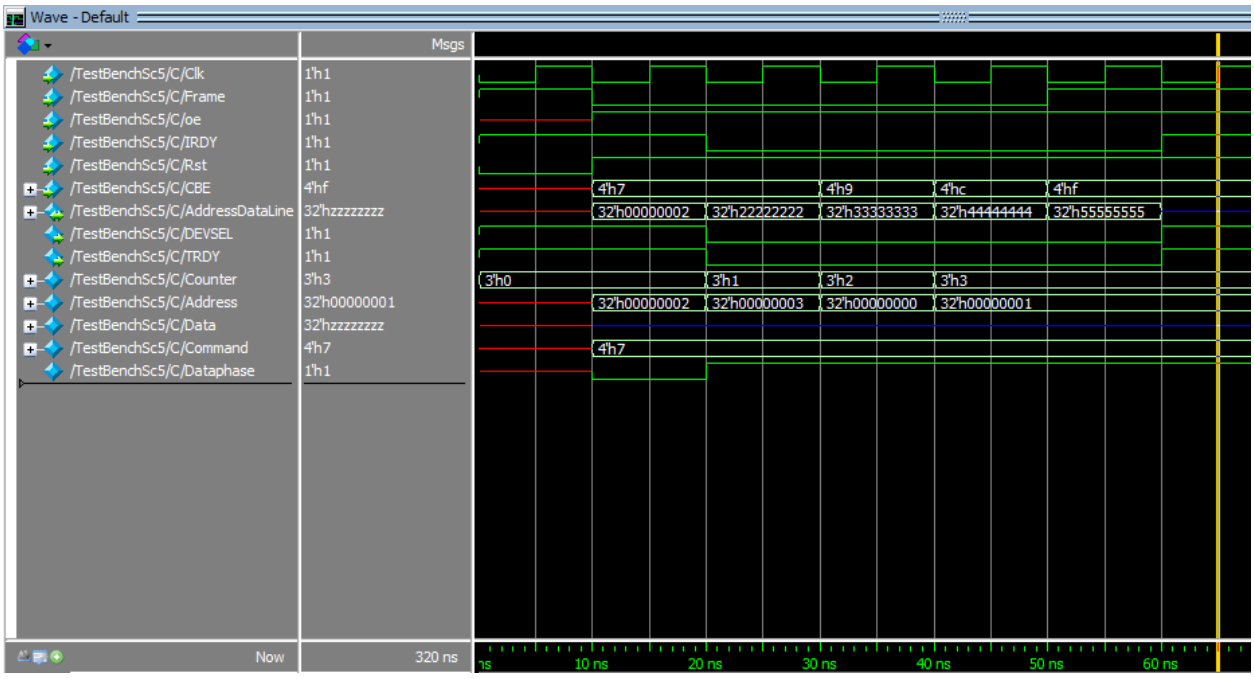

Figure 15: Writing 4 data in the buffer from address 32'd2

Write Process:

1st Cycle :

- As we didn't initialize the address data line so in the first Clock cycle the address data line and the control line takes (32'hX)
- (IRDY=1), Frame=1, TRDY and DEVSEl =1

2nd Cycle:

- we controlled the address data line to be an input signal to our target by using a flag which we named (oe) and it takes the value of the address which is 2 in this scenario and the control line take the value of the write command which is assigned by (4'b0111)
- And the frame will be 0 with the negative clock cycle as we start the write transection
- But the target is not ready yet to receive the data (TRDY=1&DEVSEL=1)

3rd Cycle:

- The initiator is now read to send the data (IRDY=0)
- since we assume that our Target is (**FAST**), so our target will be ready to write the data (TRDY=0&DEVSEL=0)

Then:

- The initiator starts to send the data to the target to be written starting by the data which will be written in the buffer starting from the data of address 32'd0 .
- In every cycle the initiator sends new data and new byte enable and the address is incremented by 1 so the next data received by the target is written in the next address automatically
- The frame changed from 0 to1 then last data is written
- Then writing transaction is ended and a turnaround cycle occurs and (IRDY&TRDY&DEVSEL=1)

Figure 16: Reading the Data from the buffer from address 1

Read Process:

- After the end of the write transaction and the turnaround cycle the frame changed from 1 to 0 as an indication for read transactions starting now .
- The initiator sends the command of read on control line which is =4'h6
- The initiator starts to send the address which is 32'd1 in our case which mean the target will start reading from the buffer from address 32'd1
- So now the Target and the initiator are ready to receive and send data (IRDY=0, TRDY=0 &DEVSEL=0)
- And by each cycle the address which the target will read from in the buffer is increment
- And new data is read until the address reaches 32'd3 which is the maximum address in the buffer, so the target start to read from 32'd0
- The frame changed from 0 to1 then the last data is read
- The reading transaction is ended, and a turnaround cycle occurs and (IRDY&TRDY&DEVSEL=1)

6th Scenario: (Sending address greater than 3. So this data is not to our target)

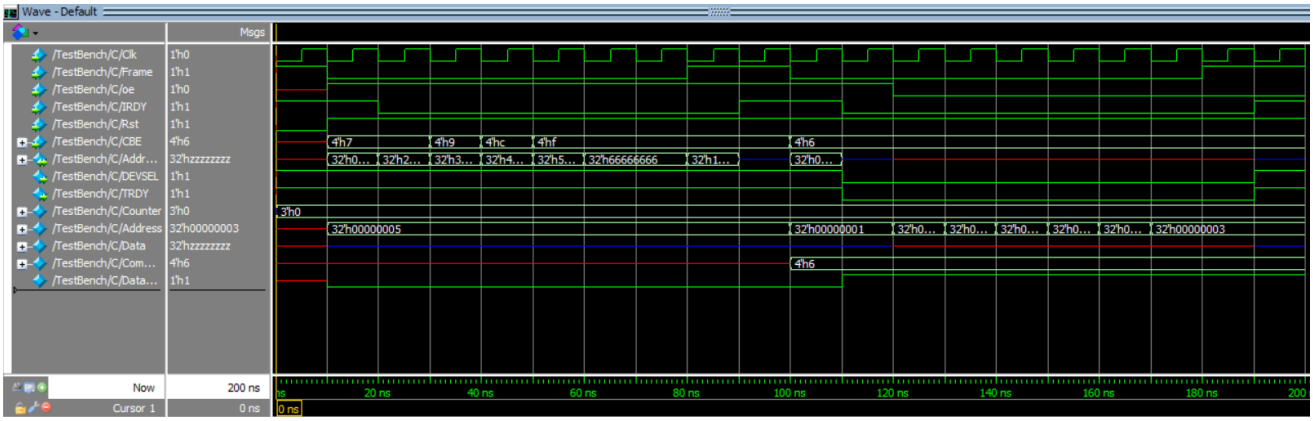

Figure 17: The full process of writing and reading when the address sent is bigger than the buffer size

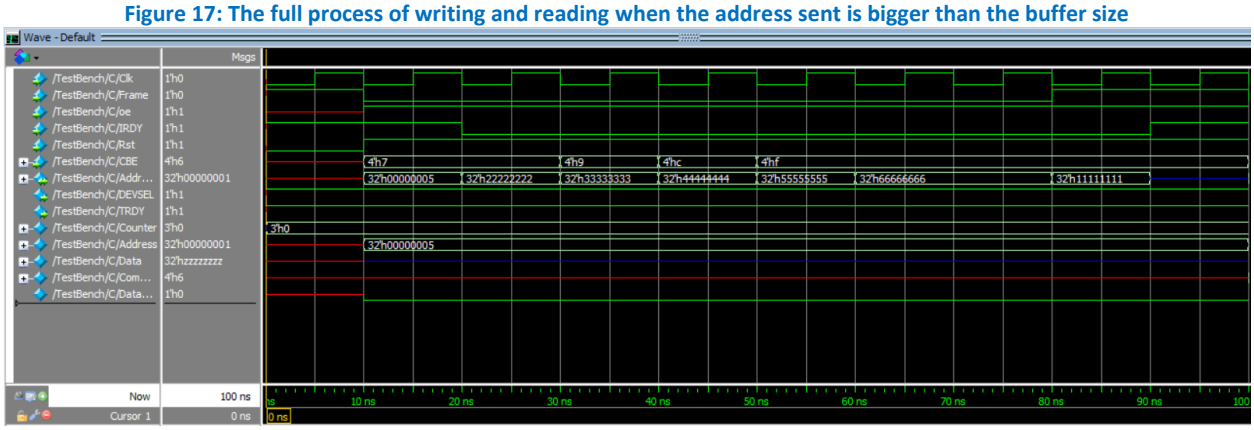

Figure 18: No Writing occurs in the buffer

Write Process:

1st Cycle :

- As we didn't initialize the address data line so in the first Clock cycle the address data line and the control line takes (32'hX)
- (IRDY=1), Frame=1, TRDY and DEVSEl =1

2nd Cycle:

- we controlled the address data line to be an input signal to our target by using a flag which we named (oe) and it takes the value of the address which is 5 in this scenario and the control line take the value of the write command which is assigned by (4'b0111)

- And the frame will be 0 with the negative clock cycle as we start the write transaction
- But the target is not ready yet to receive the data (TRDY=1&DEVSEL=1)

Since the address which the initiator sent to the target is out of its range (as our target range is from 0 to 3)

The DEVSEL & TRDY will remain not ready (=1)

And that's mean that the initiator is sending this data to another target

- As the writing transaction is ended.
- And a turnaround cycle occurs

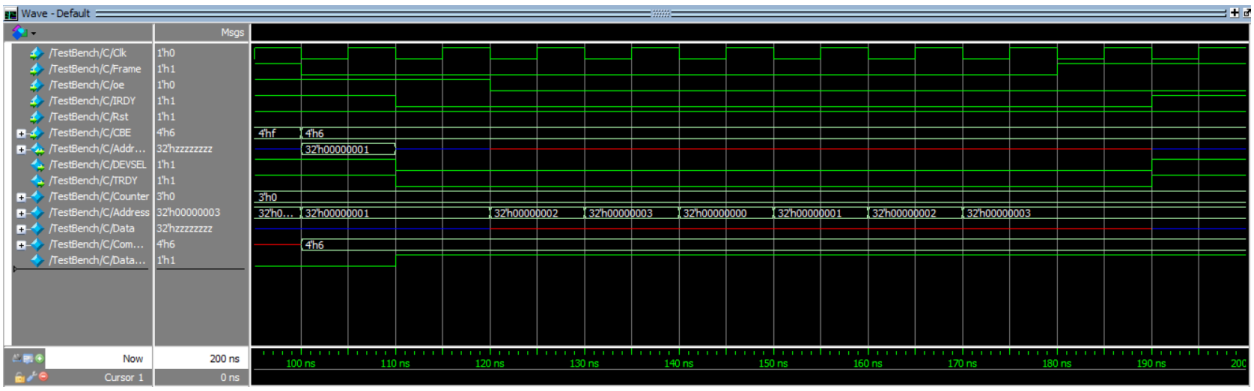

Figure 19: Reading 32'hX from the buffer from address zero

Read Process:

- After the end of the write transaction and the turnaround cycle the frame changed from 1 to 0 as an indication for read transactions starting now .
- The initiator sends the command of read on control line which is =4'h6
- The initiator starts to send the address which is 32'd1 in our case which mean the target will start reading from the buffer from address 32'd1
- So now the Target and the initiator are ready to receive and send data (IRDY=0,TRDY=0 &Devsel=0)
- And by each cycle the address which the target will read from in the buffer is increment
- But since the buffer which I am reading from it is empty as the address in the write transaction wasn't for my target therefore I will read 32'hX

7th Scenario : (Making 3 Transitions (1st write 4 data from address 2, 2nd write 4 words Starting in address 1 , Read 5 words from the buffer starting from address 1)

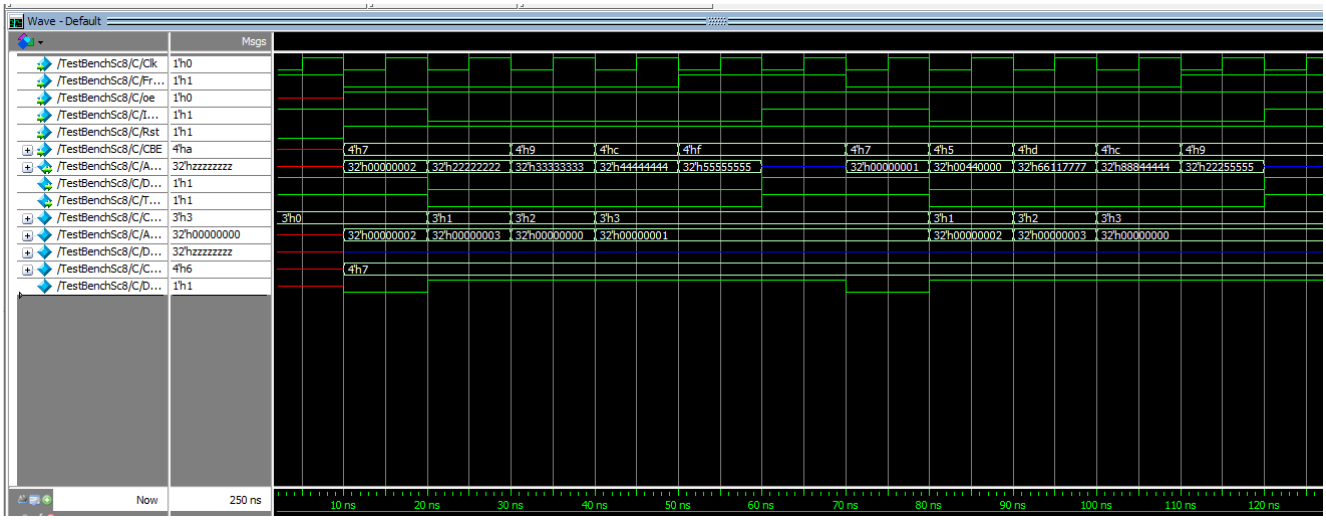

Figure 20: Writing 4 data in the buffer starting from address 2 Then writing data in the buffer starting from address 1

2nd Write Process:

- After the end of the 1st write transaction and the turnaround cycle the frame changed from 1 to 0 as an indication for 2nd write transaction is going to start .
- The initiator sends the command of write again in this scenario on control line which is =4'h7
- The initiator starts to send the address which is 32'd1 in our case which mean the target will start writing in the buffer in address 32'd1
- But since our buffer is already full by data which the target writes the last transaction
- So, the data will transfer from the buffer which can just store 4 words to the Memory which can store till 6 words
- So now the Target and the initiator are ready to receive and send data (IRDY=0,TRDY=0 &Devsel=0)
- So now the target can start writing in the buffer in address 32'd1
- And by each cycle the address which the target will write in the buffer is increment

- And in every cycle the initiator sends new data and new byte enable which choose the bytes which we need to write from this data .
- The frame changed from 0 to1 then last data is written
- Then writing transaction is ended and a turnaround cycle occurs and (IRDY&TRDY&DEVSEL=1)

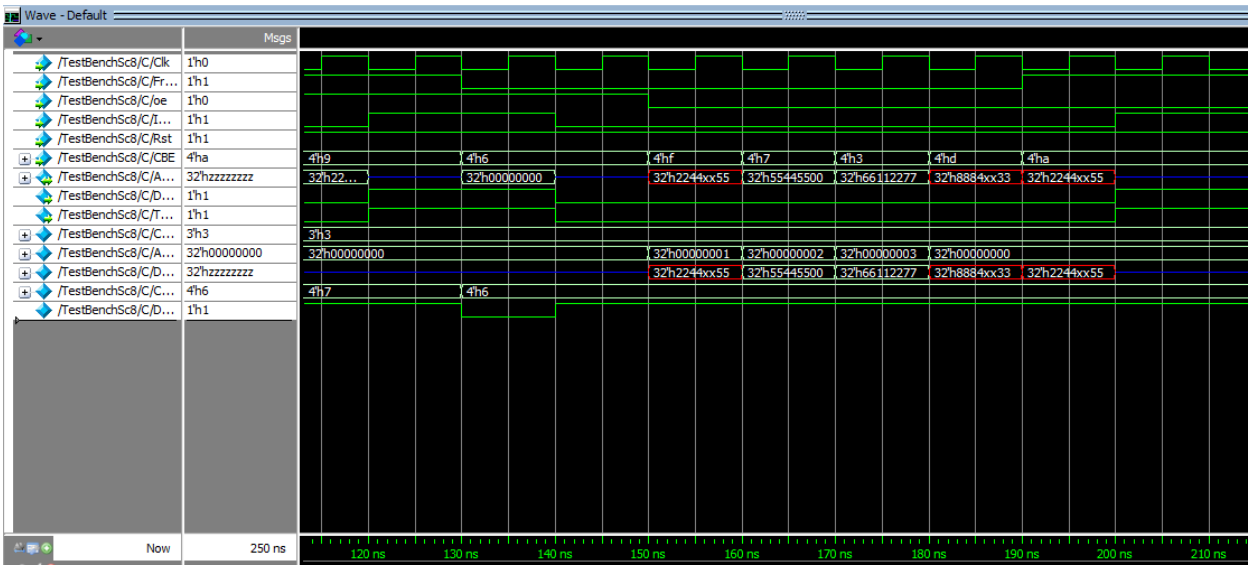

Figure 21: Reading the Data from the buffer from address zero

Read Process:

- After the end of the 2nd write transaction and the turnaround cycle the frame changed from 1 to 0 as an indication for read transactions starting now .
- And the initiator send the command of read on control line which is =4'h6
- And the initiator start to send the address which is 32'd0 in our case which mean the target will start reading from the buffer from address 32'd0
- So now the Target and the initiator are ready to receive and send data (IRDY=0,TRDY=0 &Devsel=0)
- And by each cycle the address which the target will read from in the buffer is increment
- And new data is reed until the address reaches 32'd3 which is the maximum address in the buffer so the target start to read from the first address in the buffer he start reading from the first time which is 32'd1
- And in our scenario the buffer store the written data in the 2nd write transaction so we will read the words stored in the 2nd write transaction
- The frame changed from 0 to1 then the last data is read

- The reading transaction is ended, and a turnaround cycle occurs and (IRDY&TRDY&DEVSEL=1)

8th Scenario:

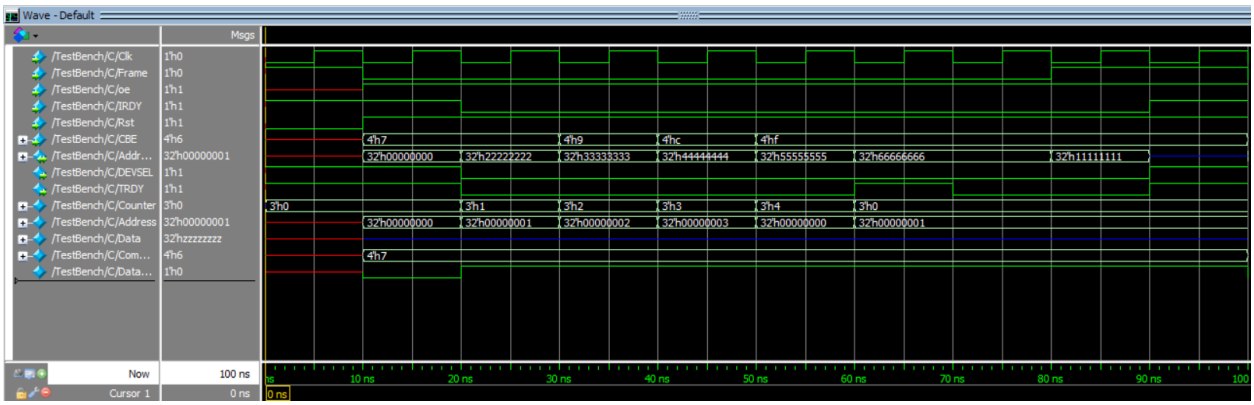

Figure 22: Writing more than 4 data in the buffer from address 32'd0 (TRDY=1 in the middle)

Write Process:

1st Cycle :

- As we didn't initialize the address data line so in the first Clock cycle the address data line and the control line takes (32'hX)
- (IRDY=1), Frame=1, TRDY and DEVSEl =1

2nd Cycle:

- we controlled the address data line to be an input signal to our target by using a flag which we named (oe) and it takes the value of the address which is 0 in this scenario and the control line take the value of the write command which is assigned by (4'b0111)
- And the frame will be 0 with the negative clock cycle as we start the write transaction
- But the target is not ready yet to receive the data (TRDY=1&DEVSEL=1)

3rd Cycle:

- The initiator is now ready to send the data (IRDY=0)
- since we assume that our Target is (**FAST**), so our target will be ready to write the data (TRDY=0&DEVSEL=0)

Then:

- The initiator starts to send the address to the target to write to it in this scenario the initiator starts sending the data from address 32’d0.
- Then the target starts to write the first data in address 32’d0 .
- In every cycle the initiator sends new data and new byte enable and the address is incremented by 1 so the next data received by the target is written in the next address automatically
- Until the initiator sent more than 4 addresses , so all the data in the buffer “the memory which the target write in it ”transfer to a larger memory in the system called "MEMORY"
  * Note:(Our buffer is designed to store only 4 data , but in this case the initiator sent two extra data , so prevent the overwrite we transfer the data from the buffer to another big memory called (MEMORY) it can store till 6 addresses)
- **At the same time the data is transferring TRDY will be =1 for one cycle which means it can’t receive any data this time**
- After one cycle , now the buffer can receive any data
- And TRDY returns 0
- so the target can write32’h66666666 &32’h11111111
- until the initiator is sending the last data the Frame change from 0 to 1.
- As the writing transaction is ended.
- And a turnaround cycle occurs
- And after the last data is sent (IRDY&TRDY&DEVSEL=1)

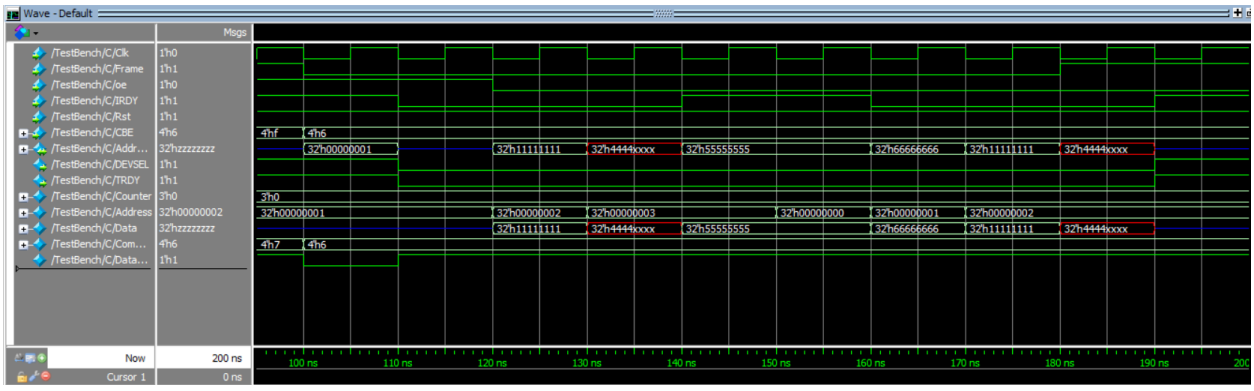

Figure 23: Reading the Data and the IRDY=1in the middle

Read Process:

- After the end of the write transaction and the turnaround cycle the frame changed from 1 to 0 as an indication for read transactions starting now.
- And the initiator sends the command of read on control line which is =4’h6

- And the initiator starts to send the address which is 32'd1 in our case which mean the target will start reading from the buffer from address 32'd1
- So now the Target and the initiator are ready to receive and send data (IRDY=0,TRDY=0 &Devsel=0)
- And by each cycle the address which the target will read from in the buffer is increment

In the 15th Cycle :

- **In our case the initiator wasn't ready for sending the address so the IRDY=1**
- **The data remain for an extra cycle until the next data sent.**

Then:

- And new data is read until the address reaches 32'd3 which is the maximum address in the buffer, so the target start to read from the first address in the buffer which is 32'd0
- The frame changed from 0 to1 then the last data is read
- The reading transaction is ended, and a turnaround cycle occurs and (IRDY&TRDY&DEVSEL=1)

4. Additional information.

- We added scenario, when IRDY gets deactivated in the middle of the read proccess (IRDY =1).
- We added scenario, when Initiator sends six data so target makes TRDY gets deactivated for one cycle in the middle of the write proccess (TRDY =1).
- We added reset to the target.

5. Contribution of each member.

Name	Contribution
Hebat-Allah Atef Ahmed	• Implementation of Target Module • Implementation of Test Bench • Implementation of different test cases • Documentation of table of contents • Documentation of Description of all signals
Nora Nabil Ali	• Implementation of Target Module • Implementation of Test Bench • Implementation of different test cases • Documentation of table of figures • Documentation of Brief description for different read/write scenarios associated with waveform screenshots
Nehal Yasser Abd El-Wahab	• Implementation of Target Module • Implementation of Test Bench • Implementation of different test cases • Documentation of Block Diagram • Documentation of Contribution of each member
Nermeen Atef Abdel Karim	• Implementation of Target Module • Implementation of Test Bench • Implementation of different test cases • Inout AddressData line • Documentation of additional information • Documentation of Contribution of each member