

Sayısal Sistemler-H1CD1

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versiyon021024

Yoklama Konusu

Bu Derste Devam Zorunluluđu Yoktur !

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Dersin Adı : Sayısal Sistemler (2+0)

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Dersin Amacı

- Bu ders öğrencilere sayısal sistemlerin mantıksal tasarımını öğretmeyi amaçlamaktadır.
- Bu kapsamda sayı sistemleri, Bool cebri ve işlem kuralları, kombinasyonel lojik devreler ve tasarımı, ardışıl devre elemanları, senkron ve asenkron ardışıl devrelerin tasarımı, hafıza devrelerinin yapıları anlatılacaktır.
- Bu dersin sonunda öğrencinin sayısal bir sistemi çözümlemesi ve ihtiyaç duyulan bir sayısal sistemi maliyeti en düşük olacak şekilde tasarlaması beklenmektedir.

Ders İçeriği

- Temel bilgiler
- Sayı Sistemleri: İkili sayılar, sayı tabanları arasında dönüşüm, farklı sayı sistemlerinde aritmetik işlemler,
- Birleşik Mantık Devreleri: ikili mantık, mantıksal kapılar,
- Bool cebri, mini-terimler ve maks-terimler, iki, üç ve dört değişkenli haritalama, çok seviyeli devre optimizasyonu.
- Birleşik fonksiyonlar ve devreler: birleşik devreler,
- Kodlayıcı tasarımları, kod çözücü tasarımları, çoklayıcı tasarımları,
- Aritmetik fonksiyonlar ve devreler: ikili toplayıcılar, yarı-tam toplayıcılar, çıkarıcılar, çoğullayıcılar, tekilleştiriciler, 1 bitlik saklayıcılar
- Flip-flop'ların çalışması, SR-RS flip flop'lar, T tipi flip-flop'lar, D tipi flip-flop'lar, JK tipi flip flop'lar,
- Sayıcılar, saklayıcılar, ALU tasarımı
- Karmaşık ardışıl lojik devre tasarım örnekleri uygulamaları

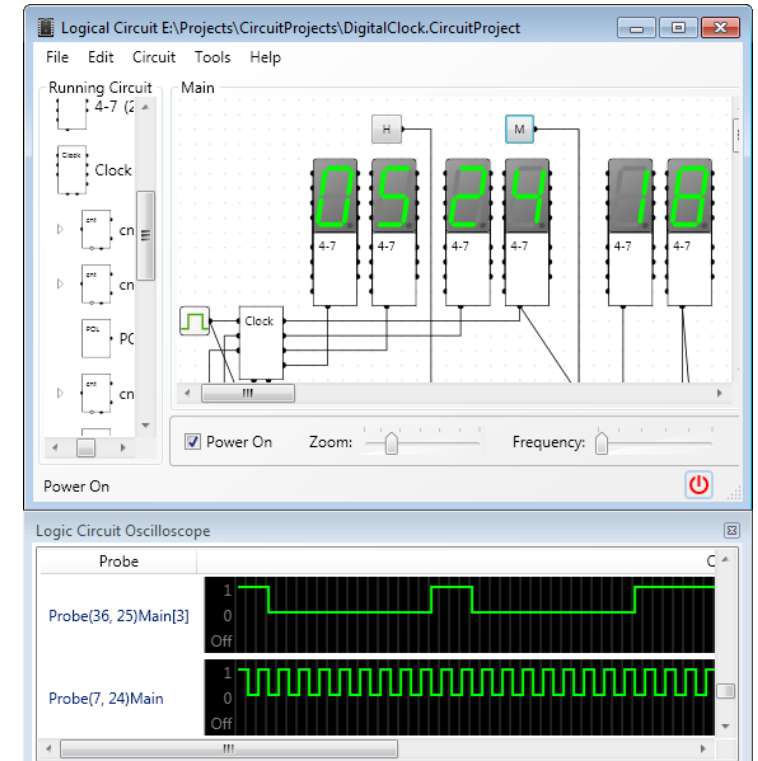
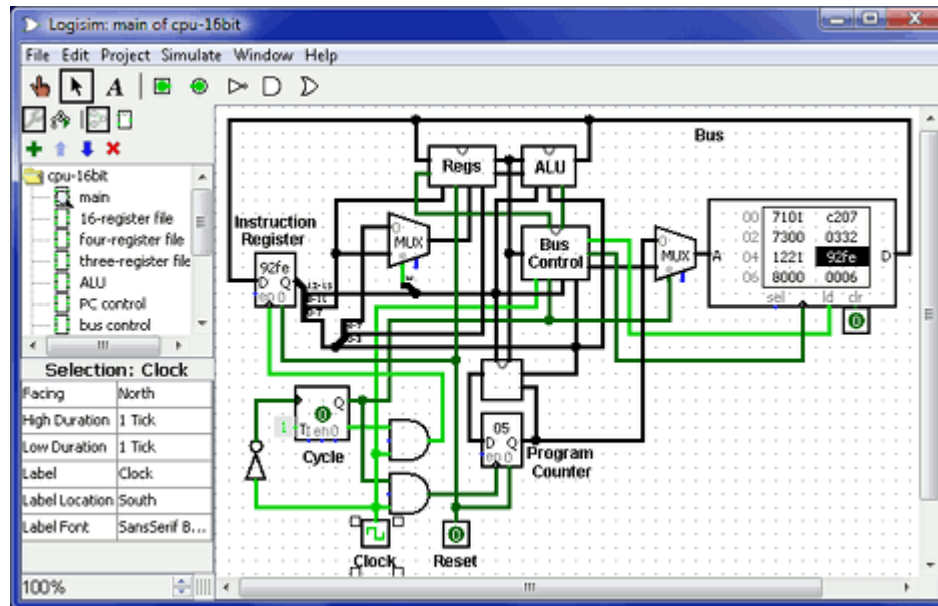
Ön Şartlar

- Temel Mantık Bilgisi
- Analiz ve Muhakeme Yeteneği
- Beyin Kas Koordinasyonu
- Programlama ve Tasarım Becerisi
 - Simulator kullanımı için



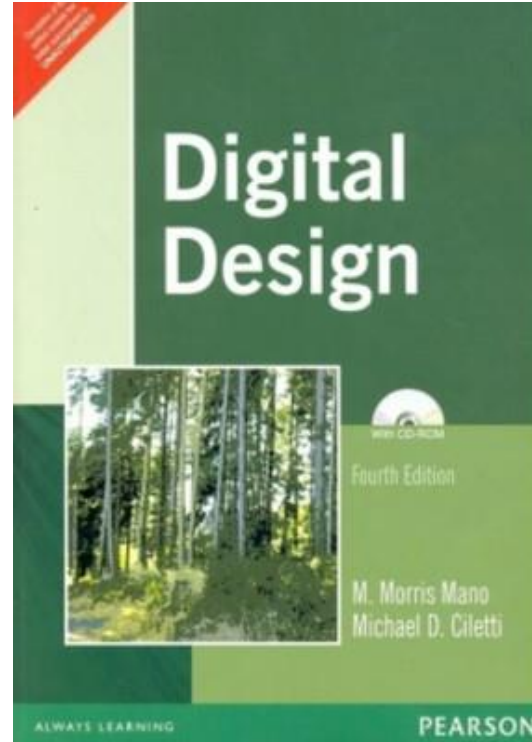
Simulator Alternatiflerini inceleyelim

- <https://circuitverse.org/simulator>
- <https://logic.ly/demo/samples>
- <http://www.cburch.com/logisim/>



Kaynaklar

- “**Digital Design**”, M. Morris Mano
- “**Sayısal Tasarım**”, M. Morris Mano (Türkçe çevirisi)



Konu Başlıkları

“Digital Design”, M. Morris Mano

Digital Systems and Binary Numbers

- 1.1 Digital Systems
- 1.2 Binary Numbers
- 1.3 Number-Base Conversions
- 1.4 Octal and Hexadecimal Numbers
- 1.5 Complements of Numbers
- 1.6 Signed Binary Numbers
- 1.7 Binary Codes
- 1.8 Binary Storage and Registers
- 1.9 Binary Logic

Boolean Algebra and Logic Gates

- 2.1 Introduction
- 2.2 Basic Definitions
- 2.3 Axiomatic Definition of Boolean Algebra
- 2.4 Basic Theorems and Properties of Boolean Algebra
- 2.5 Boolean Functions
- 2.6 Canonical and Standard Forms
- 2.7 Other Logic Operations
- 2.8 Digital Logic Gates
- 2.9 Integrated Circuits

Gate-Level Minimization

- 3.1 Introduction
- 3.2 The Map Method
- 3.3 Four-Variable K-Map
- 3.4 Product-of-Sums Simplification
- 3.5 Don't-Care Conditions
- 3.6 NAND and NOR Implementation
- 3.7 Other Two-Level Implementations
- 3.8 Exclusive-OR Function
- 3.9 Hardware Description Language

Combinational Logic

- 4.1 Introduction
- 4.2 Combinational Circuits
- 4.3 Analysis Procedure
- 4.4 Design Procedure
- 4.5 Binary Adder-Subtractor
- 4.6 Decimal Adder
- 4.7 Binary Multiplier
- 4.8 Magnitude Comparator
- 4.9 Decoders
- 4.10 Encoders
- 4.11 Multiplexers
- 4.12 HDL Models of Combinational Circuits

Konu Başlıkları

“Digital Design”, M. Morris Mano

Synchronous Sequential Logic

- 5.1 Introduction
- 5.2 Sequential Circuits
- 5.3 Storage Elements: Latches
- 5.4 Storage Elements: Flip-Flops
- 5.5 Analysis of Clocked Sequential Circuits
- 5.6 Synthesizable HDL Models of Sequential Circuits
- 5.7 State Reduction and Assignment
- 5.8 Design Procedure

Registers and Counters

- 6.1 Registers
- 6.2 Shift Registers
- 6.3 Ripple Counters
- 6.4 Synchronous Counters
- 6.5 Other Counters
- 6.6 HDL for Registers and Counters

Memory and Programmable Logic

- 7.1 Introduction
- 7.2 Random-Access Memory
- 7.3 Memory Decoding
- 7.4 Error Detection and Correction
- 7.5 Read-Only Memory
- 7.6 Programmable Logic Array
- 7.7 Programmable Array Logic
- 7.8 Sequential Programmable Devices

Design at the Register Transfer Level

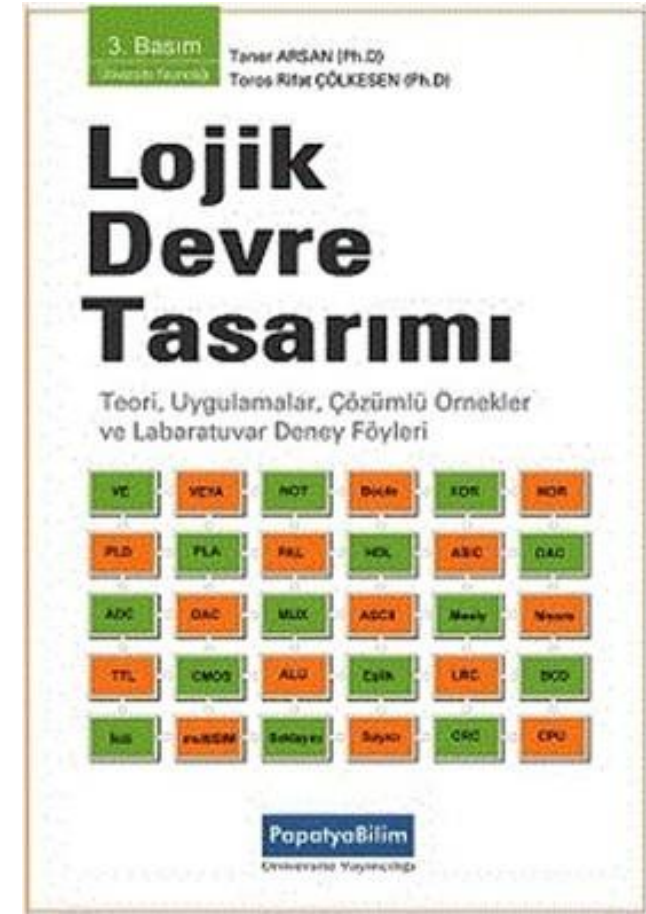
- 8.1 Introduction
- 8.2 Register Transfer Level Notation
- 8.3 Register Transfer Level in HDL
- 8.4 Algorithmic State Machines (ASMs)
- 8.5 Design Example (ASMD Chart)
- 8.6 HDL Description of Design Example
- 8.7 Sequential Binary Multiplier
- 8.8 Control Logic
- 8.9 HDL Description of Binary Multiplier
- 8.10 Design with Multiplexers
- 8.11 Race-Free Design (Software Race Conditions)
- 8.12 Latch-Free Design (Why Waste Silicon?)
- 8.13 Other Language Features

Kaynaklar

- “Lojik Devre Tasarımı”, Rifat Çölkesen, Taner Arsan

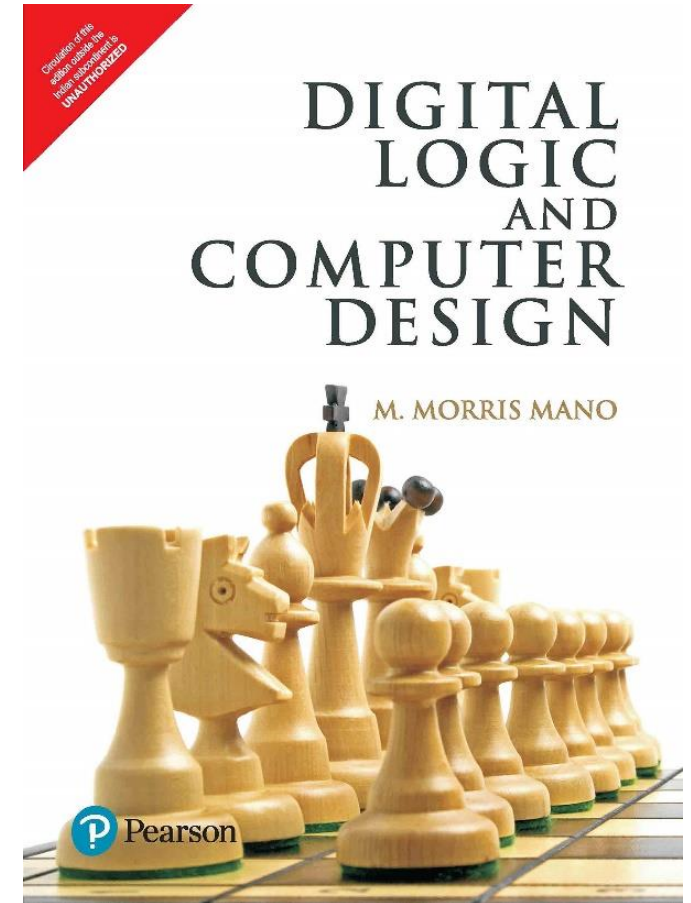
Kitap içerisinde aşağıdaki konular ele alınmış olup Lojik Devre laboratuvarı için de 10 tane deney önerisi verilmiştir:

- Lojik Devre Tasarımı Dünyası
- İşaretler ve Analog / Sayısal Dönüşüm
- Sayı Sistemleri
- Kodlama Teknikleri
- Lojik Devre Temelleri
- Boole Cebri
- Lojik Fonksiyonların İndirgenmesi
- Devre Maliyeti ve Karmaşıklık
- PLD'ler; Prom, Pal, Pla
- Ardışıl Devre Temelleri
- Saklayıcı, Sayıcı ve Bellek Elemanları
- Ardışıl Devre Tasarım Yöntemleri
- Lojik Devre Tasarımında Benzetim Ortamı
- TTL ve Cmos Tümdevre Özellikleri



Kaynaklar

- “Digital Logic and Computer Design”, M. Morris Mano



Konu Başlıkları

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Konu Başlıkları

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