



Instituto Tecnológico De Estudios Superiores de Monterrey

Laboratorio de Sistemas Digitales Avanzados

Controller & Integración.

Héctor Javier Pequeño A01246364

Prof. Emilio Caballero

Links Github:

Controller Código Fuente:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/Controller.vhdl>

Integración Código fuente:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/Integracion.vhdl>

Integración TestBench:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/IntegracionTB.vhdl>

Simulacion de la integracion al final del documento

Código Fuente Controller:

```
Run Terminal Help
Datapath.vhdl Controller.vhdl Register4bits.vhdl comparator.vhdl
LabSistemasAvanzados > HectorPequeno06 > Calculadora Maximo-comun-divisor > Controller.vhdl
15     Y_id: out_std_logic;
16     O_enb: out_std_logic;
17 );
18 end controller;
19
20 architecture arch of controller is
21
22     type state_type is (S0, S1, S2, S3, S4, S5);
23     signal state, nextstate : state_type;
24
25     begin
26
27     process (clk, reset)
28     begin
29
30         if (reset = '1') then
31             state <= S0;
32
33         elsif clk'event and clk='1' then
34             state <= nextstate;
35         end if;
36     end process;
37
38     process (state, X_menor_Y, X_Mayor_Y, GO_i, X_igual_Y)
39     begin
40         case state is
41             when S0 =>
42                 if (GO_i = '1') then
43                     nextstate <= S1;
44                 else
45                     nextstate <= S0;
46                 end if;
47             when S1 =>
48                 nextstate <= S2;
49             when S2 =>
50                 if (X_igual_Y = '1') then
51                     nextstate <= S5;
52                 elsif (X_Mayor_Y = '1') then
53                     nextstate <= S3;
54                 else
55                     nextstate <= S4;
56                 end if;
57             when S3 =>
58                 nextstate <= S2;
59             when S4 =>
60                 nextstate <= S2;
61             when S5 =>
62                 nextstate <= S5;
63             when others => null;
64         end case;
65     end process;
```

Código fuente Integración:

```
sun Terminal Help
Datapath.vhdl Controller.vhdl Integracion.vhdl Register4bits.vhdl
LabSistemasAvanzados > HectorPequeno06 > Calculadora Maximo-comun-divisor > Integracion.vhdl
3
4 entity integracion is
5     port(
6         clk, reset: in std_logic;
7         GO_i: in std_logic;
8         X_i: in std_logic_vector(3 downto 0);
9         Y_i: in std_logic_vector(3 downto 0);
10        Data_o: out std_logic_vector(3 downto 0)
11    );
12 end integracion;
13
14 architecture behavioral of integracion is
15     component datapath is
16     port (
17         clk: in std_logic;
18         rst: in std_logic;
19         X_i: in std_logic_vector(3 downto 0);
20         Y_i: in std_logic_vector(3 downto 0);
21         Y_ld: in std_logic;
22         O_enb: in std_logic;
23         X_sel: in std_logic;
24         Y_sel: in std_logic;
25         X_ld: in std_logic;
26         Data_o: out std_logic_vector(3 downto 0);
27         X_gt_Y: out std_logic;
28         X_eq_Y: out std_logic;
29         X_lt_Y: out std_logic
30     );
31 end component;
32
33     component controller is
34     port(
35         clk: in std_logic;
36         reset: in std_logic;
37         GO_i: in std_logic;
38         X_Mayor_Y: in std_logic;
39         X_igual_Y: in std_logic;
40         X_menor_Y: in std_logic;
41         X_sel: out std_logic;
42         Y_sel: out std_logic;
43         X_ld: out std_logic;
44         Y_ld: out std_logic;
45         O_enb: out std_logic
46     );
47 end component;
48 signal O_enb: std_logic;
49 signal X_MAYOR_Y, X_IGUAL_Y, X_MENOR_Y: std_logic;
50 signal X_sel, Y_sel: std_logic;
51 signal X_ld, Y_ld: std_logic;
52
53
54 begin
55
56     datp : datapath port map(
57         clk,
58         reset,
59         X_i,
60         Y_i,
61         Y_ld,
62         O_enb,
63         X_sel,
64         Y_sel,
65         X_ld,
66         Data_o,
67         X_Mayor_Y,
68         X_igual_Y,
69         X_Menor_Y
70     );
71     cont : controller port map(
72         clk,
73         reset,
74         GO_i,
75         X_MAYOR_Y,
76         X_IGUAL_Y,
77         X_MENOR_Y,
78         X_sel,
79         Y_sel,
80         X_ld,
81         Y_ld,
82         O_enb
83     );
84
85 end behavioral;
```

```
Seleccionar Símbolo del sistema
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Controller.vhdl
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -e Controller
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Integracion.vhdl
Integracion.vhdl:67:13: no declaration for "x_mayor_y"
Integracion.vhdl:68:13: no declaration for "x_igual_y"
Integracion.vhdl:69:13: no declaration for "x_menor_y"
Integracion.vhdl:76:13: no declaration for "x_mayor_y"
Integracion.vhdl:77:13: no declaration for "x_igual_y"
Integracion.vhdl:78:13: no declaration for "x_menor_y"
C:\GHDL\0.36-mingw64-llvm\bin\ghdl.exe: compilation error
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Integracion.vhdl
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -e Integracion
Integracion.vhdl:56:9: for default port binding of component instance "datp":
Integracion.vhdl:56:9: signal interface "x_mayor_y" has no association in entity "datapath"
Integracion.vhdl:56:9: signal interface "x_igual_y" has no association in entity "datapath"
Integracion.vhdl:56:9: signal interface "x_menor_y" has no association in entity "datapath"
C:\GHDL\0.36-mingw64-llvm\bin\ghdl.exe: compilation error
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Integracion.vhdl
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -e Integracion
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -e Integracion
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>
```

Integración TestBench:

```
Terminal  Help
Datapath.vhdl  Controller.vhdl  Integracion.vhdl  IntegracionTB.vhdl
abSistemasAvanzados > HectorPequeno06 > Calculadora Maximo-comun-divisor > IntegracionTB.vhdl
20 signal clk: std_logic := 0;
21 signal reset, GO_i: std_logic;
22 signal X_i, Y_i, Data_o: std_logic_vector(3 downto 0);
23
24
25
26 begin
27
28     uut : Integracion port map(
29
30         clk=>clk,
31         reset=>reset,
32         GO_i=>GO_i,
33         X_i=>X_i,
34         Y_i=>Y_i,
35         Data_o=>Data_o
36     );
37
38     clock: Process
39     begin
40         clk<='1';
41         wait for 5 ns;
42         clk<='0';
43         wait for 5 ns;
44     end process;
45
46
47     --STIMULUS PROCESS
48     stim: process
49     begin
50
51         reset <= '1';
52         GO_i <= '0';
53         X_i <= "1000";
54         Y_i <= "0001";
55         wait for 30 ns;
56
57         reset <= '0';
58         GO_i <= '1';
59         wait for 50 ns;
60
61
62         reset <= '1';
63         GO_i <= '0';
64         X_i <= "1010";
65         Y_i <= "0110";
66         wait for 20 ns;
67
68         reset <= '0';
69         GO_i <= '1';
70         wait for 30 ns;
71
72
73         reset <= '1';
74         GO_i <= '0';
75         X_i <= "0111";
76         Y_i <= "1011";
77         wait for 20 ns;
78
79         reset <= '0';
80         GO_i <= '1';
81         wait for 30 ns;
82
83
84         reset <= '1';
85         GO_i <= '0';
86         X_i <= "0101";
87         Y_i <= "1010";
88         wait for 30 ns;
89
90         reset <= '0';
91         GO_i <= '1';
92         wait for 30 ns;
93
94     end process;
95
96 end behavioral;
97
```

```
Símbolo del sistema
C:\GHD\0.36-mingw64-llvm\bin\ghdl.exe: compilation error
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a IntegracionTB.vhdl
IntegracionTB.vhdl:53:9: no declaration for "rst"
IntegracionTB.vhdl:53:9: target is not a signal name
IntegracionTB.vhdl:57:9: no declaration for "rst"
IntegracionTB.vhdl:57:9: target is not a signal name
IntegracionTB.vhdl:63:9: no declaration for "rst"
IntegracionTB.vhdl:63:9: target is not a signal name
IntegracionTB.vhdl:67:9: no declaration for "rst"
IntegracionTB.vhdl:67:9: target is not a signal name
IntegracionTB.vhdl:73:9: no declaration for "rst"
IntegracionTB.vhdl:73:9: target is not a signal name
IntegracionTB.vhdl:77:9: no declaration for "rst"
IntegracionTB.vhdl:77:9: target is not a signal name
IntegracionTB.vhdl:83:9: no declaration for "rst"
IntegracionTB.vhdl:83:9: target is not a signal name
IntegracionTB.vhdl:87:9: no declaration for "rst"
IntegracionTB.vhdl:87:9: target is not a signal name
C:\GHD\0.36-mingw64-llvm\bin\ghdl.exe: compilation error
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a IntegracionTB.vhdl
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -e IntegracionTB
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -r IntegracionTB --wave=IntegracionGHW.gwh --stop-time=250ns
.\integraciontb.exe:info: simulation stopped by --stop-time @250ns
C:\Users\Héctor Pequeno\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>
```

Simulación de la Integración:

