

INSTITUTO TECNOLÓGICO DE ESTUDIOS SUPERIORES DE MONTERREY

LABORATORIO DE SISTEMAS DIGITALES AVANZADOS

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SUBTRACTOR 4 BITS.

LINKS GITHUB:

Subtractor.vhdl:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Subtractor4bits/Subtractor.vhdl>

SubtractorTb.vhdl:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Subtractor4bits/SubtractorTb.vhdl>

Subtractor 4 bits Tb:

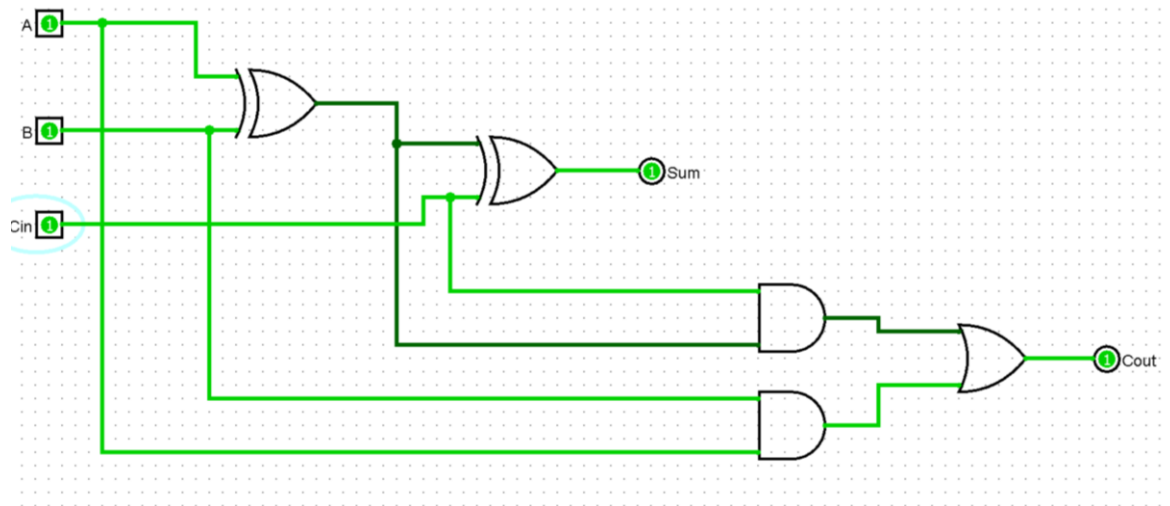
<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Subtractor4bits/Subtractor4BitsTb.vhdl>

Subtractor 4 bits vhdI:

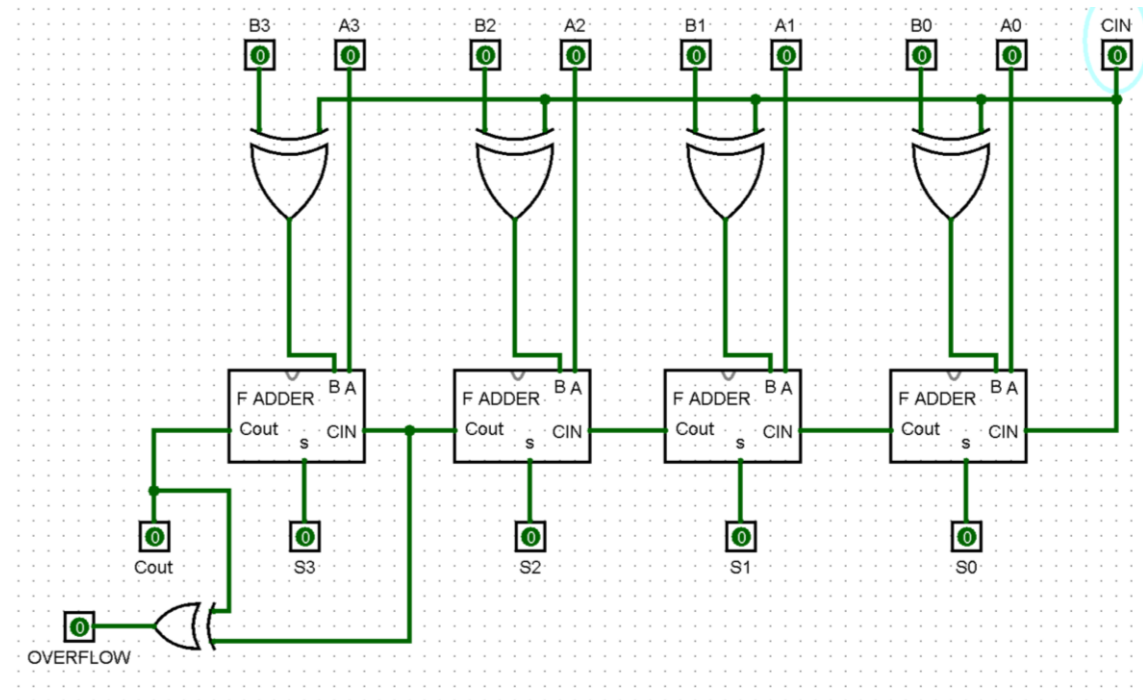
<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Subtractor4bits/Subtractor4bits.vhdl>

DISEÑOS LOGISIM.

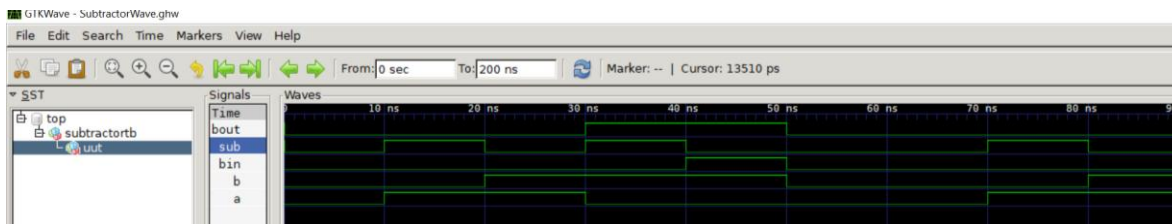
FULL ADDER.



SUBTRACTOR 4 BITS



Simulación Subtractor VHDL



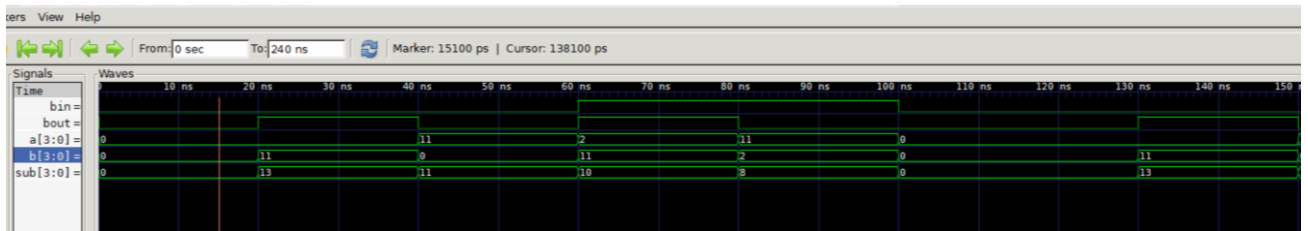
Código TB:

```
Subtractor4bits.cir  Subtractor.vhdl  SubtractorTb.vhdl X
LabSistemasAvanzados > HectorPequeno06 > Subtractor4bits > SubtractorTb.vhdl
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity Subtractor is
5  port(
6
7      A, B, Bin: in std_logic;
8      Sub, Bout: out std_logic);
9  end entity;
10
11  architecture behavioral of Subtractor is
12  component Subtractor port(
13
14      A, B, Bin: in std_logic;
15      Sub, Bout: out std_logic);
16  end component;
17
18  --inputs
19  signal A: std_logic := '0';
20  signal B: std_logic := '0';
21  signal Bin: std_logic := '0';
22
23  --outputs
24  signal sub: std_logic;
25  signal bout: std_logic;
26
27  begin
28      uut: Subtractor port map (
29
30          A=>A,
31          B=>B,
32          Bin=>Bin,
33          Sub=>Sub,
34          Bout=>Bout
35      );
36
37  --stimulus process
38  stim: process
39  begin
40
41      wait for 10 ns;
42      A<='1';
43      wait for 10 ns;
44      B<='1';
45      wait for 10 ns;
46      A<='0';
47      wait for 10 ns;
48      B<='1';
49      wait for 10 ns;
50      A<='0';
51      B<='0';
52      wait for 10 ns;
53      B<='0';
54  end process;
55  end behavioral;
```

Código Fuente Subtractor:

```
Subtractor.vhdl - Untitled (Workspace) - Visual Studio Code
Subtractor4bits.cir  Subtractor.vhdl X  SubtractorTb.vhdl
LabSistemasAvanzados > HectorPequeno06 > Subtractor4bits > Subtractor.vhdl
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity Subtractor is
5  port(
6
7      A, B, Bin: in std_logic;
8      Sub, Bout: out std_logic);
9  end entity;
10
11  architecture behavioral of Subtractor is
12
13  begin
14
15      Sub <= A xor (B xor Bin);
16      Bout <= (Bin and (B and (not A))) or ((not A) and B);
17
18  end behavioral;
```

Simulación Subtractor4Bits GTK wave:



Código TestBench:

Código Fuente:

```

5      end entity;
6
7      architecture behavioral of Subtractor4BitsTb is
8      component Subtractor4bits port(
9
10         A: in std_logic_vector(3 downto 0);
11         B: in std_logic_vector(3 downto 0);
12         Bin: in std_logic;
13         Bout: out std_logic;
14         Sub: out std_logic_vector(3 downto 0)
15     );
16
17 end component;
18
19 --inputs
20 SIGNAL A : std_logic_vector(3 downto 0) := "0000";
21 SIGNAL B : std_logic_vector(3 downto 0) := "0000";
22 SIGNAL Bin : std_logic := '0';
23
24 --OUTPUTS
25 SIGNAL Bout : std_logic;
26 SIGNAL Sub : std_logic_vector(3 downto 0);
27
28 begin
29     uut: Subtractor4bits Port map(
30         A => A,
31         B => B,
32         Bin => Bin,
33         Bout => Bout,
34         Sub => Sub
35     );
36
37 --stimulus process
38 stim: process
39     begin
40         wait for 20 ns;
41         A<="0000";
42         B<="1011";
43         wait for 20 ns;
44         A<="1011";
45         B<="0000";
46         wait for 20 ns;
47         A<="0010";
48         B<="1011";
49         Bin<='1';
50         wait for 20 ns;
51         A<="1011";
52         B<="0010";
53         Bin<='1';
54         wait for 20 ns;
55         A<="0000";
56         B<="0000";
57         Bin<='0';
58         wait for 10 ns;
59     end process;
60
61 end Subtractor4BitsTb;

```

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity Subtractor4bits is
5      port(
6          A: in std_logic_vector(3 downto 0);
7          B: in std_logic_vector(3 downto 0);
8          Bin: in std_logic;
9          Bout: out std_logic;
10         Sub: out std_logic_vector(3 downto 0)
11     );
12
13 end Subtractor4bits;
14
15 architecture behavioral of Subtractor4bits is
16     component Subtractor
17     port(
18         A, B, Bin: in std_logic;
19         Bout, Sub: out std_logic
20     );
21 end component;
22 signal Bouts: std_logic_vector(2 downto 0);
23 begin
24     --concurrent statements
25
26     SUB0: Subtractor port map(A(0), B(0), Bin ,Bouts(0) ,Sub(0));
27     SUB1: Subtractor port map(A(1), B(1), Bouts(0), Bouts(1), Sub(1));
28     SUB2: Subtractor port map(A(2), B(2), Bouts(1), Bouts(2), sub(2));
29     SUB3: Subtractor port map(A(3), B(3), Bouts(2), bout, Sub(3));
30
31
32 end behavioral;

```