Instituto Tecnológico De Estudios Superiores de Monterrey

Laboratorio de Sistemas Digitales Avanzados

Controller & Integración.

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Links Github:

Controller Código Fuente:

https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/Controller.vhdl

Integración Código fuente:

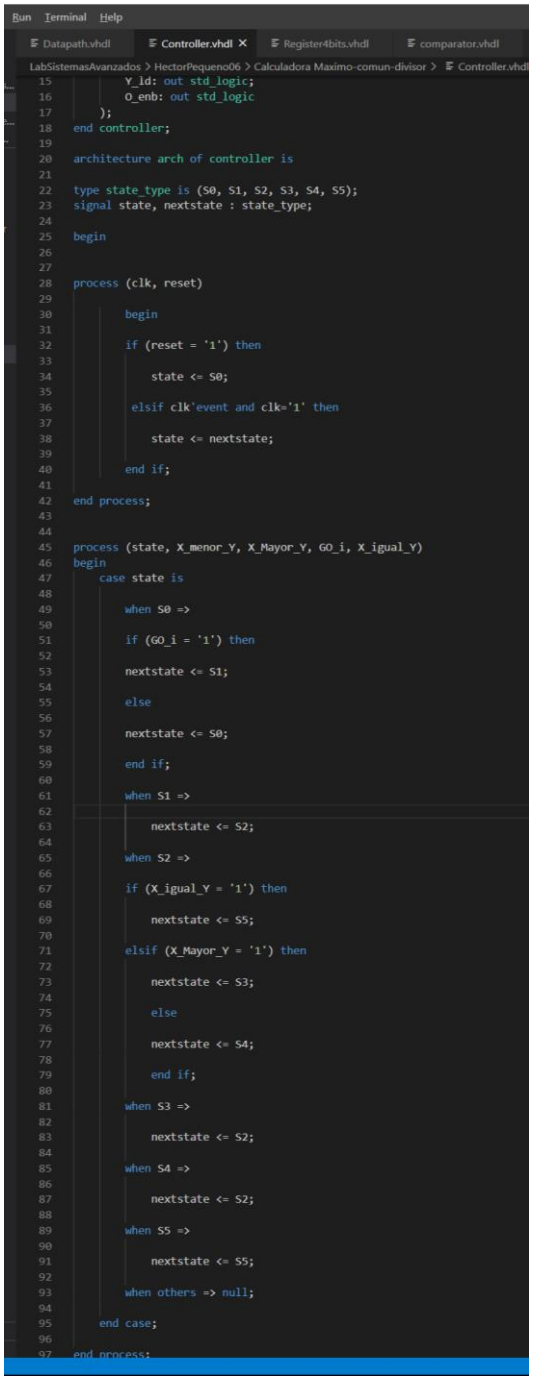
https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/Integracion.vhdl

Integración TestBench:

https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/IntegracionTB.vhdl

Simulacion de la integracion al final del documento

Código Fuente Controller:



Run Terminal Help

Datapath.vhdl | Controller.vhdl | Register4bits.vhdl | comparator.vhdl

LabSistemasAvanzados > HectorPequeno06 > Calculadora Maximo-comun-divisor > Controller.vhdl

```
        Y_ld: out std_logic;
        O_enb: out std_logic
    );
end controller;

architecture arch of controller is

type state_type is (S0, S1, S2, S3, S4, S5);
signal state, nextstate : state_type;

begin


process (clk, reset)

        begin

        if (reset = '1') then

            state <= S0;

         elsif clk'event and clk='1' then

            state <= nextstate;

        end if;

end process;


process (state, X_menor_Y, X_Mayor_Y, GO_i, X_igual_Y)
begin
    case state is

        when S0 =>

        if (GO_i = '1') then

        nextstate <= S1;

        else

        nextstate <= S0;

        end if;

        when S1 =>

            nextstate <= S2;

        when S2 =>

        if (X_igual_Y = '1') then

            nextstate <= S5;

        elsif (X_Mayor_Y = '1') then

            nextstate <= S3;

            else

            nextstate <= S4;

            end if;

        when S3 =>

            nextstate <= S2;

        when S4 =>

            nextstate <= S2;

        when S5 =>

            nextstate <= S5;

        when others => null;

    end case;

end process;
```

Código fuente Integración:

Run Terminal Help

Datapath.vhdl | Controller.vhdl | Integracion.vhdl | Register4bits.vhdl

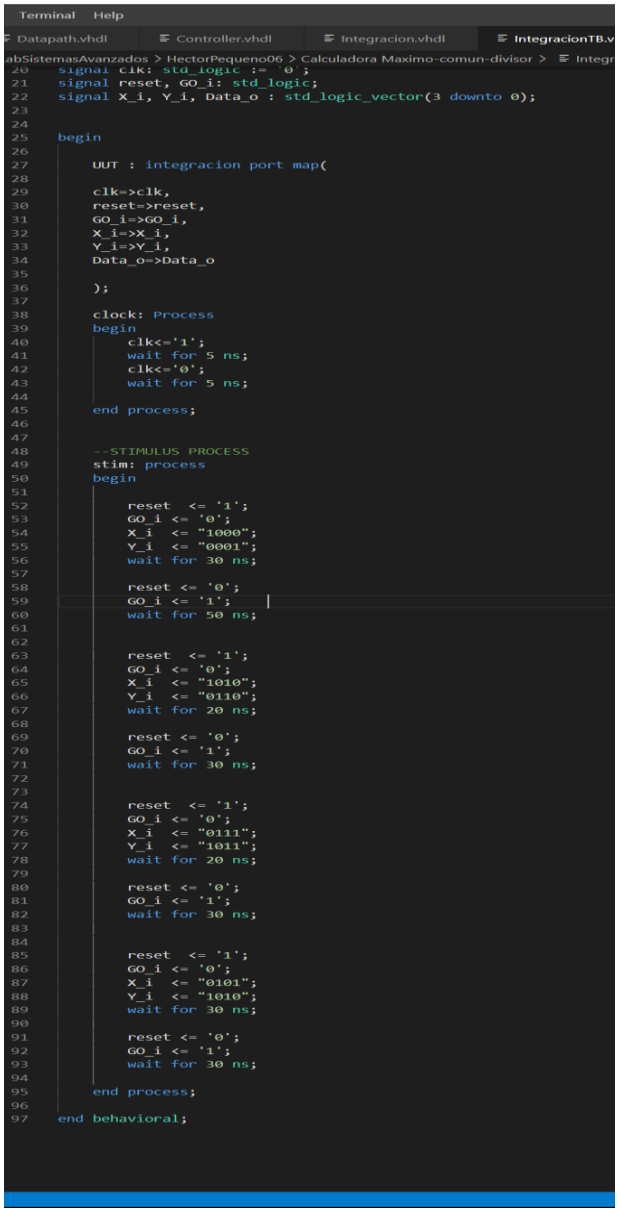
LabSistemasAvanzados > HectorPequeno06 > Calculadora Maximo-comun-divisor > Integracion.v

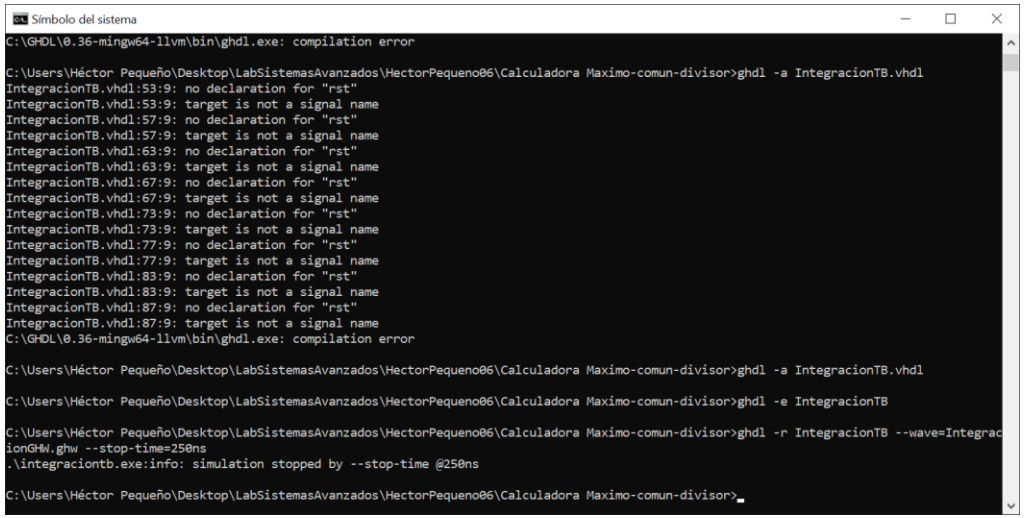
```
entity integracion is
    port(
        clk, reset: in std_logic;
        GO_i: in std_logic;
        X_i: in std_logic_vector(3 downto 0);
        Y_i: in std_logic_vector(3 downto 0);
        Data_o: out std_logic_vector(3 downto 0)
    );
end integracion;

architecture behavioral of integracion is
    component datapath is
        port (
            clk: in std_logic;
            rst: in std_logic;
            X_i: in std_logic_vector(3 downto 0);
            Y_i: in std_logic_vector(3 downto 0);
            Y_ld: in std_logic;
            O_enb: in std_logic;
            X_sel: in std_logic;
            Y_sel: in std_logic;
            X_ld: in std_logic;
            Data_o: out std_logic_vector(3 downto 0);
            X_gt_Y: out std_logic;
            X_eq_Y: out std_logic;
            X_lt_Y: out std_logic
        );
    end component;

    component controller is
        port(
            clk: in std_logic;
            reset: in std_logic;
            GO_i: in std_logic;
            X_Mayor_Y: in std_logic;
            X_igual_Y: in std_logic;
            X_menor_Y: in std_logic;
            X_sel: out std_logic;
            Y_sel: out std_logic;
            X_ld: out std_logic;
            Y_ld: out std_logic;
            O_enb: out std_logic
        );
    end component;
    signal O_enb: std_logic;
    signal X_MAYOR_Y, X_IGUAL_Y, X_MENOR_Y: std_logic;
    signal X_sel, Y_sel:std_logic;
    signal X_ld, Y_ld:std_logic;


begin

        datp : datapath port map(
            clk,
            reset,
            X_i,
            Y_i,
            Y_ld,
            O_enb,
            X_sel,
            Y_sel,
            X_ld,
            Data_o,
            X_Mayor_Y,
            X_igual_Y,
            X_Menor_Y
        );
        cont : controller port map(
            clk,
            reset,
            GO_i,
            X_MAYOR_Y,
            X_IGUAL_Y,
            X_MENOR_Y,
            X_sel,
            Y_sel,
            X_ld,
            Y_ld,
            O_enb
        );

end behavioral;
```

Seleccionar Símbolo del sistema

```
C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Controller.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -e Controller

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Integracion.vhdl
Integracion.vhdl:67:13: no declaration for "x_mayor_y"
Integracion.vhdl:68:13: no declaration for "x_igual_y"
Integracion.vhdl:69:13: no declaration for "x_menor_y"
Integracion.vhdl:76:13: no declaration for "x_mayor_y"
Integracion.vhdl:77:13: no declaration for "x_igual_y"
Integracion.vhdl:78:13: no declaration for "x_menor_y"
C:\GHDL\0.36-mingw64-llvm\bin\ghdl.exe: compilation error

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Integracion.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -e Integracion
Integracion.vhdl:56:9: for default port binding of component instance "datp":
Integracion.vhdl:56:9: signal interface "x_mayor_y" has no association in entity "datapath"
Integracion.vhdl:56:9: signal interface "x_igual_y" has no association in entity "datapath"
Integracion.vhdl:56:9: signal interface "x_menor_y" has no association in entity "datapath"
C:\GHDL\0.36-mingw64-llvm\bin\ghdl.exe: compilation error

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Integracion.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -a Integracion.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>ghdl -e Integracion

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Calculadora Maximo-comun-divisor>
```

Integración TestBench:





Simulación de la Integración: