

INSTITUTO TECNOLÓGICO DE ESTUDIOS SUPERIORES DE MONTERREY

LABORATORIO DE SISTEMAS DIGITALES AVANZADOS

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74F169 Contador 4 bits-

LINKS GITHUB:

74F169.VHDL

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/BinarySynchronousCounter/74F169.vhdl>

74F169TB.vhdl: (TESTBENCH)

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/BinarySynchronousCounter/74F169TB.vhdl>

CONTADOR8BITSbits Tb:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/BinarySynchronousCounter/binary100.vhdl>

CONTADOR8bitsTB.vhdl:

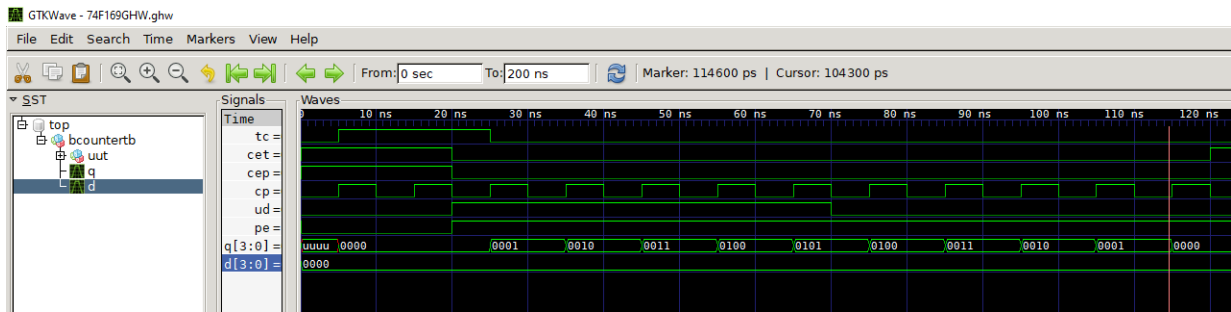
<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/BinarySynchronousCounter/Binary100TB.vhdl>

Código Fuente 74F169

```
File Edit Selection View Go Run Terminal Help 74F169.vhdl - Untitled (Workspace) - Visual Studio Code
Version1.vhdl I2C_controller.vhdl 74F169.vhdl X
LabSistemasAvanzados > HectorPequeno06 > BinarySynchronousCounter > 74F169.vhdl
21 signal Qs: unsigned(3 downto 0);
22 begin
23
24     Q<=Qs;
25
26     process(CP)
27     begin
28         if CP='1' and CP'event then
29             if PE='0' then
30                 Qs<=D;
31                 tc<='1';
32
33                 elsif UD='1' and CEP ='0' and CET='0' then
34
35                     if Qs="1111" then
36                         TC<='1';
37
38                         elsif Qs<"1111" then
39                             Qs<=Qs+1;
40                             TC<='0';
41
42                             end if;
43
44                     elsif UD='0' and CEP ='0' and CET='0' then
45                         if Qs="0000" then
46                             TC<='1';
47
48                             elsif Qs>"0000" then
49                                 Qs<=Qs-1;
50                                 TC<='0';
51
52                                 end if;
53
54                     elsif CEP='1' then
55                         Qs<=Qs;
56
57                     elsif PE='1' then
58                         Qs<=Qs;
59
60                     end if;
61
62                 end process;
63             end behavioral ;
64
65
66
67
68
69
70
71
72
73
```

Ln 23, Col 1 Spaces: 4

Funcionamiento Modulo 74F169 Simulación TestBench.



Código fuente Modulo Instanciado:

```
File Edit Selection View Go Run Terminal Help
-- binary100.vhdl X
LabSistemasAvanzados > HectorPequeno06 > BinarySynchronousCounter > -- binary100.vhdl
5  entity binary100 is
6  port(
7
8      PE: in std_logic; --negada
9      UD: in std_logic;
10     CP: in std_logic;
11     CEP: in std_logic; --negada
12     CET: in std_logic; --negada
13     D: in unsigned(7 downto 0);
14     TC: out std_logic;
15     Q: out unsigned(7 downto 0)
16
17 );
18 end entity;
19
20 architecture Behavioral of binary100 is
21 component bcounter port(
22
23     PE: in std_logic; --negada
24     UD: in std_logic;
25     CP: in std_logic;
26     CEP: in std_logic; --negada
27     CET: in std_logic; --negada
28     D: in unsigned(3 downto 0);
29     TC: out std_logic;
30     Q: out unsigned(3 downto 0)
31
32 );
33 end component;
34
35 signal TCS: std_logic;
36 signal tcsn: std_logic;
37 signal Qs: unsigned(7 downto 0);
38
39 begin
40
41     tcsn<=not tcs;
42
43     TC<=TCS;
44
45     Q<=Qs(7 downto 0);
46
47     B0: BOUNTER port map(PE,UD,CP,CEP,CET,D(3 DOWNT0 0), TCs, Qs(3 DOWNT0 0));
48     B1: BOUNTER port map(PE,UD,CP,TCSN,TCSN,D(7 DOWNT0 4), TCs, Qs(7 DOWNT0 4));
49
50     process(CP)
51     begin
52         if CP'event AND CP='1' then
53             if Qs="01100011" or Qs="10111011" then
54                 TC<='1';
55             elsif Qs="00000000" or Qs="10000000" then
56                 TC<='1';
57             else
58                 TC<='0';
59             end if;
60         end if;
61     end process;
62 end Behavioral ;
```

Simulación de dos módulos instanciados:

