



Instituto Tecnológico De Estudios Superiores de Monterrey

Laboratorio de Sistemas Digitales Avanzados

Datapath

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Links Github:

Datapath:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/Datapath.vhdl>

MUX:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/MUX.vhdl>

Comparator:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/comparator.vhdl>

Register4bits:

<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/Register4bits.vhdl>

Subtractor:

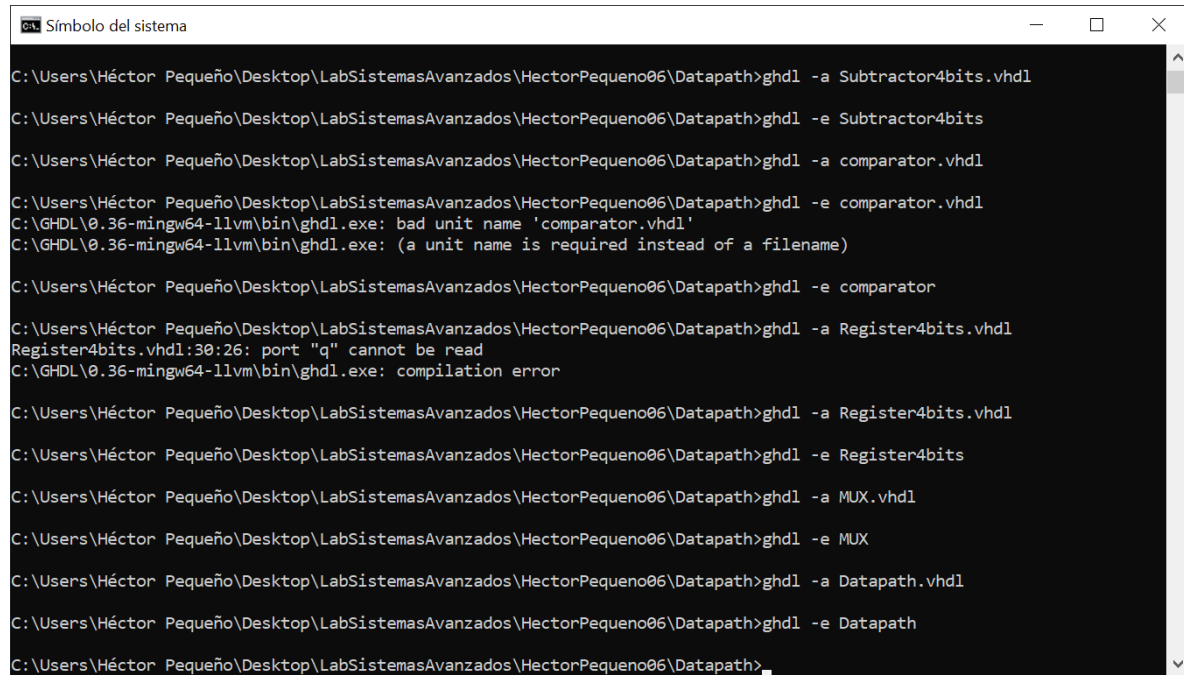
<https://github.com/HectorPequeno06/HectorPequeno06/blob/master/Calculadora%20Maximo-comun-divisor/subtractor.vhdl>

****Simulaciones adjuntadas en el Controller****

Código Fuente Datapath:

```
Run Terminal Help
Datapath.vhdl Register4bits.vhdl comparator.vhdl
LabSistemasAvanzados > HectorPequeno06 > Datapath > Datapath.vhdl
1  library IEEE;
2  use ieee.std_logic_1164.all;
3
4  entity Datapath is
5  port(
6      clk: in std_logic;
7      rst: in std_logic;
8      X_i: in std_logic_vector(3 downto 0);
9      Y_i: in std_logic_vector(3 downto 0);
10     Y_ld: in std_logic;
11     O_enb: in std_logic;
12     X_sel: in std_logic;
13     Y_sel: in std_logic;
14     X_ld: in std_logic;
15     Data_o: out std_logic_vector(3 downto 0);
16     X_gt_Y: out std_logic;
17     X_eq_Y: out std_logic;
18     X_lt_Y: out std_logic
19 );
20 end entity;
21
22 architecture behavioral of Datapath is
23 component Subtractor4bits is
24 port(
25     A: in std_logic_vector(3 downto 0);
26     B: in std_logic_vector(3 downto 0);
27     Bin: in std_logic;
28     Bout: out std_logic;
29     Sub: out std_logic_vector(3 downto 0)
30 );
31 end component;
32
33 component comparator is
34 port(
35     x, y : in std_logic_vector(3 downto 0);
36     x_Mayor_y, x_igual_y, x_menor_y : out std_logic;
37     Res: out std_logic_vector(3 downto 0)
38 );
39 end component;
40
41 component register4bits is
42 port (
43     D: in std_logic_vector(3 downto 0);
44     clk: in std_logic;
45     load: in std_logic;
46     reset: in std_logic;
47     Q: out std_logic_vector(3 downto 0)
48 );
49 end component;
50
51 component MUX is
52 port (
53     x, y: in std_logic_vector(3 downto 0);
54     sel: in std_logic;
55     res: out std_logic_vector(3 downto 0)
56 );
57 end component;
58
59 --Señales--
60 signal res: std_logic_vector(3 downto 0);
61 signal x1, x2, x3: std_logic_vector(3 downto 0);
62 signal y1, y2, y3: std_logic_vector(3 downto 0);
63 signal helper1, helper2: std_logic;
64
65 begin
66     mux_X : MUX port map (X_i, x3, X_sel, x1);
67     mux_Y : MUX port map (Y_i, y3, Y_sel, y1);
68
69     reg_X : register4bits port map (x1, clk, X_ld, rst, x2);
70     reg_Y : register4bits port map (y1, clk, Y_ld, rst, y2);
71
72     Comp : comparator port map (x2, y2, X_gt_Y, X_eq_Y, X_lt_Y, res);
73
74     SUB1_X_Y : subtractor4bits port map (x2, y2, '0', helper1, x3);
75     SUB2_Y_X : subtractor4bits port map (y2, x2, '0', helper2, y3);
76
77     Reg: register4bits port map(res, clk, O_enb, rst, Data_o);
78
79 end behavioral ;
```

Verificación de Funcionamiento:



```
Símbolo del sistema

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -a Subtractor4bits.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -e Subtractor4bits

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -a comparator.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -e comparator.vhdl
C:\GHDL\0.36-mingw64-llvm\bin\ghdl.exe: bad unit name 'comparator.vhdl'
C:\GHDL\0.36-mingw64-llvm\bin\ghdl.exe: (a unit name is required instead of a filename)

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -e comparator

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -a Register4bits.vhdl
Register4bits.vhdl:30:26: port "q" cannot be read
C:\GHDL\0.36-mingw64-llvm\bin\ghdl.exe: compilation error

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -a Register4bits.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -e Register4bits

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -a MUX.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -e MUX

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -a Datapath.vhdl

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>ghdl -e Datapath

C:\Users\Héctor Pequeño\Desktop\LabSistemasAvanzados\HectorPequeno06\Datapath>
```