INSTITUTO TECNOLOGICO DE ESTUDIOS SUPERIORES DE MONTERREY

LABORATORIO DE SISTEMAS DIGITALES AVANZADOS

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74F169 Contador 4 bits-

LINKS GITHUB:

74F169.VHDL

https://github.com/HectorPequeno06/HectorPequeno06/blob/master/BinarySynchronousCounter/74F169.vhdl

74F169TB.vhdl: (TESTBENCH)

https://github.com/HectorPequeno06/HectorPequeno06/blob/master/BinarySynchronousCounter/74F169TB.vhdl

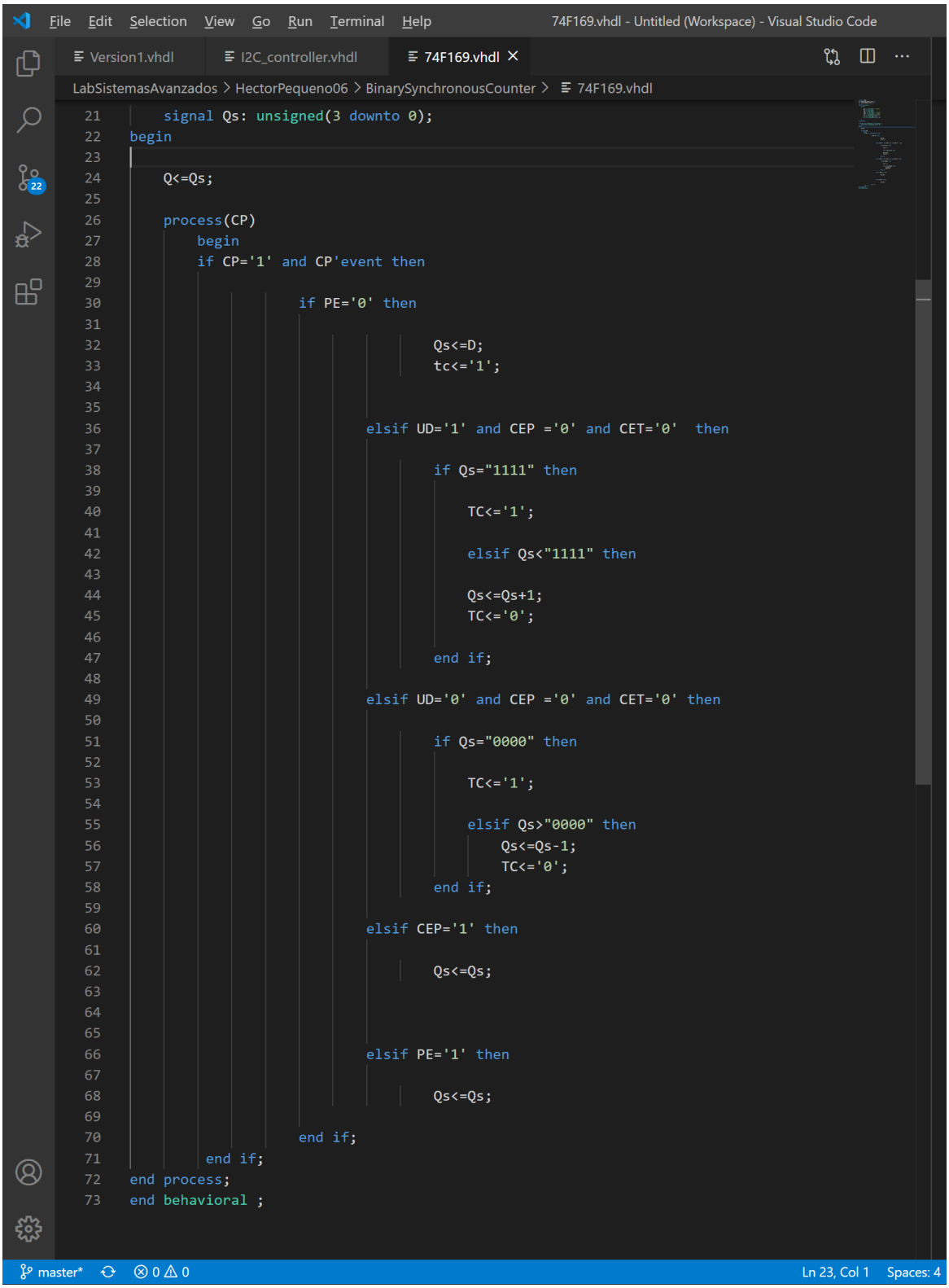
CONTADOR8BITSbits Tb:

https://github.com/HectorPequeno06/HectorPequeno06/blob/master/BinarySynchronousCounter/binary100.vhdl

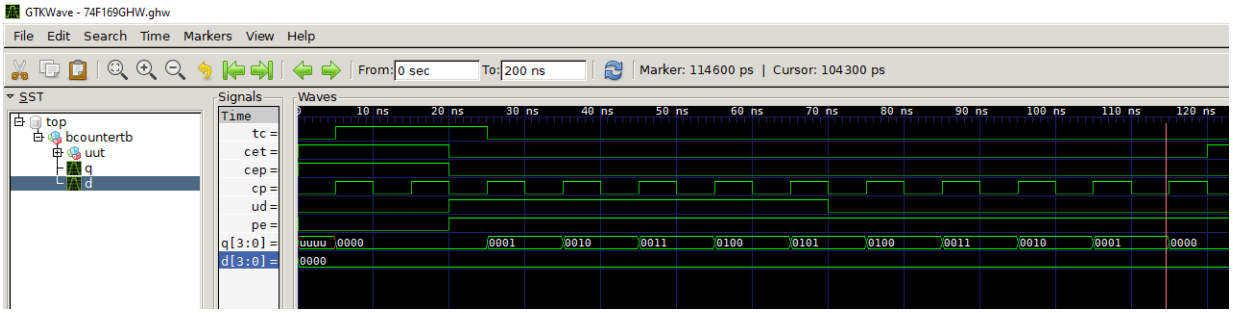
CONTADOR8bitsTB.vhdl:

https://github.com/HectorPequeno06/HectorPequeno06/blob/master/BinarySynchronousCounter/Binary100TB.vhdl

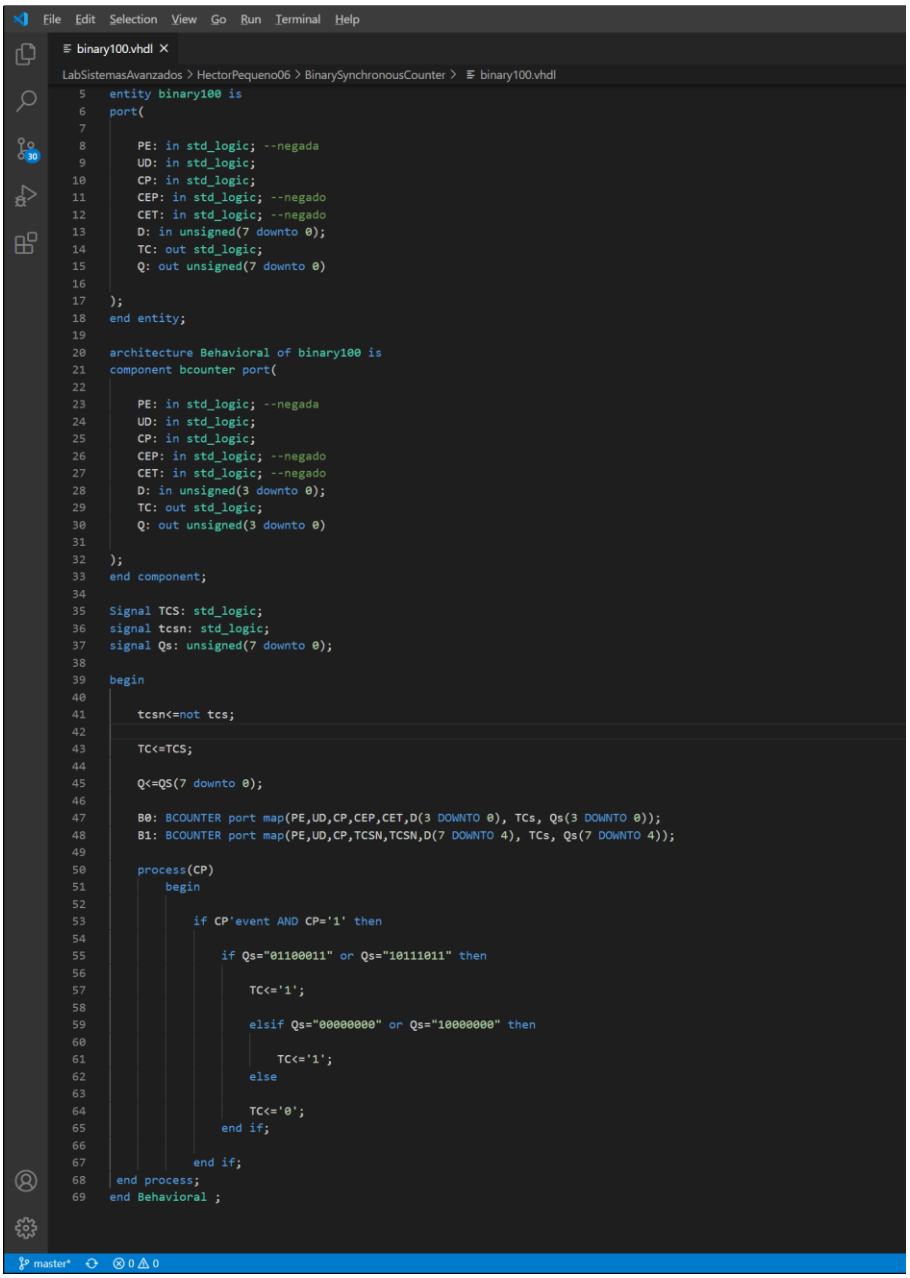
Código Fuente 74F169



Funcionamiento Modulo 74F169 Simulación TestBench.



Código fuente Modulo Instanciado:



```vhdl
entity binary100 is
port(

    PE: in std_logic; --negada
    UD: in std_logic;
    CP: in std_logic;
    CEP: in std_logic; --negado
    CET: in std_logic; --negado
    D: in unsigned(7 downto 0);
    TC: out std_logic;
    Q: out unsigned(7 downto 0)

);
end entity;

architecture Behavioral of binary100 is
component bcounter port(

    PE: in std_logic; --negada
    UD: in std_logic;
    CP: in std_logic;
    CEP: in std_logic; --negado
    CET: in std_logic; --negado
    D: in unsigned(3 downto 0);
    TC: out std_logic;
    Q: out unsigned(3 downto 0)

);
end component;

Signal TCS: std_logic;
signal tcsn: std_logic;
signal Qs: unsigned(7 downto 0);

begin

    tcsn<=not tcs;

    TC<=TCS;

    Q<=QS(7 downto 0);

    B0: BCOUNTER port map(PE,UD,CP,CEP,CET,D(3 DOWNTO 0), TCs, Qs(3 DOWNTO 0));
    B1: BCOUNTER port map(PE,UD,CP,TCSN,TCSN,D(7 DOWNTO 4), TCs, Qs(7 DOWNTO 4));

    process(CP)
        begin

            if CP'event AND CP='1' then

                if Qs="01100011" or Qs="10111011" then

                    TC<='1';

                    elsif Qs="00000000" or Qs="10000000" then

                        TC<='1';
                    else

                    TC<='0';
                end if;

            end if;
end process;
end Behavioral ;
```

Simulación de dos módulos instanciados: