Nikhil D. Hegde

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RESEARCH INTERESTS

I am interested in the areas of parallel and distributed computing, and programming languages. Specifically, I am interested in developing techniques to bridge the gap between performance and ease of programming of irregular applications on heterogeneous systems.

EDUCATION

Ph.D	Electrical and Computer Engineering, **Purdue University**, West Lafayette, USA *Thesis: Distributed Execution of Recursive Irregular Applications* Advisor: Prof. Milind Kulkarni	2019
M.Tech	Computer Science and Engineering, **Indian Institute of Technology**, Madras, India *Thesis: Mobility Management and the Role of Mobile Node in Meghadoot Architecture* Advisor: Prof. C. Siva Ram Murthy	2005
B.E	Computer Science and Engineering, **B.M.S.College of Engineering**, Bangalore, India	2002

POSITIONS SUMMARY

Assistant Professor	Indian Institute of Technology Dharwad, Karnataka, India	08/19 -present
Graduate Instructor	Purdue University, West Lafayette, USA	06/19 - 08/19
Teaching Assistant	**Purdue University**, West Lafayette, USA	01/19 - 05/19
Research Assistant	**Purdue University**, West Lafayette, USA	2017 – 2018
Summer Intern	Technology Manufacturing Group, AQS, **Intel Corp.**, Hillsboro, USA	2017
Research Assistant	**Purdue University**, West Lafayette, USA	2014 – 2017
Teaching Assistant	**Purdue University**, West Lafayette, USA	2013 – 2014
Senior Engineer	Mobile Communications Group, **Intel India Pvt. Ltd.**, Bangalore	2012 – 2013
Senior Engineer	Symbian Technology Group, **Nokia India Pvt. Ltd.**, Bangalore	2010 – 2012
Senior Engineer	**AdsFLO India Pvt. Ltd.**, Bangalore	2007 – 2010
Software Engineer – II	HPC Connectivity Group, **STMicroelectronics India Pvt. Ltd.**, Greater Noida	2005 – 2007
Software Engineer	**Infosys Technologies Ltd.**, Bangalore	2002 – 2003

PUBLICATIONS

CONFERENCES

- **Nikhil Hegde,** Qifan Chang, and Milind Kulkarni. 2019. D2P: From Recursive Formulations to Distributed-Memory Codes. In *Proceedings of the International Conference for High Performance Computing, Networking, Storage, and Analysis* (SC)*.* https://doi.org/10.1145/3295500.3356205. Acceptance Rate: 23%

- **Nikhil Hegde**, Jianqiao Liu, and Milind Kulkarni. 2017. SPIRIT: A Framework for Creating Distributed Recursive Tree Applications. In *Proceedings of the International Conference on Supercomputing* (ICS). ACM, New York, NY, USA, Article 3, 11 pages. https://doi.org/10.1145/3079079.3079095 Acceptance rate: 16%.

- **Nikhil Hegde**, Jianqiao Liu, Kirshanthan Sundararajah, and Milind Kulkarni. 2017. Treelogy: A benchmark suite for tree traversals. In *2017 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*. 227-238. https://doi.org/10.1109/ISPASS.2017.7975294 Acceptance rate: 30%.

- Jianqiao Liu, **Nikhil Hegde**, and Milind Kulkarni. 2016. Hybrid CPUGPU Scheduling and Execution of Tree Traversals. In *Proceedings of the 2016 International Conference on Supercomputing (ICS'16)*. ACM, New York, NY, USA, Article 2, 12 pages. https://doi.org/10.1145/2925426.2926261 Acceptance rate: 24%.
- K. Balaji, **N. Hegde**, B. V. Ramana, B. S. Manoj, and C. S. R. Murthy. 2005. Performance evaluation of a hybrid wireless network architecture for rural communication. In *2005 IEEE International Conference on Personal Wireless Communications, 2005. ICPWC 2005.* 212-216. https://doi.org/10.1109/ICPWC.2005.1431334
- **N. Hegde**, K. Balaji, B. V. Ramana, B. S. Manoj, and C. S. R. Murthy. 2005. Implementation and Performance Evaluation of a Hybrid Wireless Network Architecture for Rural Communication. In *Proceedings of the Eleventh National Conference on Communications: NCC-2005*. ISBN: 8177647350 9788177647358

TECHNICAL REPORTS
- **Nikhil Hegde,** Qifan Chang, and Milind Kulkarni. 2018. *D2P: Automatically generating distributed dynamic programming codes.* School of Electrical and Computer Engineering Technical Report TR-ECE-18-09. Purdue University, West Lafayette, IN, USA. https://docs.lib.purdue.edu/ecetr/492

AWARDS, GRANTS, and SERVICE
- (Grant) Toward an Auto-Programming Framework for Recursive Irregular Applications, SERB-SRG, Principal Investigator 2022-2024
- (Grant) Fast Eigensolvers for Large-Scale Hierarchical Matrices -From Design to Deployment, DST-NSM, Principal Investigator 2021-2023
- (Grant) "D2P: A framework for code generation and distributed-memory parallelization of dynamic programming algorithms". Allocation Manager: (PI: Milind Kulkarni), 11/18 - 11/19, XSEDE Startup Grant TG-ASC170007 2018
- (Grant) NSF travel grant to attend ISPASS, Santa Rosa, CA. 2017
- (Grant) NSF travel grant to attend IISWC, Providence, RI. 2016
- Supercomputing (SC) 2020(mentor), 2021 (mentor), 2022 (Tutorial Committee Member)
- HiPC, Technical Program Committee Member, 2022
- ACM TACO, Reviewer 2022
- International Conference on Parallel Processing (ICPP), Technical Program Committee member 2020, 2022

TALKS, WORKSHOPS, and PRESENTATIONS
- Concurrency and Java, Invited Talk, Mentor Graphics (Siemens EDA) 2021
- Parallel Programming Models, Invited Talk, NIT Andhra Pradesh 2021
- HPC101, Workshop, under the ambit of National Supercomputing Mission (NSM) 2021
- Parallel Programming Models, 2-day workshop, Broadridge Financial Solutions 2020
- SPIRIT: A runtime system for distributed irregular tree applications
  International Conference on Supercomputing (ICS), Chicago 2017
- Treelogy: a benchmark suite for tree traversal applications
  IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Santa Rosa 2017
- Implementation and Performance Evaluation of a Hybrid Wireless Network Architecture for Rural Communication
  National Conference on Communications (NCC), IIT Kharagpur, India 2005

POSTERS
- SPIRIT: A runtime system for distributed irregular tree applications
  Principles and Practice of Parallel Programming (PPoPP), Barcelona 2016

- Treelogy: a benchmark suite for tree traversal applications
  IEEE International Symposium on Workload Characterization (IISWC), Providence   2016

SOFTWARE CREATED
- **SPIRIT and Treelogy - https://bitbucket.org/plcl/treelogy**
- **D2P - https://bitbucket.org/plcl/d2p**

OTHER PROJECTS
- WaSP: Ensemble-based Warm-Starting Parameter Initialization for Training of Neural Network Models (Purdue University, Research project, 2/2016).
- A compiler for the LITTLE programming language (Purdue University, ECE573 project, 12/2013).

TEACHING EXPERIENCE

Assistant Professor   Computer Science and Engineering, **IIT Dharwad**   8/2019-present
CS406 (Compilers), CS316 (Compilers Lab), CS305 (Software Engineering)
CS601 (Software Development for Scientific Computing),
CS410 (Parallel Computing)
- Fully responsible for teaching CS406, CS316, CS305, CS601: creating syllabus (CS601 only), updating the course content, delivering lectures to a large class, holding office hours, preparing exams, managing tools (GitHub Classroom, GitHub teams, Actions, Autograding), designing and updating the course webpage for efficient realization of course objectives; https://hegden.github.io/teaching

Graduate Instructor   Electrical and Computer Engineering, **Purdue University**   6/2019 – 8/2019
Advanced C Programming (ECE264)
- Fully responsible for teaching the course: updating the course content, delivering lectures to a large class, holding office hours, preparing exams, managing tools (GitHub Classroom, Piazza), designing and updating the course webpage for efficient realization of course objectives; https://hegden.github.io/ece264

Teaching Assistant   Electrical and Computer Engineering, **Purdue University**
Introduction to Data Science (ECE29595)   1/2019 – 5/2019
Introduction to ASIC Design (ECE337)   8/2013 – 5/2014
- Delivered short lectures at the beginning of the lab session, assisted students on their programming tasks, graded assignments and exams, advised on project execution and presentation.

Lab Assistant   Computer Science and Engineering, **Indian Institute of Technology, Madras**   8/2004 – 4/2005
Paradigms of Programming (CS3100)
Introduction to Computer Science and Engineering (CS1300)
- Assisted students on their programming tasks.

PROFESSIONAL EXPERIENCE

Intern   **Advanced Quality Systems, MTD, Intel Corp.,** Hillsboro, USA   5/2017 – 8/2017
- Built predictive models using machine learning techniques to accurately predict yield and quality in Intel's chip manufacturing lines

Senior Engineer   **Mobile Communications Group, Intel India Pvt. Ltd.**, Bangalore   7/2012 – 8/2013
- *Development, and integration of GPS receiver software modules on cellular platform.*
  Designed and developed modules to support different positioning protocols: OTDOA, Assisted-GPS (AGPS), Network-based, and LTE Positioning Protocol.

Senior Engineer   **Nokia India Pvt. Ltd.**, Bangalore   6/2010 – 6/2012

- *Creation of hardware adaptation and OS layer for GPS receiver chips used in Nokia smartphones.*
  Ported I2C driver for SMP compliance, improved Symbian OS scheduler, developed location services protocols (RRLP, RRC, SUPLV1.0) and tested for GCF and PTCRB compliance, developed modules to support Assisted-GPS and network-based positioning technologies**.**
- *Creation of robust authentication methods for Mobile Device Management (DM)*
  Developed modules to support mutual-authentication of mobile device and DM server.

Senior Engineer   **AdsFLO India Pvt. Ltd.**, Bangalore   10/2007 – 5/2010

- *Creation of targeted mobile advertising solutions for iOS, WinCE, Symbian based smartphones, and DVB-H based devices.*
  Supported demonstration of the product at MWC (2007 – 2009), and CES (2008 – 2009), developed Ad-scheduling algorithms to ensure fairness, optimize fill rate, and minimize Ad fatigue, developed Electronic Service Guide (ESG), and applied basic image-processing and error-correction algorithms.
- *Recruitment for the mobile devices team*
  Conducted technical interviews and mentored new employees

Software Engineer – II   **STMicroelectronics India Pvt. Ltd.**, Greater Noida   7/2005 – 10/2007

- *Design and development of link-layer software for the DVB-H receiver chip.*
  Modeled memory controller, Reed-Solomon encoder, and DVB-H traffic decoder in software. Performed link layer validation of DVB-H IP on FPGA, Implemented drivers for taped-out chip.

Software Engineer   **Infosys Technologies Ltd.**, Bangalore   12/2002 – 7/2003

- Tested MPLS enabled network switches.

SKILLS

Programming: C, C++, Symbian C++, Objective C, Perl, Python, Shell, OpenGL-ES, Linux Kernel, MPI, OpenMP, Pthreads, Boost Graph Libraries.
Debuggers: Lauterbach, Trace-32, Fastrace, ARM extended debugger (AXD), Multi-ICE, gdb.
Others: Spirent ULTS, Cadence SimVision, WireShark Network Traffic Analyzer, OpenSSL, JBoss, and Tomcat, LaTeX.
Versioning and Quality: Rational tool chain, SVN, CVS, Git, Bugzilla.