Department of Electronic Systems Engineering

भारतीय विज्ञान संस्थान

NeuRonICS Lab
Neurally-inspired Reconfigurable Intelligent Circuits & Systems

Waveform + Tone Generation using CORDIC Algorithm

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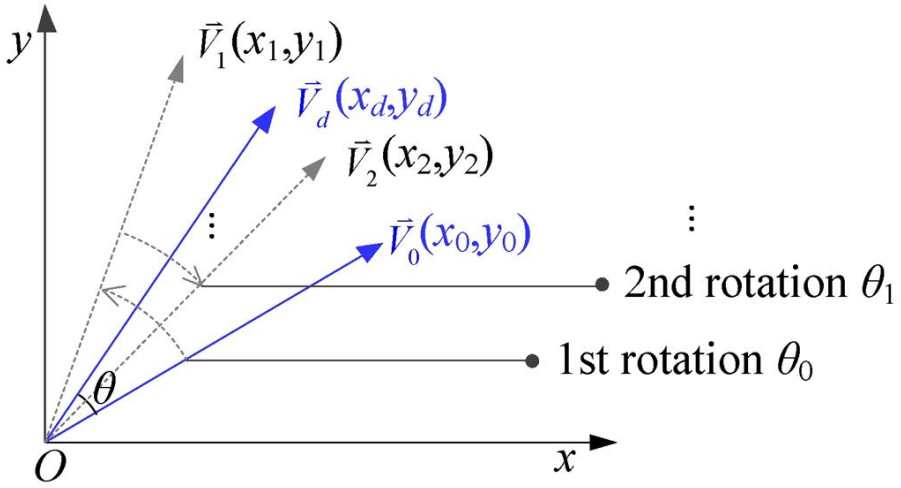
Principle:



$$x[i+1] = x[i] - \sigma_i 2^{-i} y[i]$$

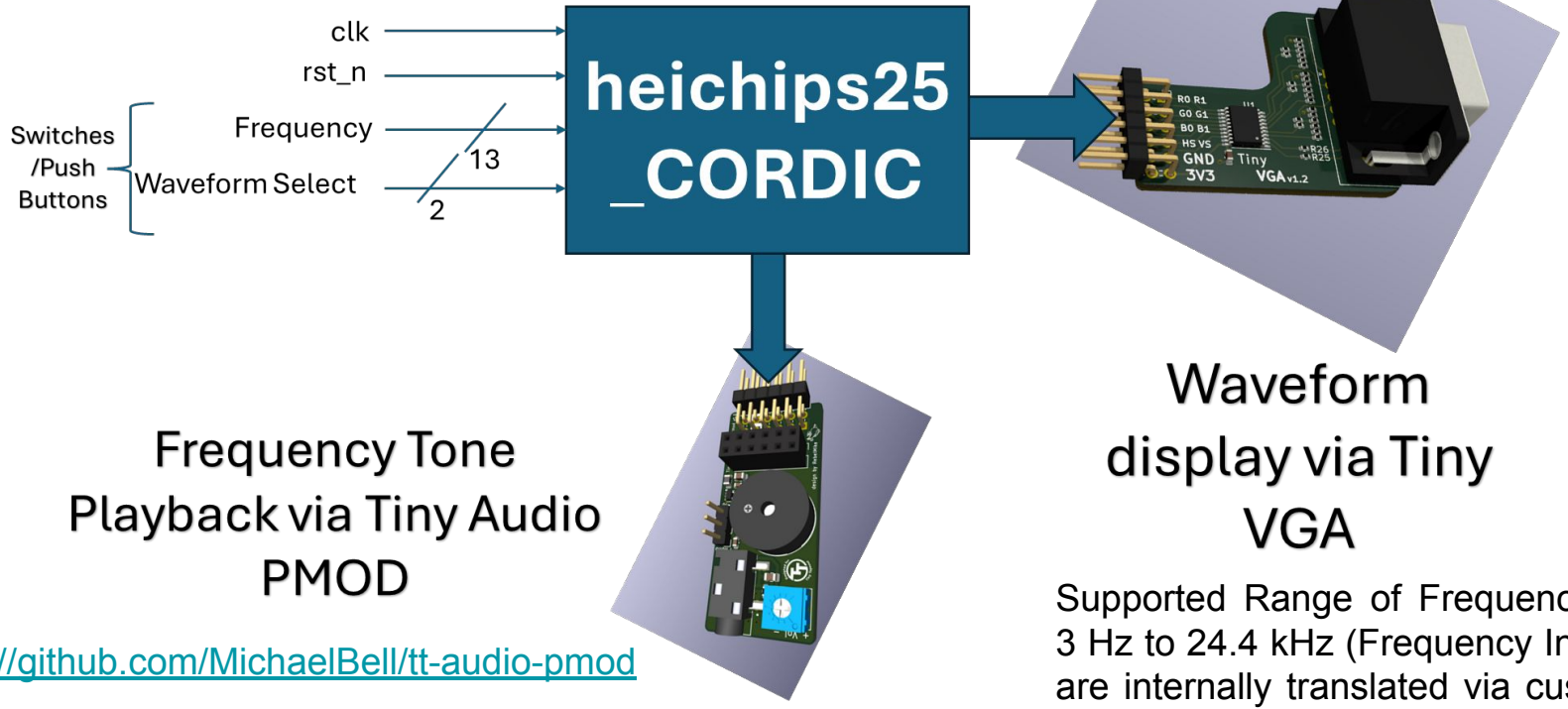
$$y[i+1] = y[i] + \sigma_i 2^{-i} x[i]$$

$$z[i+1] = z[i] - \sigma_i tan^{-1}(2^{-i})$$

J. E. Volder, "The CORDIC Trigonometric Computing Technique," in IRE Transactions on Electronic Computers, vol. EC-8, no. 3, pp. 330-334, Sept. 1959, doi: 10.1109/TEC.1959.5222693.

System Block Diagram

https://github.com/mole99/tiny-vga



Frequency Tone Playback via Tiny Audio PMOD

https://github.com/MichaelBell/tt-audio-pmod

Waveform display via Tiny VGA

Supported Range of Frequencies:- 3 Hz to 24.4 kHz (Frequency Inputs are internally translated via custom logic)

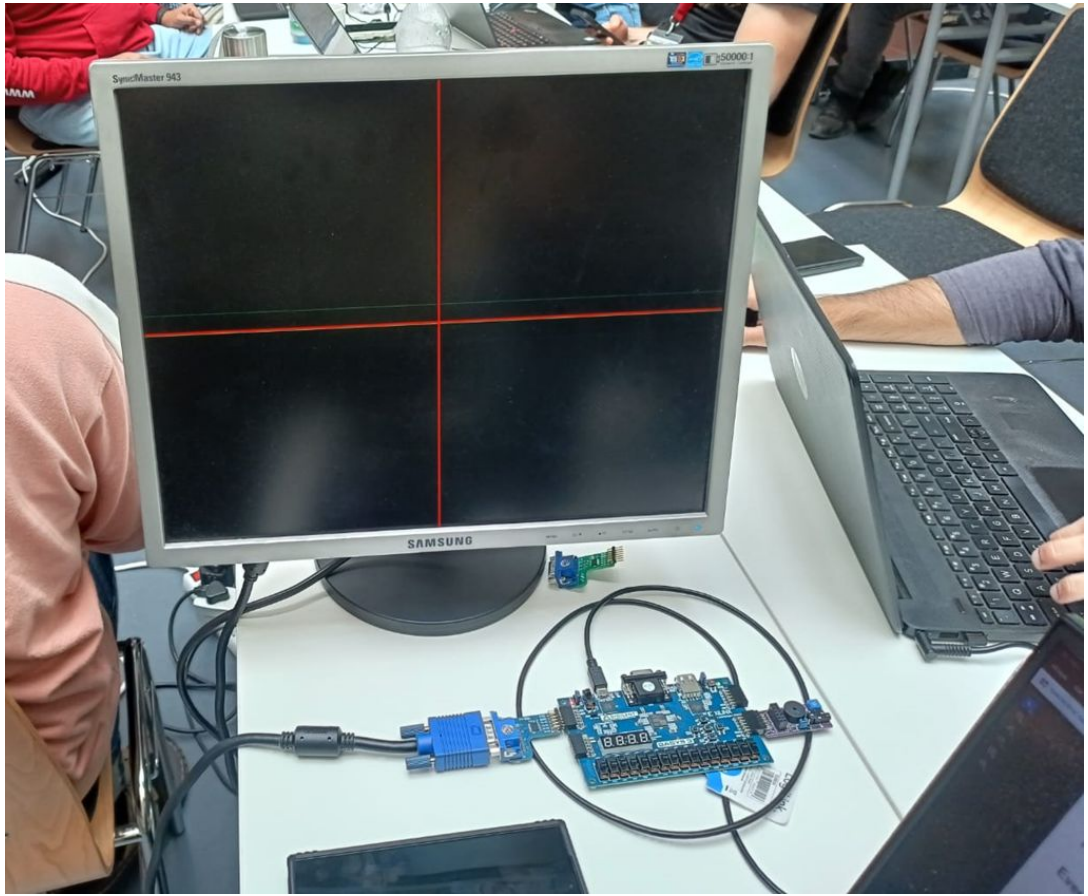
Results

- Achieved resource-efficient sine/cosine/trigonometric computations without multipliers.
- Instantaneous frequency tuning via IO pin control → real-time configurability.
- No external memory buffer for VGA output → optimized, low-latency design.
- Sinusoidal, triangular, and square wave outputs.
- PMOD speaker integration - actual sound synthesis from silicon.

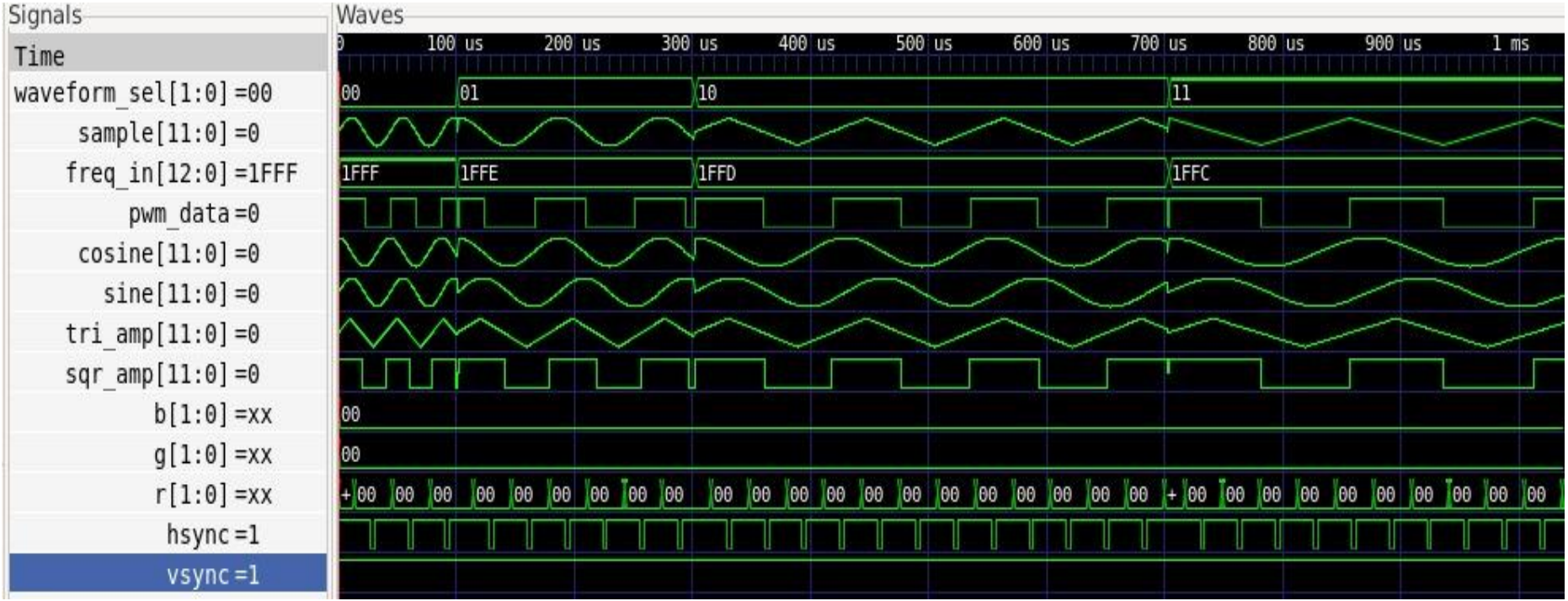
Hardware Optimisations

- Pipelined Implementation for the CORDIC block to maximize the throughput
- Reduced the data-width to fit in the area required
- Not using external memory. All the compute is on-the-fly basis
- No Data buffer for the VGA Module

BASYS 3 FPGA Setup



Verification Results:



Generated Waveforms for different Frequencies. Support for Triangular and Square Signals are also added. Pwm_data corresponds to the input for the audio pmod, whereas r, g, b, hsync and vsync correspond to the inputs for the tiny VGA module.

Synthesis Results

Setup slack (Worst Slack, WNS):

nom_fast_1p32V_-40°C	+5.99 ns
nom_slow_1p08V_125°C	+2.93 ns (worst-case setup)
nom_typ_1p20V_25°C	+5.08 ns

Hold slack (Worst Slack, WNS):

nom_fast_1p32V_-40°C	+0.109 ns
nom_slow_1p08V_125°C	+0.609 ns
nom_typ_1p20V_25°C	+0.283 ns

Area

Die area	100,000 μm² (500 × 200 μm)
Core area	93,351 μm²
Instance area (stdcells)	79,552 μm²
Utilization	**85.2%**
Instances	7,286

Power

Total Power: ~12 mW

Internal	7.8 mW
Switching	4.2 mW
Leakage	negligible (~1.8 µW)

IR drop

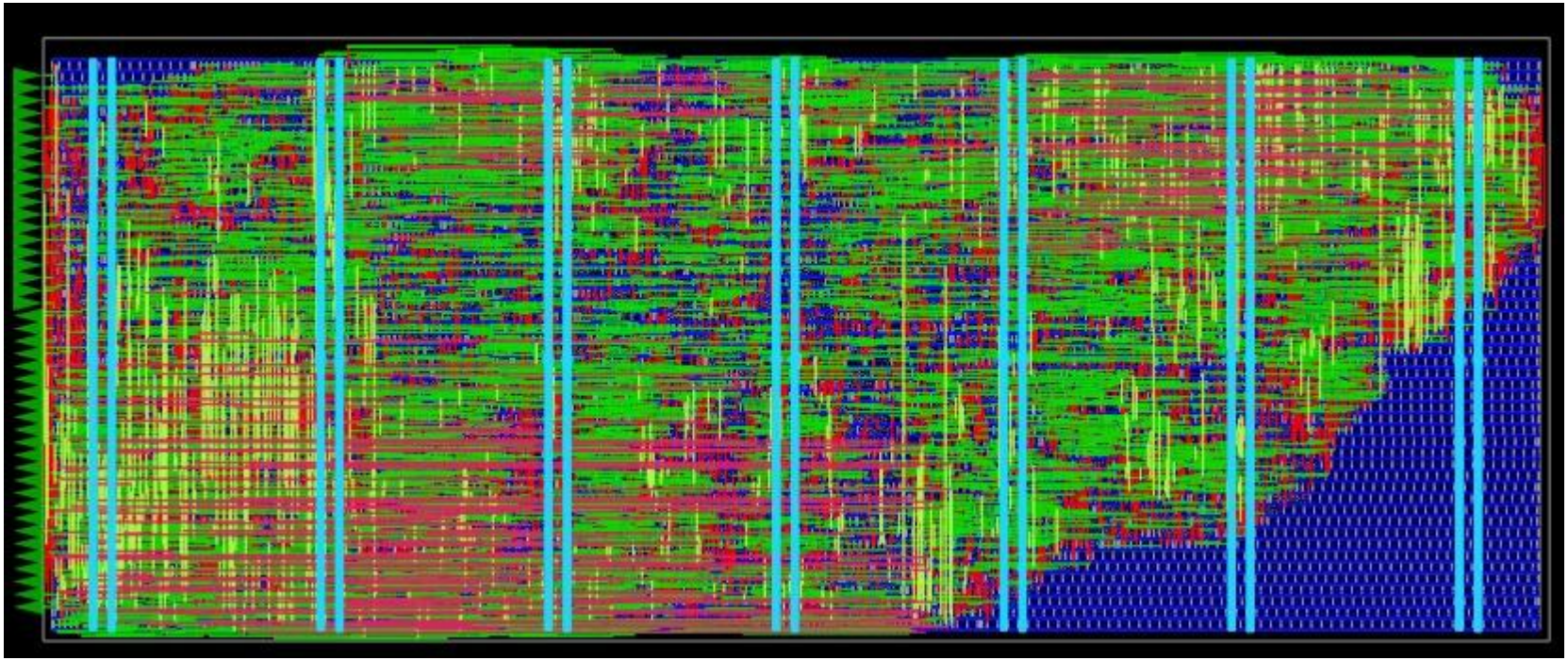
Average	~1 mV
Worst	~2.34 mV
Supply at VDD	1.2 V → **<0.2% drop**

Antenna violations: 3 nets (fixable with diode insertion if required).

Final DRC errors: 0 (both Magic & KLayout).

LVS mismatches: 0 (perfect match).

Chip Layout:



Final Layout of the generated design. The Utilization factor is around **85%** in the small die area.

Thank You