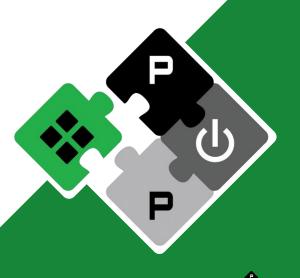


HeiChips--Snitch

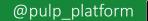
Diyou Shen Kevin Klein Asma Mohsin Gulafshan dishen@iis.ee.ethz.ch kevin.klein@stud.uni-heidelberg.de asma.mohsin@stud.uni-heidelberg.de gulafshan.gulafshan@stud.uni-heidelberg.de



Open Source Hardware, the way it should be!



pulp-platform.org







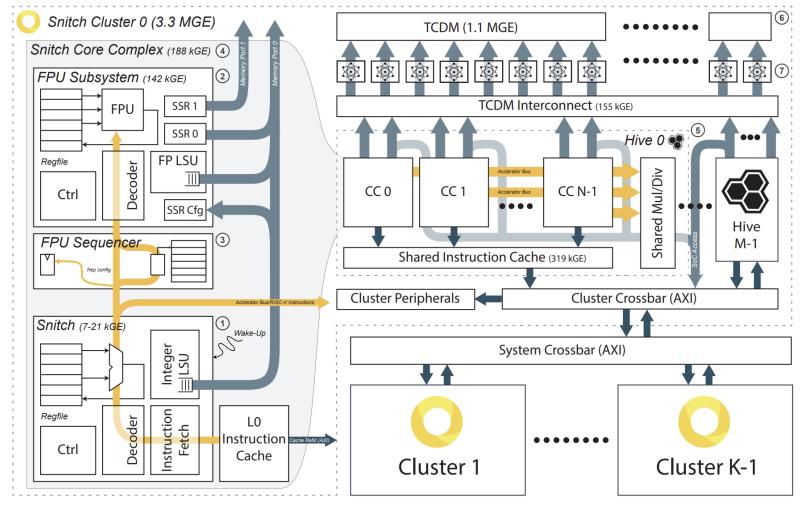




Adapted from Snitch Cluster

- 32-bit, RISC-V
- Single Core
- No extra extensions
- No outstanding LD/ST





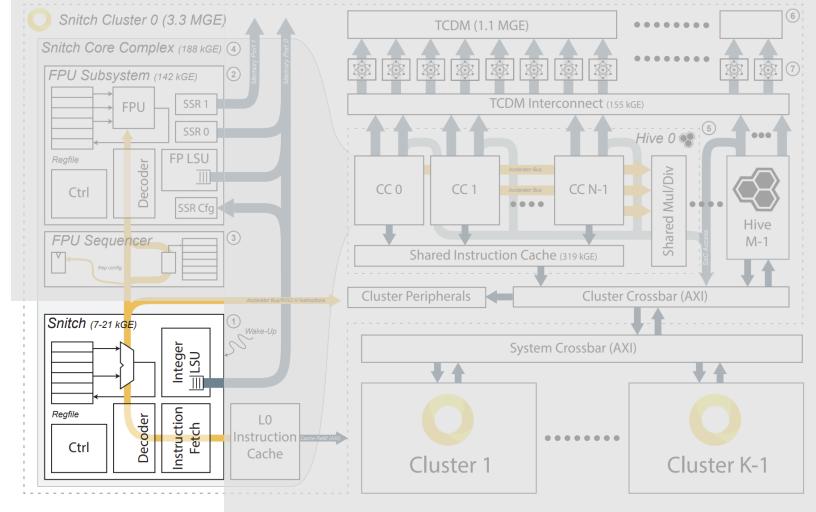






Adapted from Snitch Cluster

- 32-bit, RISC-V
- Single Core
- No extra extensions
- No outstanding LD/ST



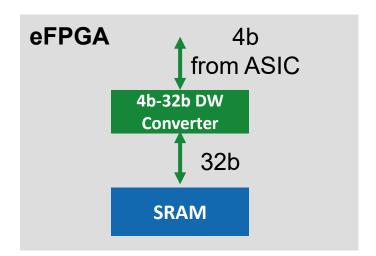


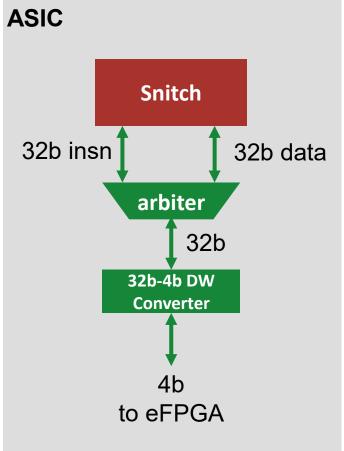




Adapted from Snitch Cluster

- 32-bit, RISC-V
- Single Core
- No extra extensions
- No outstanding LD/ST











Adapted from Snitch Cluster

- 32-bit, RISC-V
- Single Core
- No extra extensions
- No outstanding LD/ST

Early backend results

- Area: 113744 um2
 - Fit well in large tile
 - Need to enable RVE (reduced register) if only have small tile
- Timing (100MHz)
 - Hold clean
 - Setup: WNS of -1.5ns, plan to divide the clk internally to resolve the problem

Direction	Name	Usage
Out	uio_out[3:0]	req data out
Out	uio_out[7:4]	addr high out
Out	uo_out[7:4]	addr low out
Out	uo_out[3]	write enable
Out	uo_out[2]	strb enable
Out	uo_out[1]	rsp ready
Out	uo_out[0]	req valid
In	ui_in[7:4]	rsp data in
In	ui_in[3]	unused
In	ui_in[2]	wake up
In	ui_in[1]	rsp valid
In	ui_in[0]	req ready







Verification plan

- TB in sv
- Compile assembly code into a simulation memory
- load, macc/mul/add, store data
- Maybe a Hello World to UART later

