



Open-source process design kit based on IHP-SG13G2 technology

Krzysztof Herman



HeiChips, Heidelberg 2025

Projects: BMFTR -> FMD-QNC (16ME0831)

About me

- 0 BSc in electronics
- 0 MSc in Acoustics
- 0 PhD in Telecommunications
- 0 15 years of experience in academia Poland/Chile
- 0 bi-polar experience
- 0 IHP-Open-PDK developer since 2023

...one of the first „victims” of the open-source silicon movement



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Introduction to the IHP

Our motivation and goals in the open source silicon domain

Description of the open source solutions developed and supported by IHP

Understanding the power of the community

Planification of Open MPW runs

How do we make the PDK ? ?

IHP in a nutshell



- 0 IHP is the European research and innovation centre for silicon-based systems, ultrahigh-frequency circuits and technologies,
- 0 Unique selling point of a 200mm pilot line for state-of-the-art BiCMOS technologies, operated under industry-like conditions, 24/7, for the provision of prototypes and low-volume production runs.
- 0 Qualified technological platform with direct access for science and industry
- 0 Vertical structure from material research to system architecture
- 0 350+ employees, 40+ nationalities



Vision

"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalized and networked world as well as for the sustainable preservation of our natural living conditions."

130nm SiGe BiCMOS Technologies for RF Applications



	SG13S	SG13G2	SG13G3Cu
HBT f_t/f_{max}	250 / 340 GHz	350 / 450 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CEO}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
HeiChipsors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	2.1 fF / μm^2
Metallization	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	*Cu: 4 + 2 (3 μm) Al: 2 (3 μm)

*Cu BEOL from X FAB

- SG13G2 technology was selected for the development of an open source PDK

- Target are high-end technology developments, low volume market introduction, technology transfer for potential mass production in commercial fabs
- SG13S & SG13G2 are qualified and ready for Low Volume of high end products
- SG13G3Cu is early access - qualification scheduled 2025

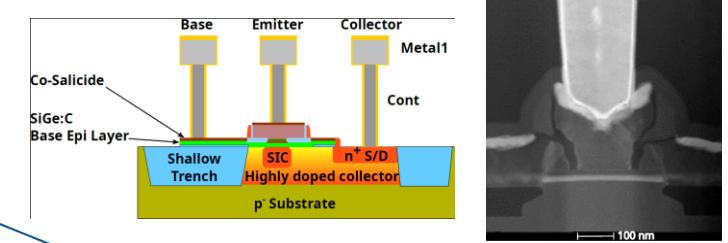


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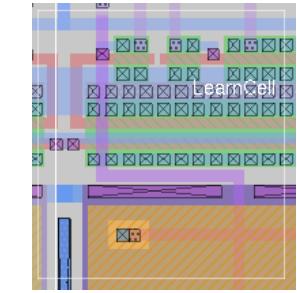
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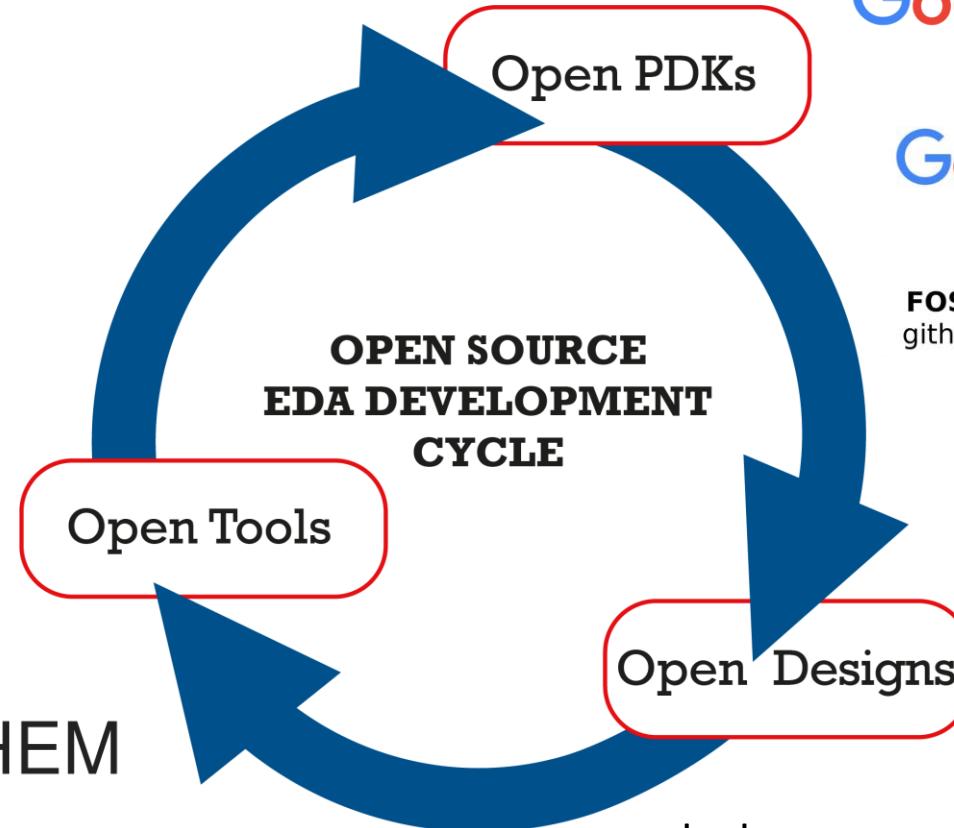
Planification of Open MPW runs

How do we make the PDK ? ?

Open source ASIC development cycle



XSCHEM



Google + SKYWATER TECHNOLOGY

Google + GLOBAL FOUNDRIES

FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk



IHP-Open-PDK



test cases, regression tests, benchmarks, use cases,
user stories, feedback, error reports, feature requests

IHP Open PDK on github



IHP-GmbH / IHP-Open-PDK

Type / to search

Issues 135 Pull requests 19 Discussions Actions Projects 1 Wiki Security Insights Settings

IHP-Open-PDK Public Edit Pins Unwatch 30 Fork 96 Star 560

dev 2 Branches 2 Tags Go to file Add file Code About

This branch is 162 commits ahead of main .

KrzysztofHerman Merge pull request #559 from FlinkbaumFAU/remove_verilogp... 1 hour ago 961 Commits

.github Updating klayout installation for actions 5 months ago

ihp-sg13g2 Merge pull request #559 from FlinkbaumFAU/remove_verilo... 1 hour ago

Preview Mode

130nm BiCMOS Open Source PDK, dedicated for Analog, Mixed Signal and RF Design

ihp-open-pdk-docs.readthedocs.io open-source pdk ihp

Readme

QR code

Minimal installation – plug and play & KISS approach

Working with the IHP Open PDK



Welcome to IHP 130nm BiCMOS Open Source PDK documentation!



This documentation is currently a work in progress.



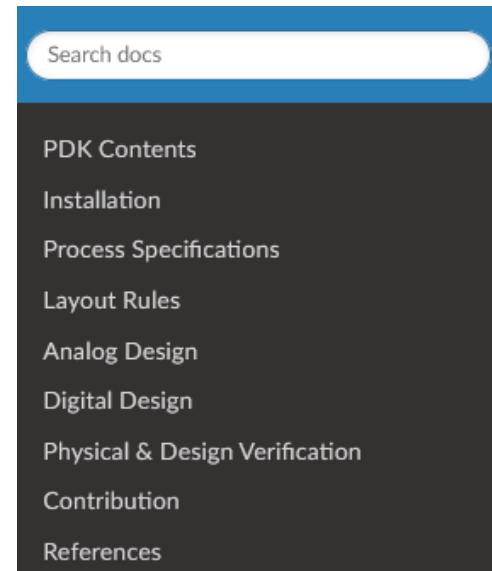
Current Status – Experimental Preview

Ubuntu 22.04+ compatible

Configuration: \$PDK_ROOT, \$PDK

Dependencies installation: mainly apt-get

Tools have to be installed (binaries, sources)



1. Dependencies

The tools supported by IHP-Open-PDK are open source and are not always distributed as binaries or through packages available to install using programs such as apt-get. In order to use the tools one have to compile/build it from the sourc code usually available on platforms like github, gitlab, sourcforge codeberg. Having all the build tools installed and meeting all necessary dependencies the installation program is usually straightforward.

1.1. Build tools

The first step to build a tool/program from a source code is to have build tools, what means necessary compilers and make systems, which allows the user to build the source code.

```
sudo apt-get install -y build-essential  
sudo apt-get install -y qtbase5-dev qttools5-dev  
sudo apt-get install -y clang cmake libtool autoconf  
sudo apt-get install -y python3 python3-dev python3-pip python3-virtualenv python3-venv  
sudo apt-get install -y ruby ruby-dev
```

1.2. Useful tools

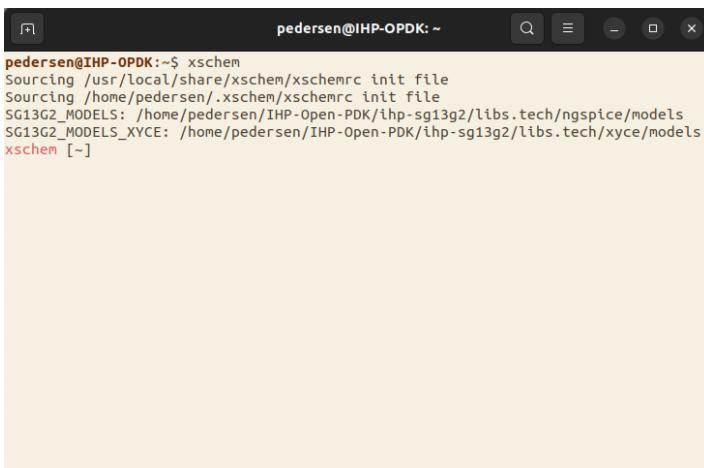
Before performing installation from sources it is recommended to install some tools that are useful:

```
sudo apt-get install -y btop tree xterm graphviz git  
sudo apt-get install -y octave liboctave-dev
```



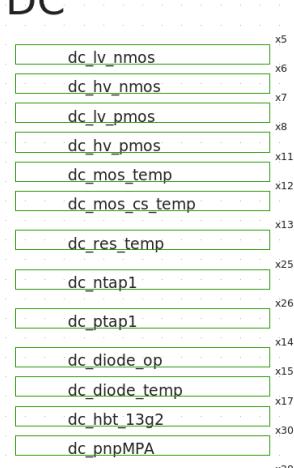
Getting started really isn't that hard!





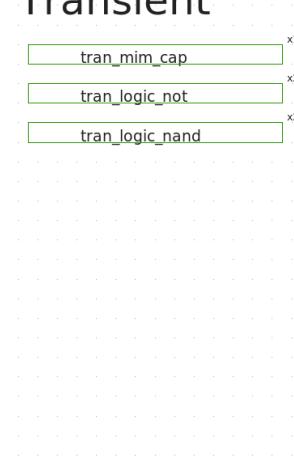
```
pedersen@IHP-OPDK:~$ xschem
Sourcing /usr/local/share/xschem/xschemrc init file
Sourcing /home/pedersen/.xschem/xschemrc init file
SG13G2_MODELS: /home/pedersen/IHP-Open-PDK/lhp-sg13g2/libs.tech/ngspice/models
SG13G2_MODELS_XYCE: /home/pedersen/IHP-Open-PDK/lhp-sg13g2/libs.tech/xyce/models
xschem [~]
```

DC



- dc_lv_nmos
- dc_hv_nmos
- dc_lv_pmos
- dc_hv_pmos
- dc_mos_temp
- dc_mos_cs_temp
- dc_res_temp
- dc_ntap1
- dc_ptap1
- dc_diode_op
- dc_diode_temp
- dc_hbt_13g2
- dc_pnpMPA
- dc_logic_not

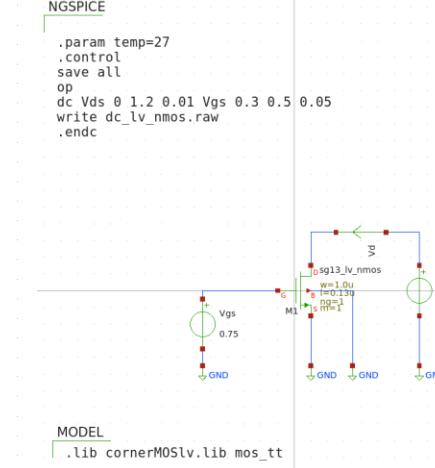
Transient



- tran_mim_cap
- tran_logic_not
- tran_logic_nand

NGSPICE

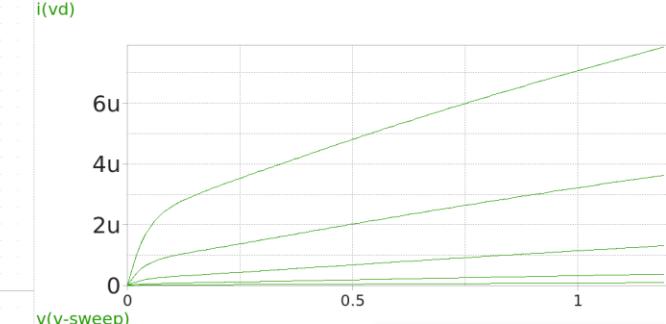
```
.param temp=27
.control
  save all
  op
  dc Vds 0 1.2 0.01 Vgs 0.3 0.5 0.05
  write dc_lv_nmos.raw
.endc
```



MODEL

```
.lib cornerMOSlv.lib mos_tt
```

i(vd)



load waves Ctrl + left click

Copyright 2023 IHP PDK Authors
x5. sg13g2_tests/dc_lv_nmos.sch



```
** Copyright 2001-2024. The ngspice team.
** Please get your ngspice manual at https://ngspice.sourceforge.io/docs.html
** Documentation is also available at https://ngspice.sourceforge.net/bgnspice.html
** Creation Date: Tue Jul 18 16:09:25 2023 UTC 2024
*****
Note: No compatibility mode selected!
Circuit: ** sch_path: /home/pedersen/IHP-Open-PDK/lhp-sg13g2/libs.tech/xschem/sg13g2_tests/dc_lv_nmos.sch
Doing analysis at TEMP = 27,000000 and TNOM = 27,000000
Using SPARSE 1.3 as Direct Linear Solver
No. of Data Rows : 1
Doing analysis at TEMP = 27,000000 and TNOM = 27,000000
Using SPARSE 1.3 as Direct Linear Solver
No. of Data Rows : 696
Binary raw file "dc_lv_nmos.raw"
Program exit.
```

Some of the Information Available in ChatGPT



1. Process Technology

- Overview of advanced semiconductor technology, including high-performance devices and integrated components
- Offers various modules for expanded functionality

2. Multi-Project Wafer (MPW) Services

- Includes details on pricing, schedules, and supported processes
- Specifies chip area requirements and approval process for smaller designs

3. Layout and Process Specifications

- Defines design rules, device specifications, and physical constraints
- Includes details on available materials and process layers



Design examples and courses



IHP-GmbH / IHP-AnalogAcademy

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OS-EDA / Course

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Course Public

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Course instance: 1 Week, hands on

Mon	Tue	Wed	Thu	Fri
L1: Introduction T1: Training	Q1, Q2: Recap Feedback L3: Verilog T3: Training	Q3, Q4: Recap Feedback L5: PDK T5: Training	Q5, Q6: Recap Feedback L7: OpenROAD Flow scripts T7: Training	Q7: Recap L8: Tapeout Feedback
L2: OpenROAD tools T2: Training	L4: OpenROAD first run T4: Training	L6: OpenROAD GUI T6: Training	L7: OpenROAD Flow scripts 2 T7: Training	Spare time and Wrap-Up

L : Lectures
T : Training and Hands-On
Q : Questions

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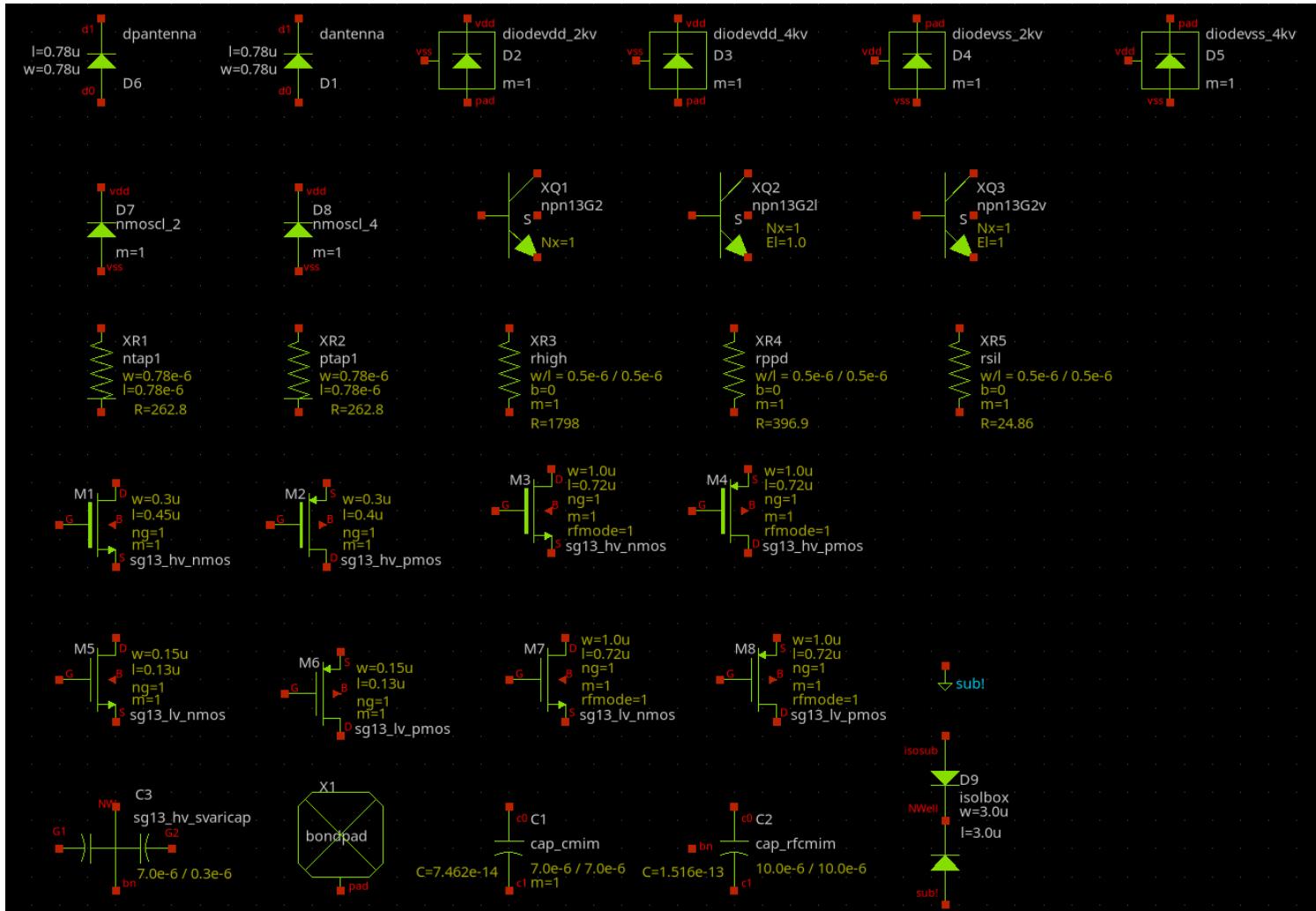
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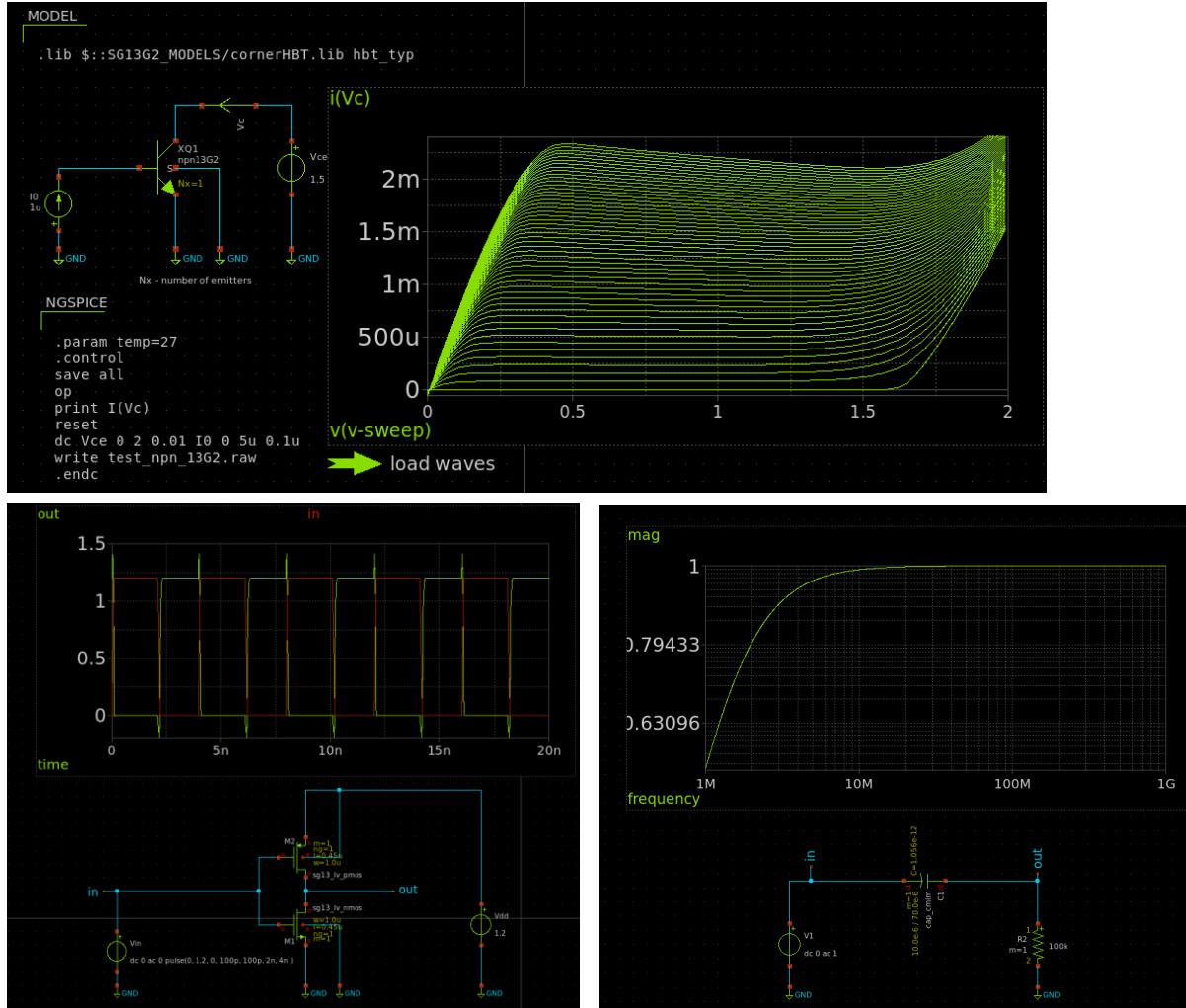
OpenPDK support for schematic capture



The current version of the IHP OpenPDK supports:

- xschem primitives for schematic capture
- automatic ngspice/Xyce compatible netlist generation
- example use cases to show the basic functionalities and parameters of the primitives

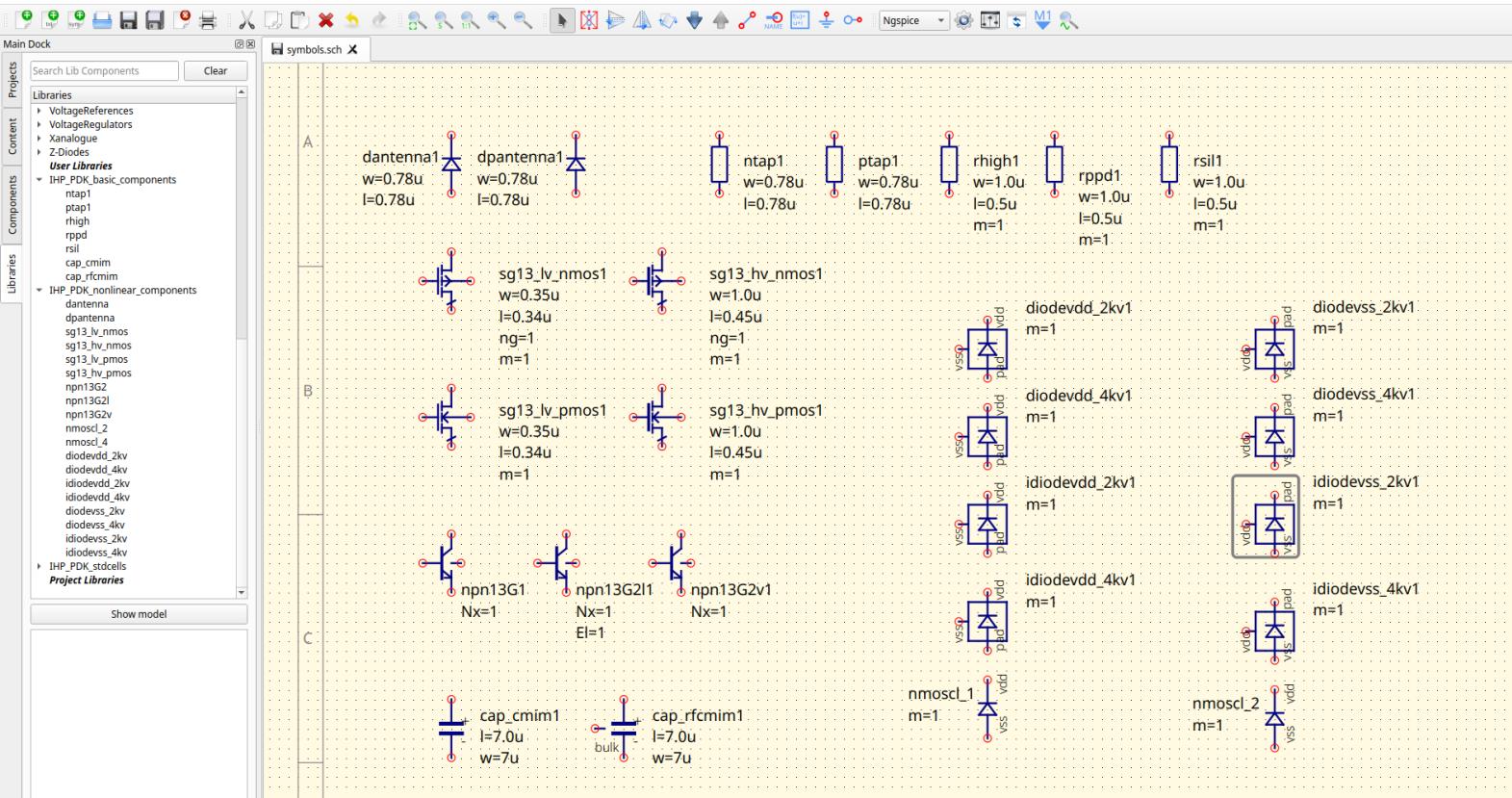
OpenPDK support for simulations



Analog simulation facilities:

- PSP103.6 MOSFET models from SemiMod,
- ngspice/Xyce compatible netlists,
- process corners: typical, best case, worst case,
- statistics related to the process variation,
- simulation examples segmented by simulation type: DC, TRAN, AC, MonteCarlo, S-parameters
- postprocessing python scripts,
- model extensions for RF frequency range,
- ngspice 40+ compatible

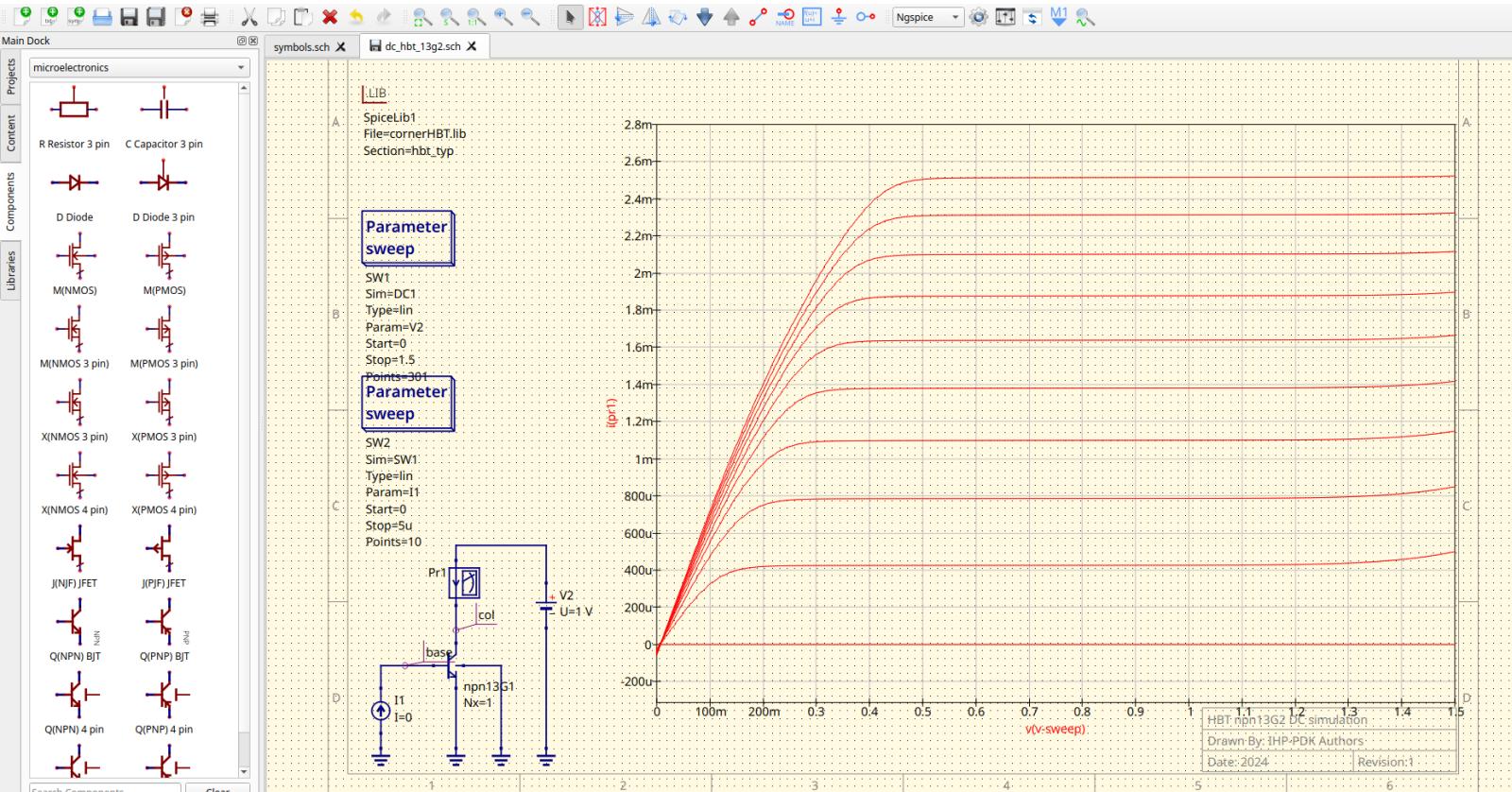
OpenPDK support for Qucs-S schematic capture



The current version of the IHP OpenPDK supports:

- o primitives for schematic capture
- o automatic ngspice/Xyce compatible netlist generation
- o example use cases to show the basic functionalities and parameters of the primitives
- o XSPICE model support (under development)

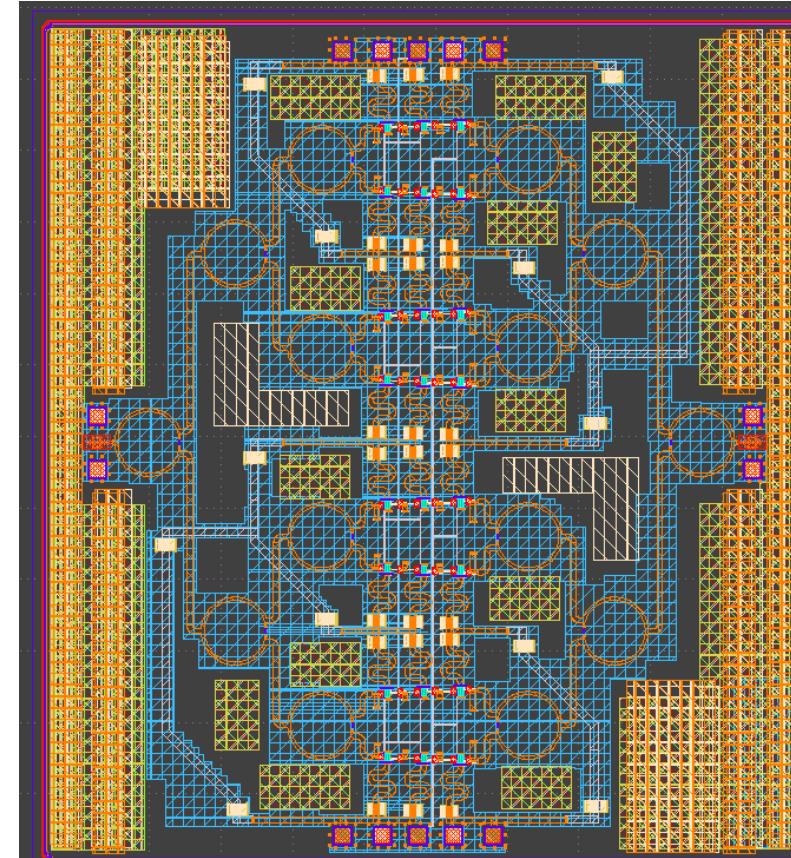
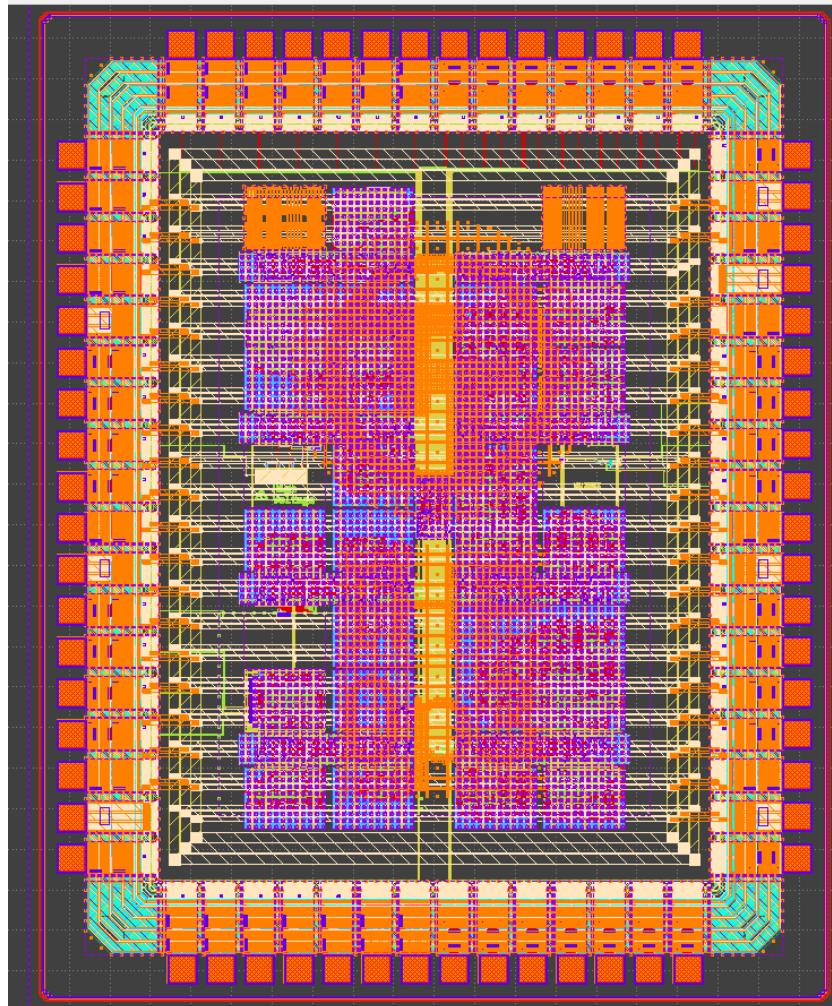
OpenPDK support for Qucs-S schematic capture



Qucs-S development:

- o Agnostic support for PDK
- o CDL netlisting
- o Interoperability with OpenEMS and Klayout
- o XML symbol library import
- o RF related features

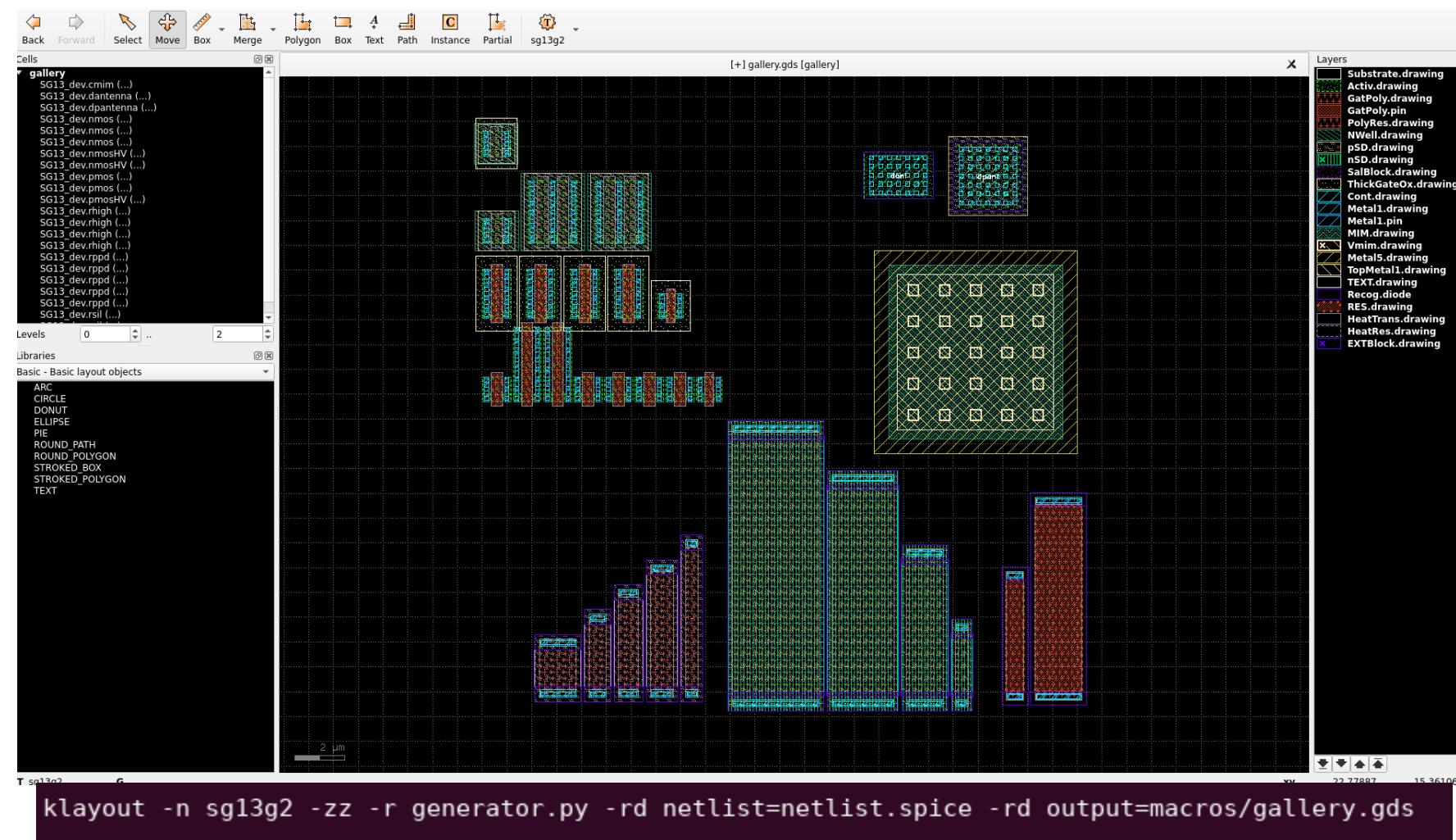
KLayout – primary tool for open source layout design



KLayout key features:

- o hierarchical view
- o parametric cell support
- o DRC/LVS checks
- o command line batch mode
- o XOR and DIFF tools
- o Custom scripts in Python/Ruby
- o Plugins

KLayout – Pycell support



- o Pycells compatible with Synopsys PyCell Studio and Keysight ADS
 - o KLayout wrapper API development
 - o Klayout Device generator

KLayout example DRC run on `gatpoly` QA cell



The screenshot shows the KLayout 0.28.12 interface with a project named "sg13g2_qacells.gds [gatpoly]".

Left Panel (Main View):

- Cells:** Shows the hierarchy: **gatpoly** > metal1 > nwell.
- Layers:** A list of layers including Activ.drw, GatPoly.drw, GatPoly.flr, Cont.drw, Metal1.drw, Metal1.pin, pSD.drw, NWell.drw, Substrate.drw, ThickGateOx.drw, and TEXT.drw.
- Marker Database Browser:** Shows the database "sg13g2.lyrdb" and the layout "sg13g2_qacells.gds".
- Marker Statistics:** A table showing marker counts:

Cell / Category	Count (Not Visited)
By Cell	37 (35)
[gatpoly]	37 (35)
aFil.g	1
aFil.g2	4 (4)
GFil.g	1
Gat.d	8 (8)
M1.j	1 (1)
M1Fil.h	4 (4)
Gat.a	12 (12)
Gat.b	6 (6)
By Category	37 (35)
All	37 (35)
- Info:** Min. GatPoly to Activ space = 0.07

Right Panel (Marker Database Browser):

- Database:** sg13g2.lyrdb
- ... on layout:** sg13g2_qacells.gds
- Directory:** Shows the marker categories and their counts.
- Markers:** A list of markers with icons and checkboxes.
- Info:** Shows the minimum space requirement for the selected marker "Gat.d [gatpoly]".

KLayout example LVS run on sg13_lv_nmos mosfets



Netlist LVS

... on layout sg13_lv_nmos.gds

Netlist Schematic Cross Reference Log

Circuits Objects Layout Reference

sg13_lv_r sg13_lv_nmos ↔ \$ sg13_lv_nmos SG13_LV_NMOS

↳ Pins
↳ Nets
↳ Devices

- ↳ sg13_lv_nn \$11 / sg13_lv_nmos [L=(N1 / SG13_LV_NMOS [L=0.13, W=0.15]
- ↳ sg13_lv_nn \$12 / sg13_lv_nmos [L=(N2 / SG13_LV_NMOS [L=0.13, W=0.2]
- ↳ sg13_lv_nn \$14 / sg13_lv_nmos [L=(N3 / SG13_LV_NMOS [L=0.15, W=0.2]
- ↳ sg13_lv_nn \$9 / sg13_lv_nmos [L=0. N4 / SG13_LV_NMOS [L=0.15, W=0.3]
- ↳ sg13_lv_nn \$6 / sg13_lv_nmos [L=0. N5 / SG13_LV_NMOS [L=0.3, W=0.3]
- ↳ sg13_lv_nn \$13 / sg13_lv_nmos [L=(N6 / SG13_LV_NMOS [L=0.25, W=0.6]
 - ↳ S ↔ D ⚠ \$35 (1) D6 (2)
 - ↳ D ↔ S ⚠ \$36 (1) S6 (2)
 - ↳ G \$37 (1) G6 (2)
 - ↳ B \$1 (26) SUB (27)
- ↳ sg13_lv_nn \$16 / sg13_lv_nmos [L=(N7 / SG13_LV_NMOS [L=0.15, W=0.6]
- ↳ sg13_lv_nn \$4 / sg13_lv_nmos [L=3. _PATTERN_37 / SG13_LV_NMOS [L=3.74, W=5.55]
- ↳ sg13_lv_nn \$5 / sg13_lv_nmos [L=4. _PATTERN_40 / SG13_LV_NMOS [L=4.6, W=7.09]

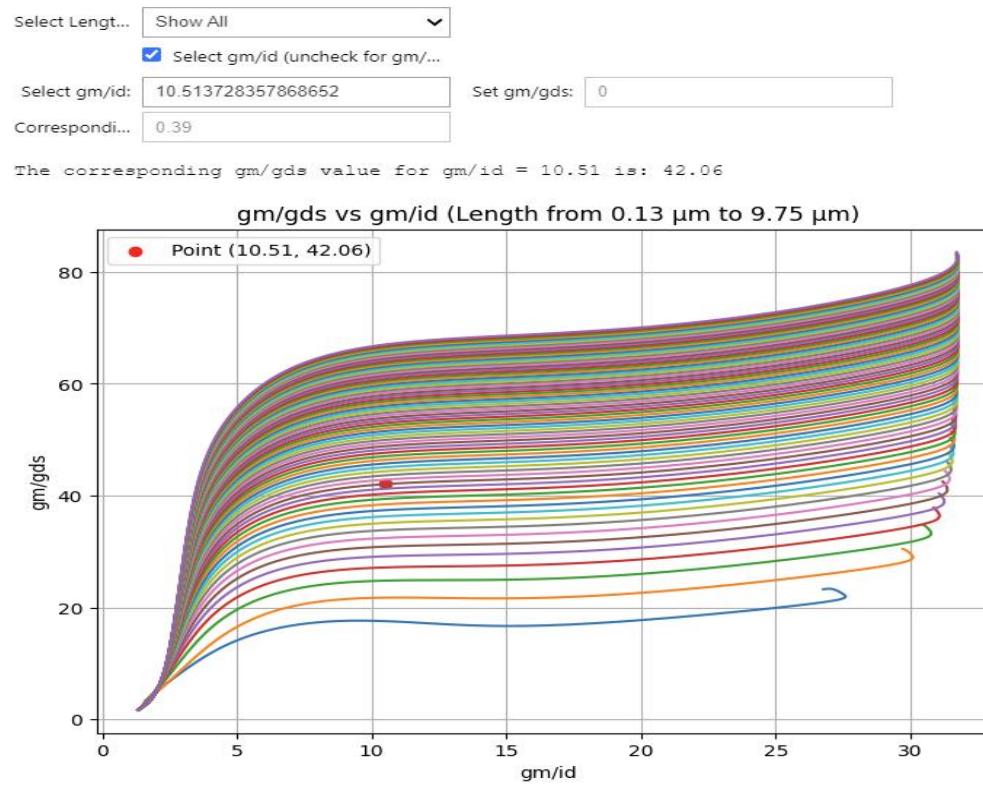
KLayout LVS ruledeck:

- o accepts CDL netlist,
- o extracts devices from layout,
- o creates extracted netlist,
- o performs checks and compares:
 - o Pins
 - o Nets
 - o Devices
- o reports inconsistencies
- o can run in batch mode

OS tools for Advanced IC Design?

MOSFET Sizing with GM/ID Curves:

- 0 Using Python scripting alongside Ngspice to generate GM/ID curves for efficient MOSFET sizing



Mixed Signal Design

- 0 Verilator
- 0 Xspice
- 0 Creating digital models in conjunction with analog design

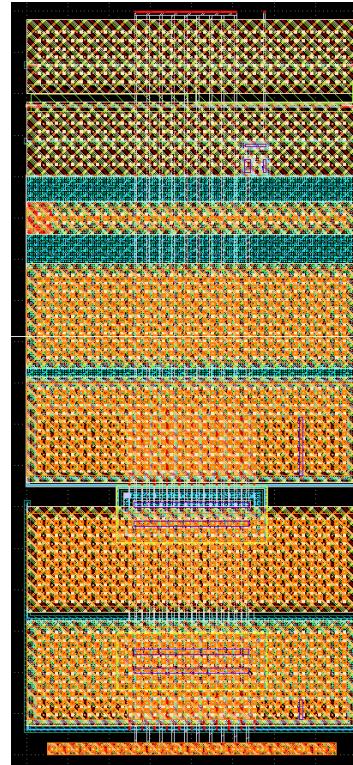
Layout Automation

- 0 Physical verification, filler scripts
- 0 Pcells generation from SPICE-Files
- 0 Streamlining the layout process

Digital primitives

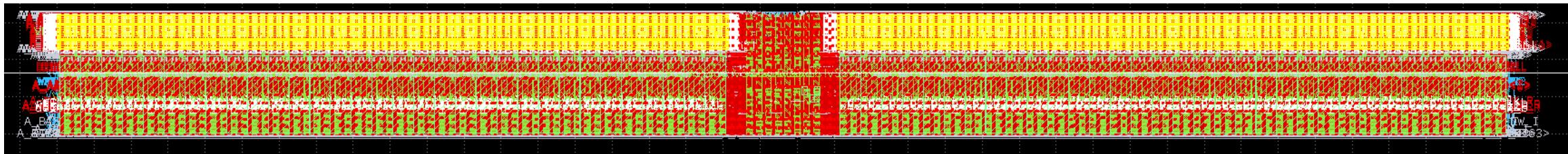
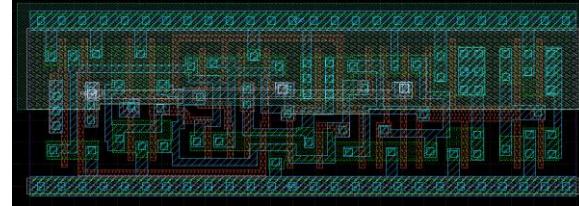


	StdCells	IOCells	SRAM
Verilog	x	x	x
LIB	x	x	x
LEF	x	x	x
CDL	x	x	x
SPICE	x	x	x
GDS	x	x	x

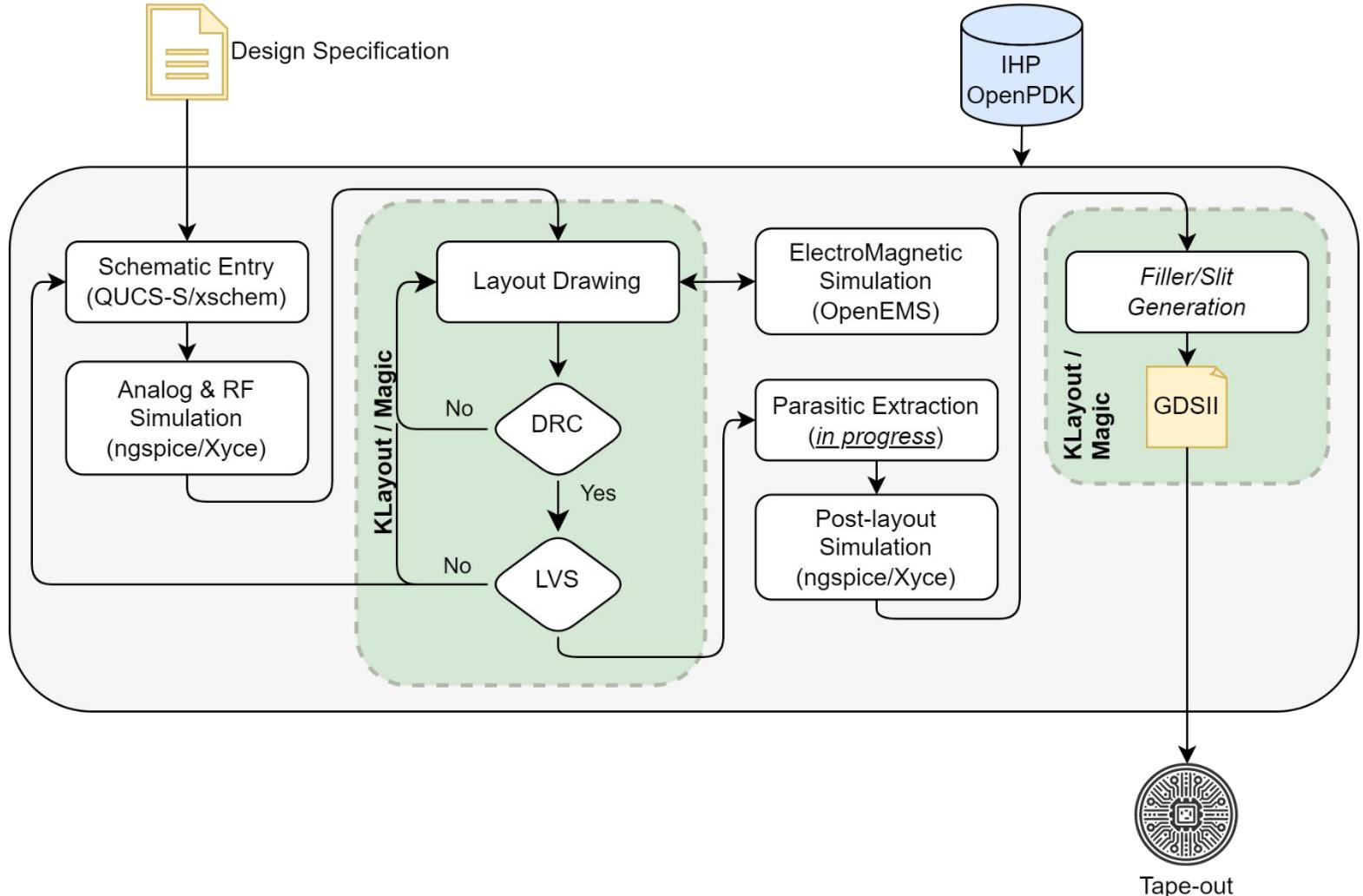


Digital components:

- 0 stdcells
 - 0 84 cells,
 - 0 combinational logic,
 - 0 sequential elements,
 - 0 scan flops,
 - 0 gated cells.
- 0 IOCells,
 - 0 In, Out, InOut, Analog
 - 0 different drive strengths
- 0 SRAM
 - 0 hard macros of a single port SRAM
 - 0 different sizes

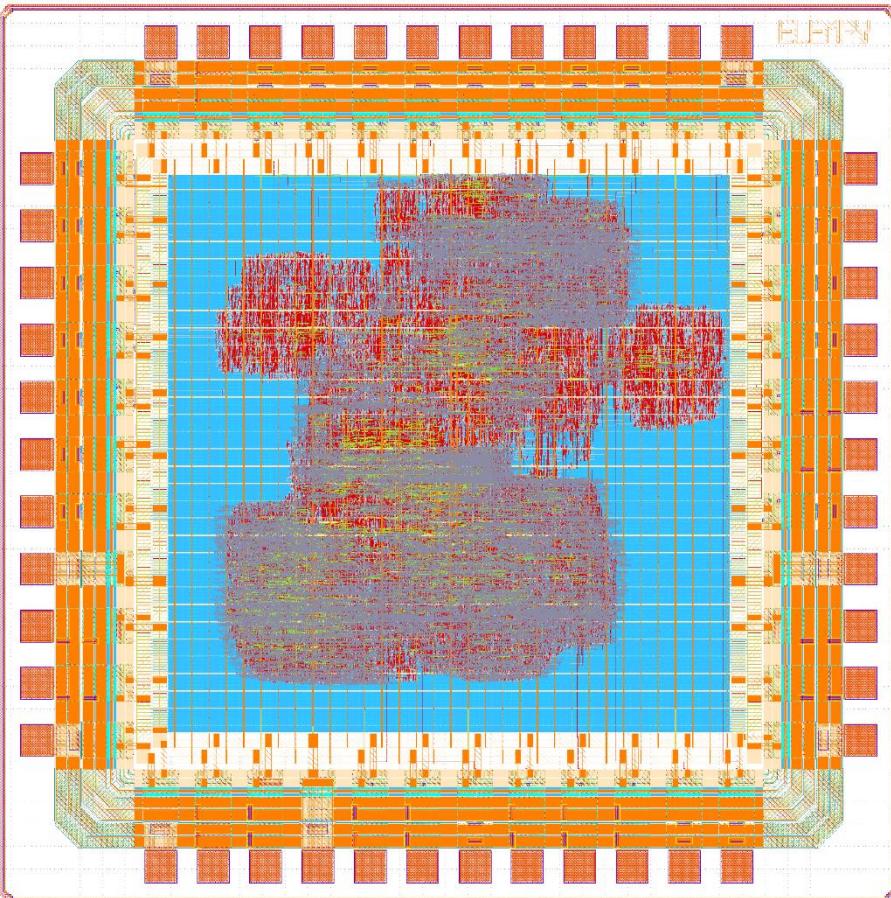


Analog/RF Open Source Design Flow: status at a glance

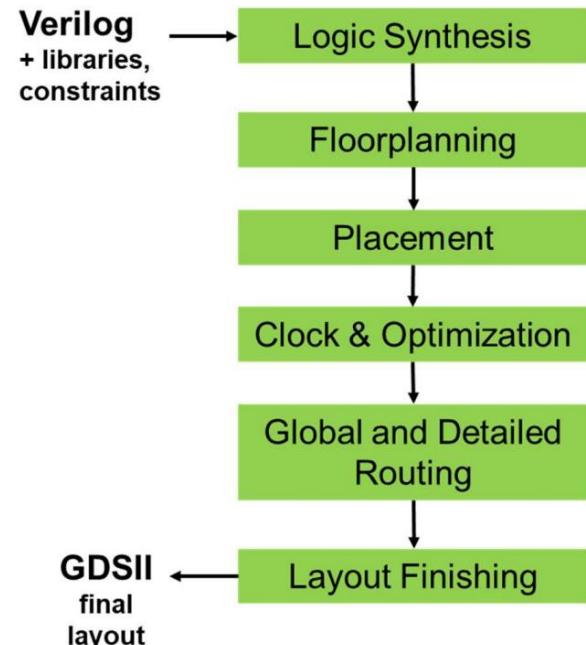
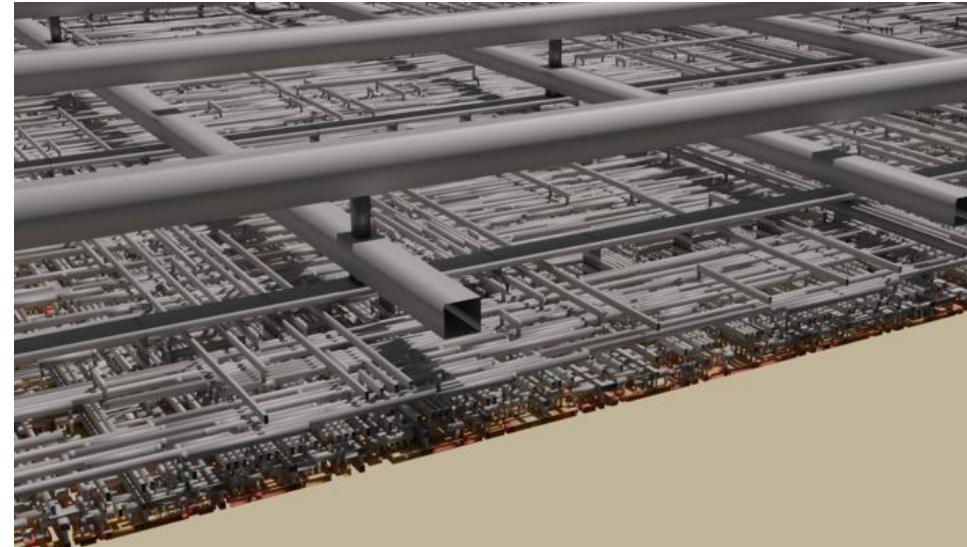


- 0 KLayout-oriented flow
 - 0 Layout design
 - 0 Parameterizable cells
 - 0 Physical Verification
- 0 QUCS-S, xschem
- 0 ngspice, Xyce
- 0 OpenEMS, ElmerFEM, AWS Palace
- 0 Working on a faster solver for EMS (ELMER)

Digital OpenROAD-flow-scripts Flow



- o Yosys + ABC -> synthesis
- o OpenROAD -> PnR
- o Klayout -> GDS streaming+checks

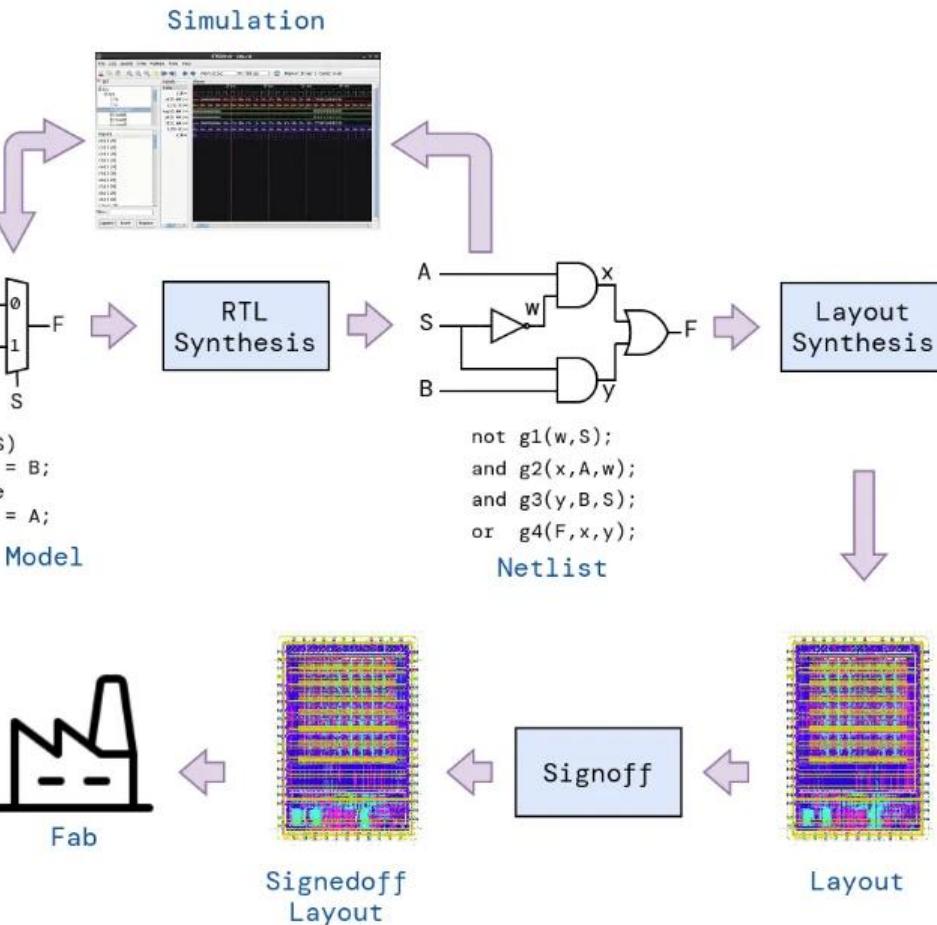


<https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts>

Digital LibreLane flow



IDEA



<https://github.com/librelane/librelane>

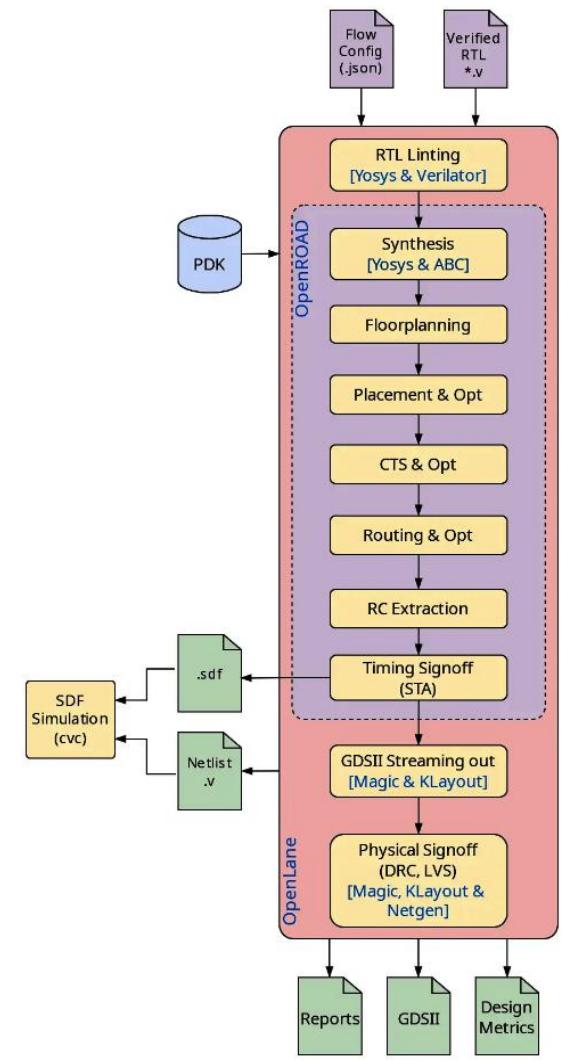


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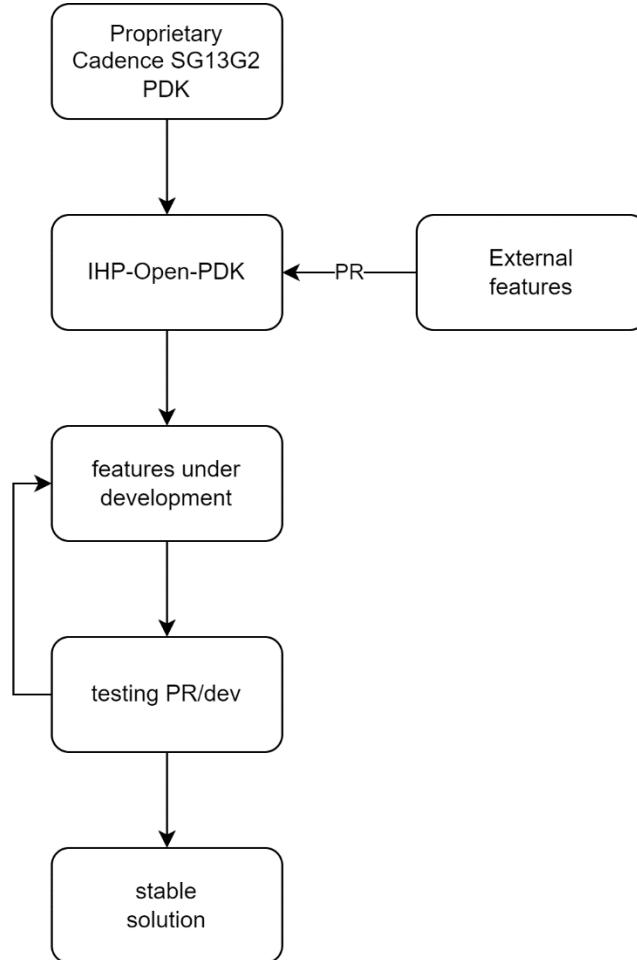
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PDK development cycle

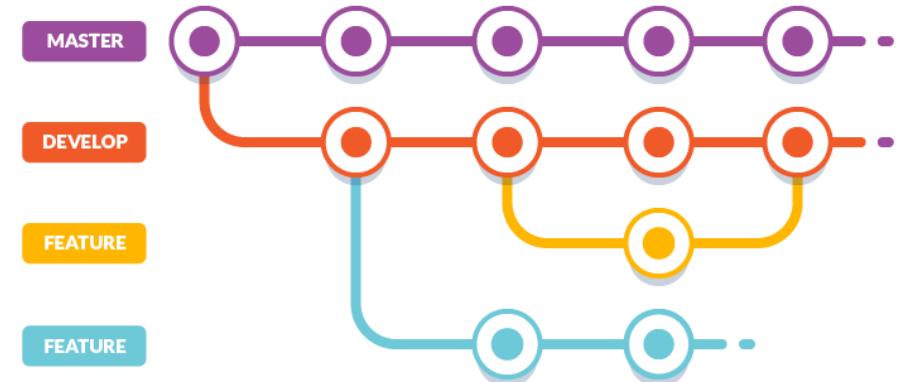


Principal rules

- Tight link between SG13G2 PDK and its open-source equivalent
- Compatibility with the open-source EDA tools
- Preserving the structure proposed in SKY130
- Read-only
- Based on git and following git flow

Key actors

- PDK core team
- Tools and flow developers
- Designers
- OS Community



PDK development cycle – community support



Issues 135 Pull requests 24 Discussions Actions Projects 1 Wiki Issues 135 Pull requests 24 Discussions Actions Projects 1 Wiki

is:issue	
<input type="checkbox"/>	Open 135 Closed 165
Author ▾ Labels	
<input type="checkbox"/>	Cannot run simulation on test scheme #566 · by thonglinh90 was closed yesterday
<input type="checkbox"/>	Questions about sealring For MPW shuttle runs question #562 · EngGhaith opened 4 days ago
<input type="checkbox"/>	Xyce plugins support limited to only 2 plugins bug #560 · KrzysztofHerman opened 4 days ago
<input type="checkbox"/>	Double prefix in stdcell names in verilog netlist created by xschem bug #557 · by FlinkbaumFAU was closed 4 days ago
<input type="checkbox"/>	Discrepancy in LVS Netlist Extraction for Parallel Capacitors #555 · PhillipRambo opened last week

Filters ▾	Search is:pr is:open
<input type="checkbox"/>	24 Open ✓ 231 Closed Author ▾
<input type="checkbox"/>	Code changes fixes the problem that Xyce/ADMS can't handle switch... × #568 opened 10 hours ago by dwarning
<input type="checkbox"/>	Adding some updates for LVS run setup and actions ✓ #567 opened yesterday by FaragElsayed2
<input type="checkbox"/>	Stdcell update 2. Hot Fix 1. ✓ #565 opened 3 days ago by b10346
<input type="checkbox"/>	Changes in Act and GatPoly filler macro. ✓ #564 opened 3 days ago by KrzysztofHerman
<input type="checkbox"/>	Added bulk node to resistor models rhigh + rppd + rsil cont. ✓ #563 opened 3 days ago by KrzysztofHerman • Draft
<input type="checkbox"/>	Xyce plugins sourced from a plugin list ✓ #561 opened 4 days ago by KrzysztofHerman • Draft

Work in progress – analog/mixed/RF flow



- 0 Parasitics Extraction PEX – ongoing, <https://github.com/martinjankoheler/klayout-pe>
- 0 Noise modeling in ngspice (transient noise, low frequency noise) – ongoing
- 0 Qucs-S support – ongoing, agnostic PDK support, RF features
- 0 Device models – issues found and reported by community members, migration to Verilog-A behavioral models
- 0 New and fast DRC ruledeck for klayout
- 0 OpenEMS integration for EM field solving
- 0 Mixed mode testcases using xspice + verilator

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Our motivation and goals in the open source silicon domain

Description of the open source solutions developed and supported by IHP

Understanding the power of the community

Planification of Open MPW runs

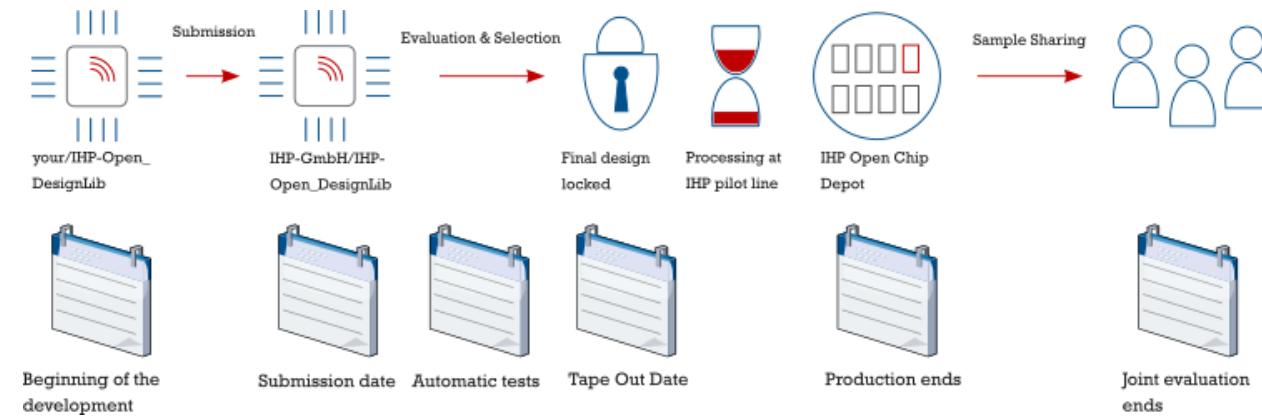
How do we make the PDK ? ?

Free MPW Runs - support open source PDK & design

- 0 The table provides schedule of MPW Runs for FMD-QNC project in 2024 and 2025

Tape out date	22/05/24	11/11/24	22/11/24	01/03/25	09/05/25	18/07/25	15/09/25
Technology	SG13G2	SG13CMOS	SG13G2	SG13G2	SG13G2	SG13G2	SG13CMOS
Area [mm ²]	10	220	20	140	30	30	220

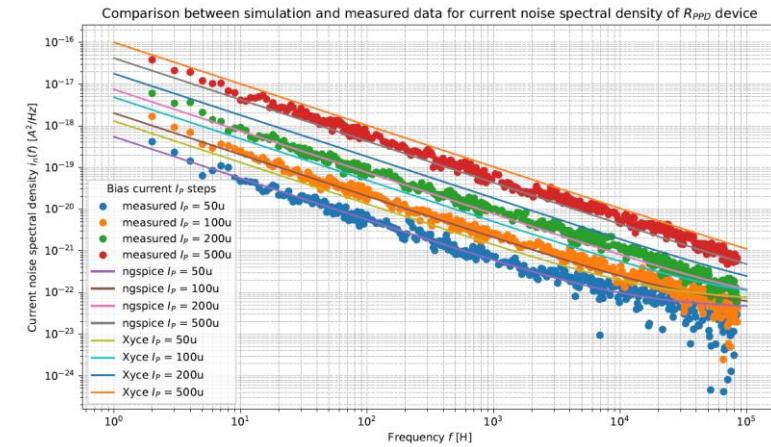
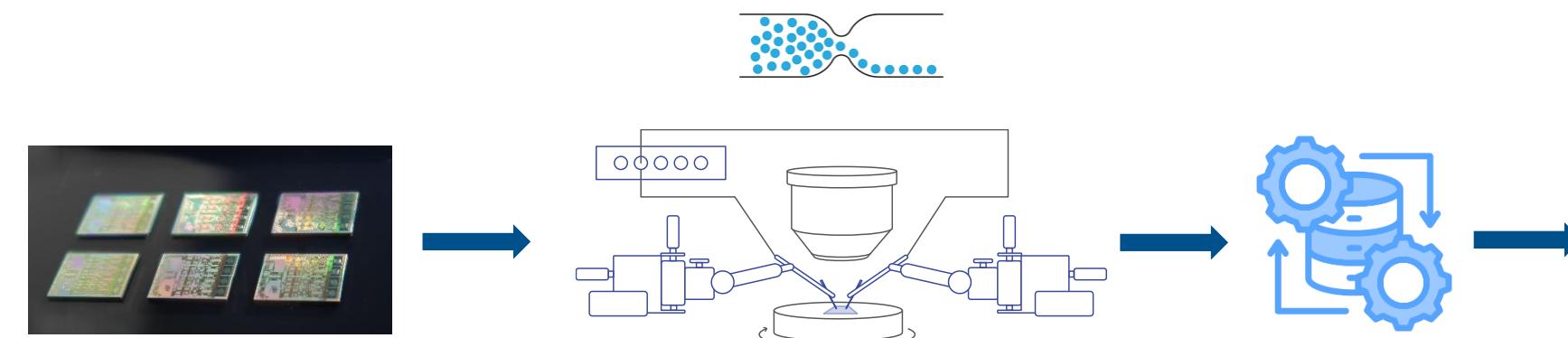
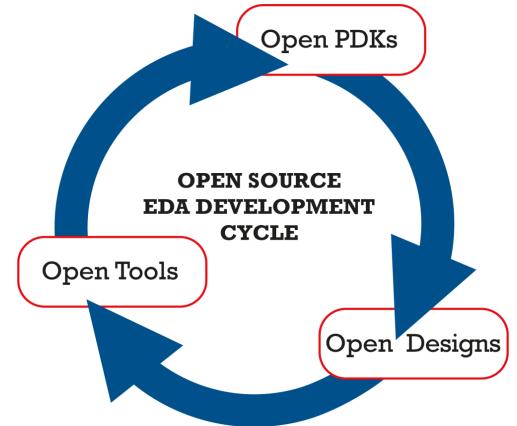
For more details check: <https://ihp-open-ip.readthedocs.io/en/latest/>



- 0 Project funds can be used exclusively to produce chip designs for non-economic activities, such as university education, research projects, and others
- 0 A concept for sustainable provision of free or low-cost MPW area for the open source community is to be developed.

The future – Joint Evaluation

- 0 Receiving your own silicon is just one milestone—it doesn't mean the development cycle is complete.
- 0 The samples/wafers from free OpenMPW will be stored at IHP
- 0 Anybody can rent chips for measurements
- 0 Silicon cross validation as research good practices
- 0 Verified IP can become part of an open-source design library
- 0 How to organize the measurement to balance the load of the measurements lab ?**
- 0 How to organize the data processing ?**



The future – European Chip Design Platform with open-source



- 0 Chips JU initiative
- 0 Cloud based design environment with EDA tools, flows and IP's
- 0 Open source is part of the platform: Analog, RF, AMS, Digital and Photonics related tools, flows
- 0 Open-source design library: open source IP's

DCT

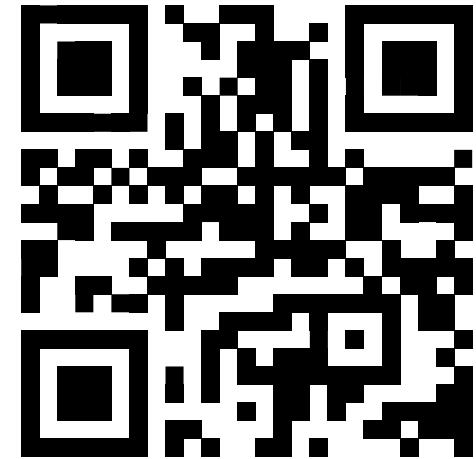
DET

DET

DET



DET call is open right now – ChipFlow will apply so contact Rob Taylor for more details



The future - Low cost MPW



In order to maintain open source MPW IHP plans to have two OpenMPW runs per year

- 0 SG13CMOS – CMOS only run with AL BEOL where price „P” in EUR is calculated based on total area (mm^2) „A” booked

$$P = \begin{cases} - & \text{if } A < 100 \\ 150000/A & \text{if } 100 \leq A \leq 150 \\ 1000 & \text{if } A > 150 \end{cases}$$

- 0 SG13G2 – fully featured G2 with AL BEOL at approx. 2800 EUR/ mm^2

The above mentioned prices refer to the open-source designs, where all the views are compatible with the open source EDA tools.

For customers who do not wish to disclose their IP, we offer participation in the OpenMPW program at a 20% discount off the regular price, as the wafers can be shared with other customers.

The turn around processing time is approx. 6 months for CMOS - 8 months for BiCMOS

The typical offer includes 20 bare die samples. Packaging will be offered on request (additional fee can be applied)

The first run can take place 24-th Nov 2025 (CMOS)

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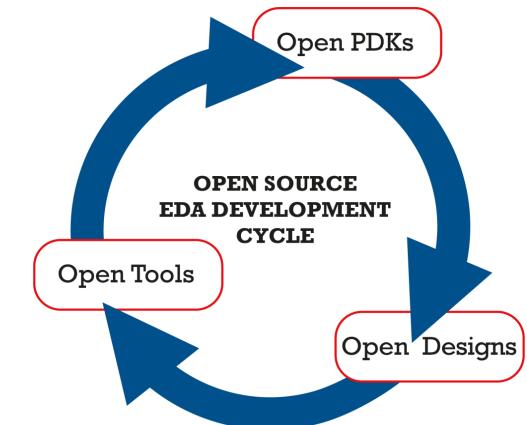
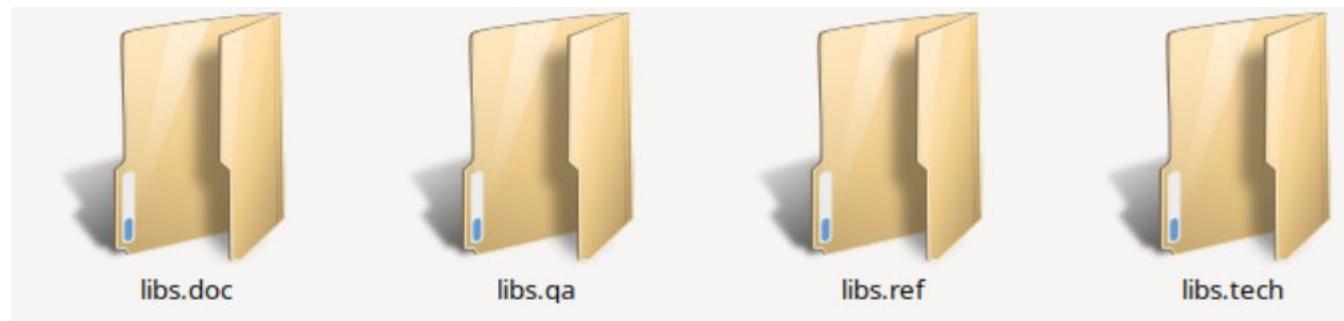
Planification of Open MPW runs

How do we make the PDK ? ?

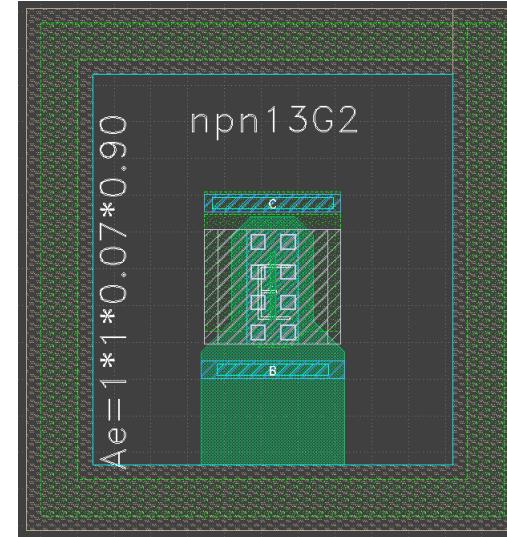
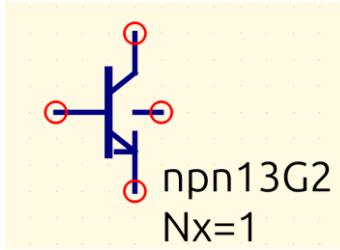
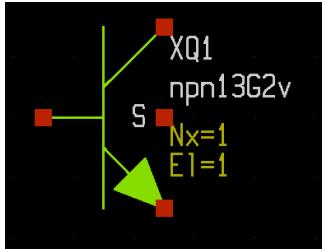
How do we make the IHP-Open-PDK ?

Key development rules of IHP-Open-PDK:

- o Compatibility with technology – PDK is defined by technology
- o Compatibility with the open-source tools (standarization, dependencies)
- o Tight link between Cadence SG13G2 PDK and its open-source version
- o Four+ eyes principle – review process



Device integration process



- o \$PDK_ROOT/\$PDK/libs.tech/xschem/sg13g2_pr/npn13G2.sym
- o \$PDK_ROOT/\$PDK/libs.tech/xschem/sg13g2_tests/
- o \$PDK_ROOT/\$PDK/libs.tech/qucs-s/user_lib/IHP_nonlinear...*.lib
- o \$PDK_ROOT/\$PDK/libs.tech/qucs-s/examples/
- o \$PDK_ROOT/\$PDK/libs.tech/ngspice/model/cornerHBT.lib
- o \$PDK_ROOT/\$PDK/libs.tech/xyce/model/cornerHBT.lib
- o \$PDK_ROOT/\$PDK/libs.tech/verilog-a/vbic/vacode/vbic_1p3.va
- o \$PDK_ROOT/\$PDK/libs.tech/klayout/python/sg13g2_pycell_lib/ihp
- o \$PDK_ROOT/\$PDK/libs.tech/magic/ *ongoing
- o \$PDK_ROOT/\$PDK/libs.tech/klayout/tech/drc
- o \$PDK_ROOT/\$PDK/libs.tech/klayout/tech/lvs

Check list:

- o Xschem symbol
- o Qucs-S symbol
- o Ngspice model
- o Xyce model
- o Verilog-A model
- o Xschem example
- o Qucs-S example
- o Klayout PyCell
- o Magic Pcell
- o DRC -test
- o LVS extraction rules
- o LVS - test

Device model development

Current modelling approach:

- 0 Based on Spice
- 0 Partially supported by Verilog-A models via OSDI interface

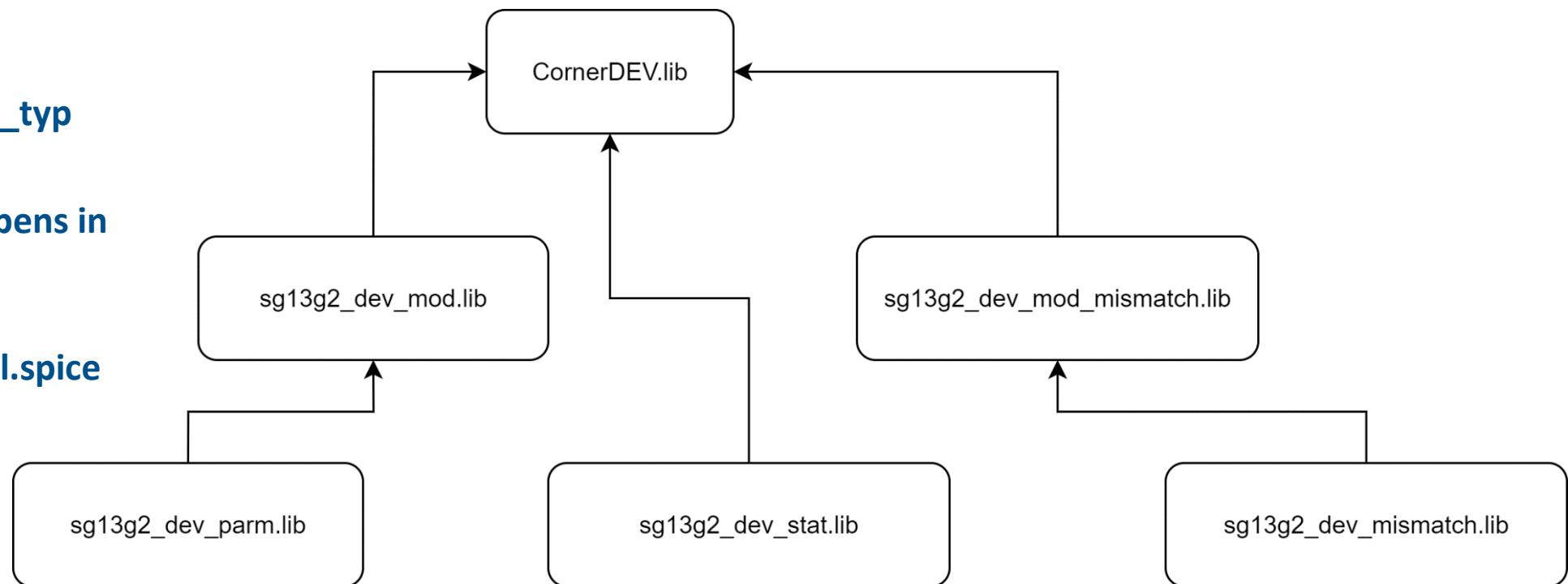
Corners:

- 0 dev_typ, dev_bcs, dev_wcs, dev_typ_stat
- 0 mos_tt, mos_ff, mos_ss, mos_fs, mos_sf, mos_tt_stat

.lib CornerDEV.lib dev_typ

The actual magic happens in
\$HOME/.spiceinit

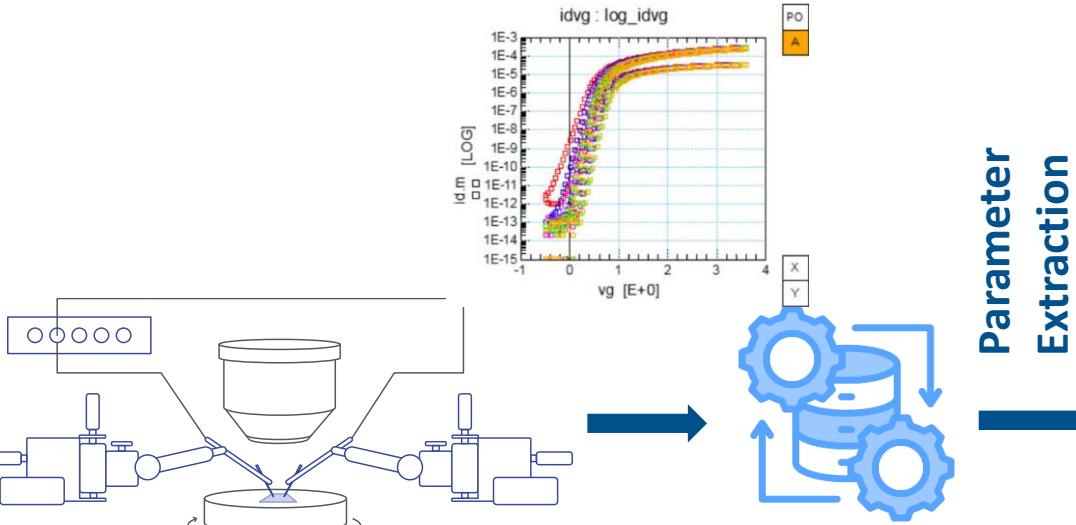
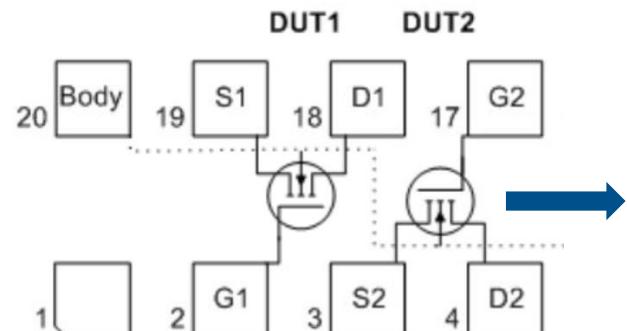
.include sg13g2_stdcell.spice



Device model development

Current modelling approach:

- 0 Industrial flow uses Keysight ICCAP
- 0 Measurements are taken for different conditions: temperature
- 0 Multiple measurements -> statistics (process, global variation)
- 0 Co-simulation spectre, hspice, ngspice



Alternative open-source flow:

- 0 Device Modeling Toolkit by Semimod
- 0 co-simulation with ngspice
- 0 Verilog-A modelcards support

```
.model npn13G2_NX_vbic npn
+ level = 9
+ vbe_max = 1.6
+ vbc_max = 5.1
+ vce_max = 1.6
+ tnom = 27
+ cbeo = '8.00E-16*(Nx*0.25)**0.975'
+ cje = '8.418E-15*(Nx*0.25)**0.975*vbic_cje'
+ pe = 0.92
+ me = 0.12
+ aje = -0.50
+ wbe = 1.00
+ cbco = '2.36E-15*(Nx*0.25)'
+ cjc = '1.53E-15*(Nx*0.25)*vbic_cjc'
+ pc = 0.558
+ mc = 0.12
+ ajc = -0.50
+ cjep = '3.56E-15*(Nx*0.25)*vbic_cjc'
```

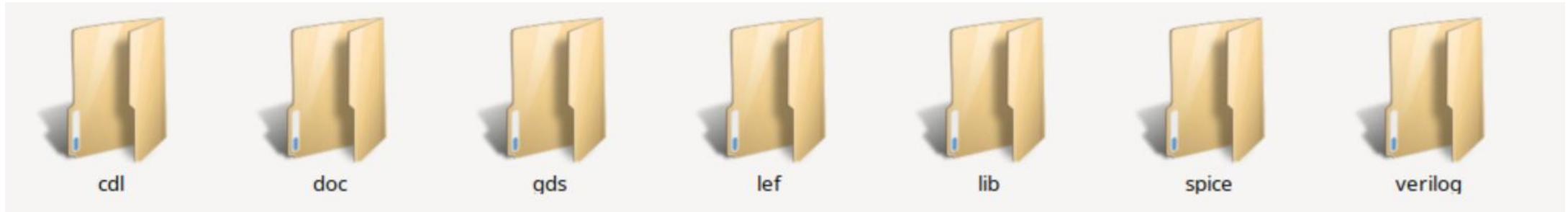
Standard cells development

Standard cells reverse engineering:

- o GDS -> CDL
- o CDL->SPICE
- o SPICE->LIB
- o CDL->Verilog
- o GDS->LEF

Stdcell alternative open-source flow:

- o Verilog
- o Schematic/Spice netlist
- o SPICE->LIB (lctime, libretto, CharLib)\
- o SPICE->GDS Iclayout
- o GDS->LEF (Magic)

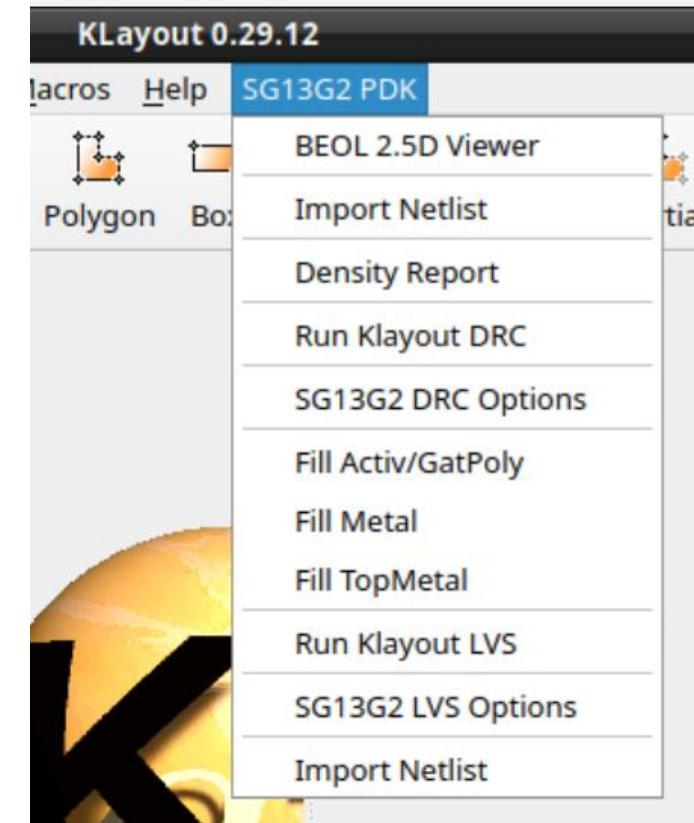


Physical verification is critical

- 0 Klayout DRC rule deck is written in RUBY
- 0 \$PDK_ROOT/\$PDK/libs.tech/klayout/tech/drc
- 0 be careful when running DRC during submission it is only a foundry precheck

- 0 Klayout LVS rule deck is written in RUBY
- 0 \$PDK_ROOT/\$PDK/libs.tech/klayout/tech/lvs

- 0 performance – populate jobs on multicore up to 24
- 0 be careful with RAM

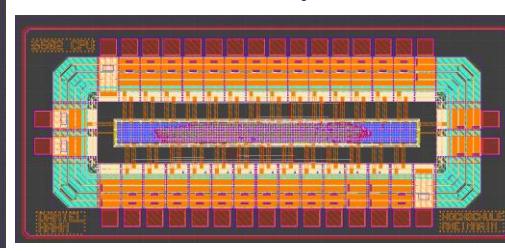
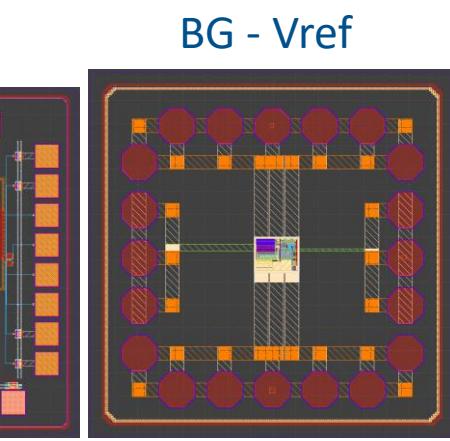
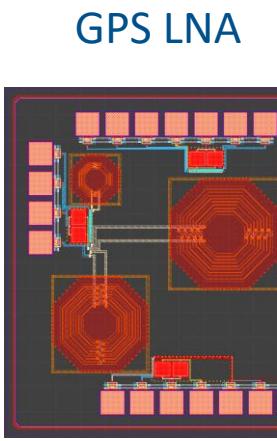
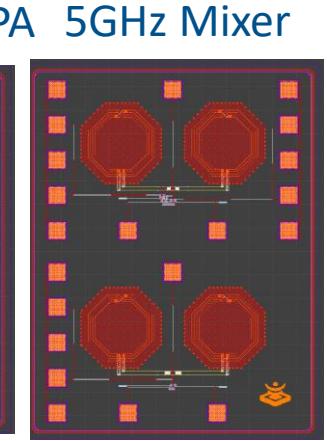
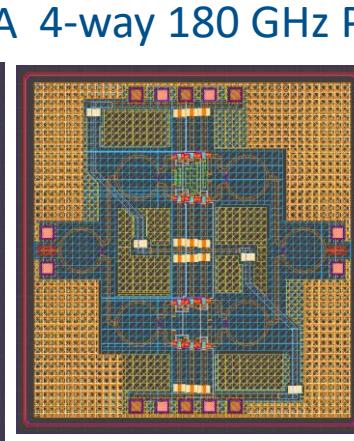
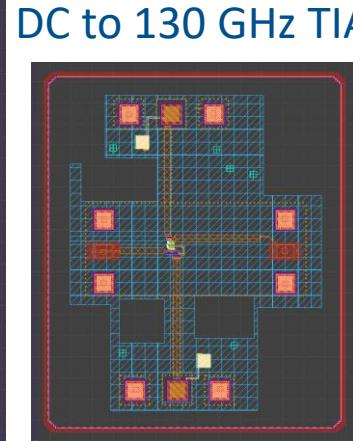
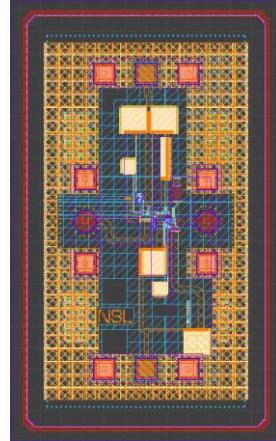


Open-source design library

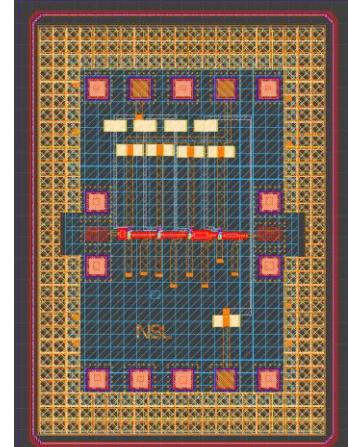


In principle the Design Library does not exist yet but...

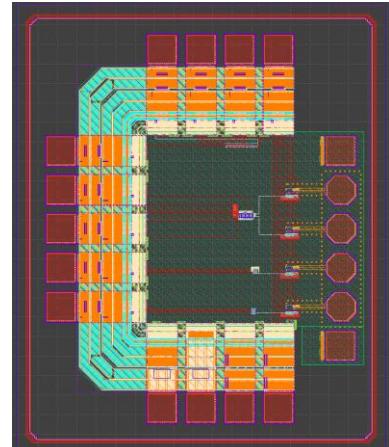
97 GHz TIA



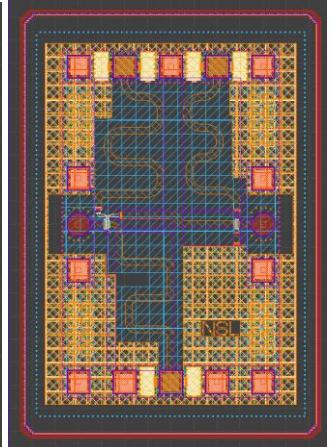
160 GHz LNA



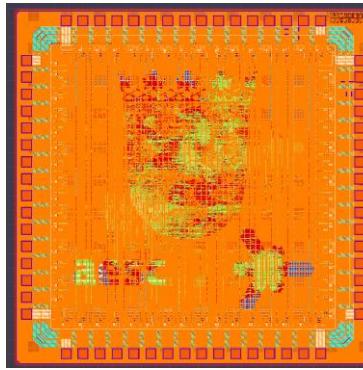
Active L VCO



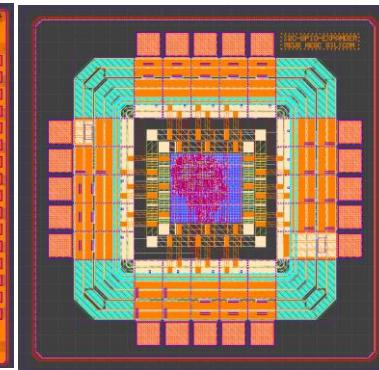
40 GHz LN TIA



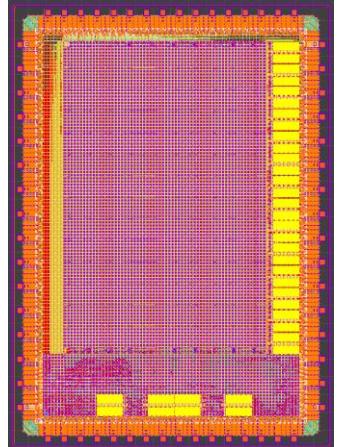
ElemRV-N



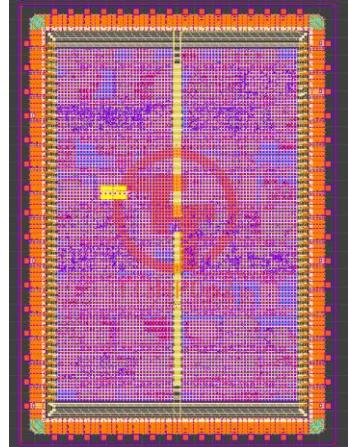
I2c-gpio-expander



Greyhound



2x TT





How to reach us

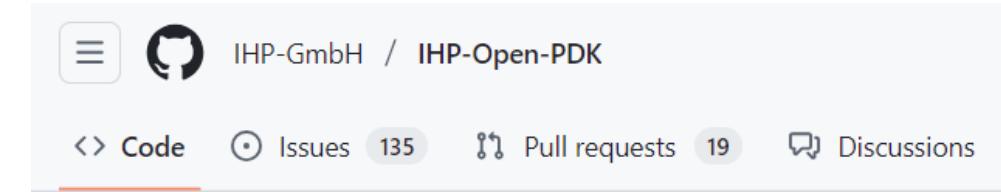
Email

-0 openpdk@ihp-microelectronics.com



GitHub

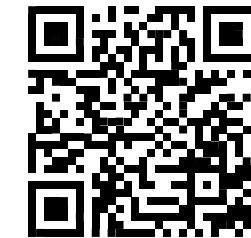
-0 issues – for reporting issues, questions



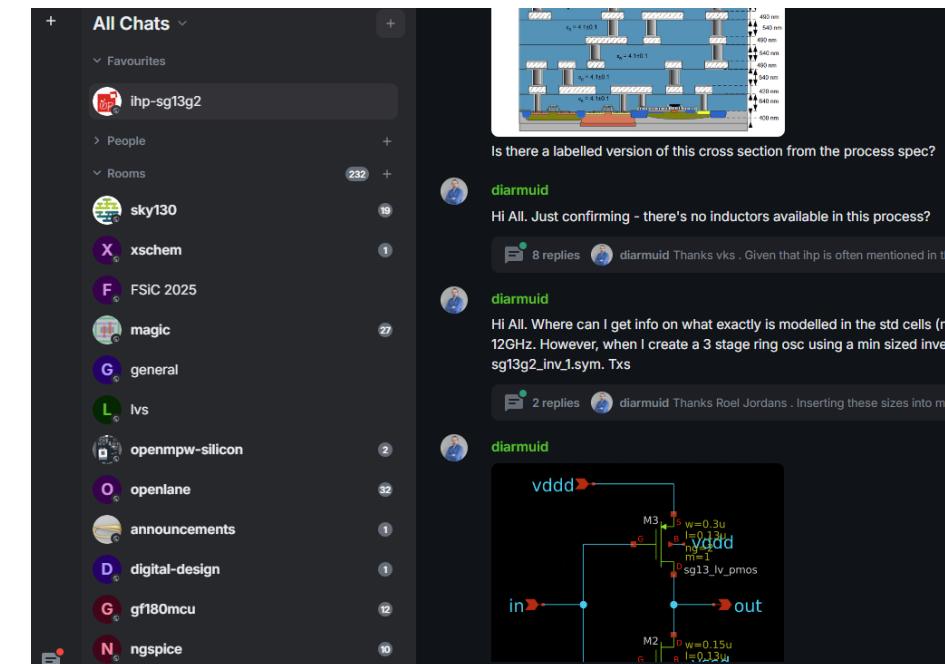
-0 discussions – for requesting features

Open Source Fossi-Chat.org channel:

#ihp-sg13g2



-0 general discussions





Funding opportunities

<https://nlnet.nl/>

[Amaranth HDL](#)

Design FPGAs and ASICs in Python

[Apicula IO primitives](#)

Add additional IO primitives to libre Gowin FPGA tools

[FABulous Demo SoC](#)

SoC with open source FPGA based on FABulous

[FPGA-ISP-UVC-USB2](#)

Open hardware FPGA-based USB webcam

[LiteX](#)

Developer framework for FPGA and ASIC designs

[LibreSilicon: Pad Cell Generator](#)

Custom pad cells for integrated chip layout generation

[Test Procedures for MOSFET SPICE Model Validation](#)

[pcb-rnd, sch-rnd](#)

Open source EDA suite

Send in your ideas. Deadline October 1, 2025

Acknowledgements



To BMFTR -> FMD-QNC (16ME0831) <https://www.elektronikforschung.de/projekte/fmd-qnc>

To our team at IHP



Join our team:

- open positions
- student's internship

To all members of the open-source community who have supported and contributed our initiatives



Thank you for your attention!

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