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Analysis and Design of a Multiple Feedback Loop Control Strategy for Single-Phase Voltage-Source UPS Inverters

Naser M. Abdel-Rahim, *Student Member, IEEE,* and John E. Quaicoe, *Senior Member, IEEE*

***Abstract*— This paper presents the analysis and design of a multiple feedback loop control scheme for single-phase voltage-source uninterruptible power supply (UPS) inverters with an L-C filter. The control scheme is based on sensing the current in the capacitor of the load filter and using it in an inner feedback loop. An outer voltage feedback loop is also incorporated to ensure that the load voltage is sinusoidal and well regulated. A general state-space averaged model of the UPS system is first derived and used to establish the steady-steady quiescent point. A linearized small signal dynamic model is then developed from the system general model using perturbation and small-signal approximation. The linearized system model is employed to examine the incremental dynamics of the power circuit and select appropriate feedback variables for stable operation of the closed-loop UPS system. Experimental verification of a laboratory model of the UPS system under the proposed closed-loop operation is provided for both linear and nonlinear loads. It is shown that the control scheme offers improved performance measures over existing schemes. It is simple to implement and capable of producing nearly perfect sinusoidal load voltage waveform at moderate switching frequency and reasonable size of filter parameters. Furthermore, the scheme has excellent dynamic response and high voltage utilization of the dc source.**

I. Introduction

UNINTERRUPTIBLE POWER supplies (UPS's) are used to interface critical loads such as computers and communication systems to the utility system. The output voltage of the UPS inverter is required to be sinusoidal with minimum total harmonic distortion. This is usually achieved by employing a combination of pulse-width modulation (PWM) scheme and a second-order filter at the output of the inverter.

One way of achieving a "clean" sinusoidal load voltage is by using a sine pulse width modulation (SPWM) scheme [1], [2]. In this technique, the load voltage is compared with a reference sinusoidal voltage waveform and the difference in amplitude is used to control the modulating signal in the control circuit of the power inverter. A more advanced technique employs a programmed optimum PWM scheme that is based on the harmonic elimination technique [3], [4]. These schemes have been shown to perform well with linear loads. However, with nonlinear loads the PWM scheme does not guarantee low distortion of the load voltage.

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To overcome this drawback, a real-time feedback control scheme using dead-beat control was proposed [5], [6]. This technique employs the capacitor voltage and its derivative in a control algorithm to calculate the duration of the ON/OFF states of the inverter switching devices such that the capacitor voltage is exactly equal to the reference voltage at the next sampling time. Although this technique has been successfully implemented for single- and three-phase applications, it has the following drawbacks: 1) it is complex to implement; 2) it is sensitive to parameter variations; and 3) its control algorithm requires the estimation of the load parameters [7].

In order to achieve a control scheme that overcomes the above disadvantages, a current regulated control scheme for dc/ac applications was proposed in [8]. In this technique, the current in the filter capacitor is used as the feedback variable in a two-switch inverter circuit topology to achieve a sinusoidal capacitor current. An outer voltage control loop is also incorporated for load voltage regulation and compensation for imperfections in the implementation of the current control loop.

Although the technique results in a sinusoidal capacitor current, the power circuit configuration and the switching scheme used to implement the technique produce a load voltage that is sinusoidal with dc offset. For UPS applications, the presence of the dc voltage offset is unacceptable.

This paper investigates the suitability of a current-regulated voltage-controlled strategy for a single-phase voltage-source half-bridge inverter with a second-order filter. The scheme incorporates an inner capacitor current loop, an outer capacitor voltage loop, a fixed switching frequency, and variable duty cycle approach to produce sinusoidal output voltage with minimum harmonic distortion. The fixed switching frequency approach produces a defined frequency spectrum at the inverter output, which makes it easier to design an electromagnetic interference filter to prevent interference with communication circuits.

The paper is organized as follows: Section II provides the steady-state performance of the UPS system under open-loop control. A procedure for selecting appropriate feedback variables that result in a stable operation of the closed-loop system is provided in Section III. The proposed control strategy is proposed in Section IV. Section V presents a design procedure for selecting the gains of the inner and outer feedback loops. The control block of the proposed control strategy, its principle of operation, computer simulation, and

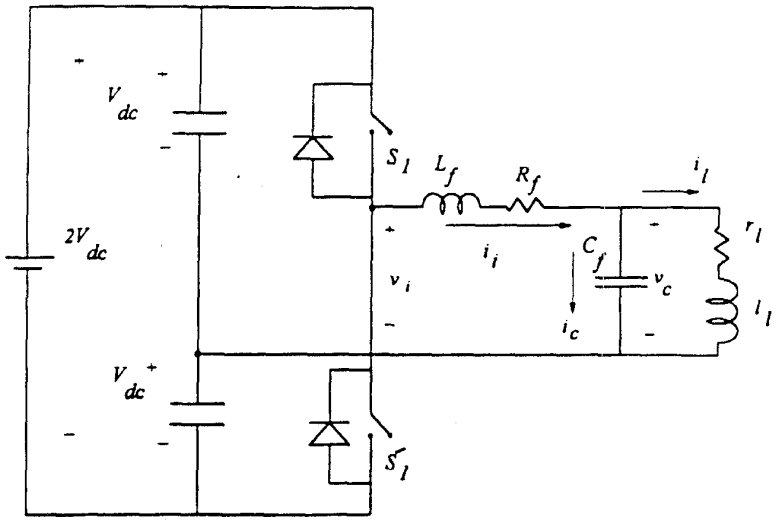


Fig. 1. The single-phase half-bridge UPS inverter.

experimental verification are presented in Section VI. Finally, conclusions are drawn in Section VII.

II. Analytical Model of the Open-Loop System: Steady-State Performance

Fig. 1 shows the circuit diagram of the single-phase half-bridge voltage-source UPS inverter. It consists of a load filter (L_f and C_f) and an R-L load.

The system differential equations can be written in state-space form as

$$\frac{d}{dt}\begin{bmatrix} i_i(t) \\ i_l(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & 0 & \frac{-1}{L_f} \\ 0 & \frac{R_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & \frac{-1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i(t) \\ i_l(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}(2S_1^* - 1)}{L_f} \\ 0 \\ 0 \end{bmatrix} \tag{1}$$

where $S_1^* = 1$ when S_1 is ON and $S_1^* = 0$ when S_1 is OFF.

Equation (1) is discontinuous due to the presence of the switching function S_1^*. One way of studying the system performance and characterizing its behavior is to solve (1) numerically and simulate the system behavior at various operating points and system parameters. This method has the disadvantage of being computationally intensive and provides little insight into the operation of the system.

On the other hand, an averaged time-continuous model of the UPS system can be obtained for (1) by assuming that the inverter switching frequency, f_s, is much higher than the frequency of the modulating signal, $v_m(t)$. Consequently, the discontinuous switching function S_1^* can be replaced by its time-dependent duty cycle $d_1(t)$ [9], as

$$d_1(t) = \frac{1}{2}\left(\frac{v_m(t)}{V_t} + 1\right) \tag{2}$$

where V_t is the amplitude of the carrier waveform.

For a modulating signal given by

$$v_m(t) = V_m \sin(\omega_m t) \tag{3}$$

the system state-space averaged continuous equation can be obtained by substituting the discontinuous switching function, S_1^*, in (1) by its average value in (2) and (3). The resultant system equation is obtained as

$$\frac{d}{dt}\begin{bmatrix} i_i(t) \\ i_l(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & 0 & \frac{-1}{L_f} \\ 0 & \frac{R_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & \frac{-1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i(t) \\ i_l(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} \frac{MV_{dc}\sin(\omega_m t)}{L_f} \\ 0 \\ 0 \end{bmatrix} \tag{4}$$

where M is the modulation index, defined as

$$M = \frac{V_m}{V_t}. \tag{5}$$

The first row of (4) indicates that the averaging process replaces the effect of the inverter switching function with a controllable sinusoidal voltage source of magnitude $M\ V_{dc}$. It should be noted that (4) is valid only through the linear range of operation, i.e., $M \leq 1.0$.

Assuming that the resistance associated with the filter inductor is negligibly small, the equivalent circuit of the averaged UPS system is as shown in Fig. 2.

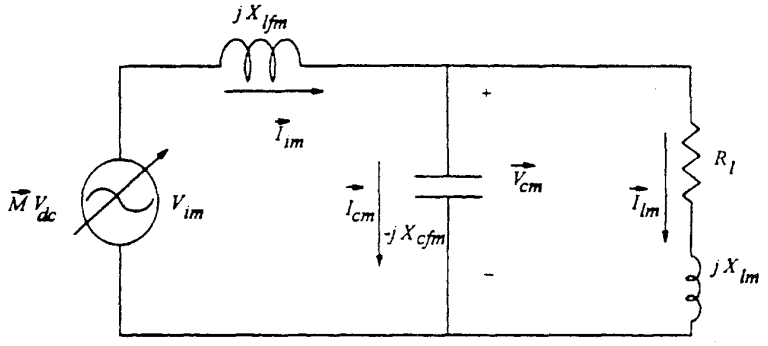


Fig. 2. Equivalent circuit of the averaged UPS system.

The system steady-state variables are obtained from Fig 2. using the following phasor analysis

$$\vec{I}_{im} = \frac{V_{dc}\vec{M}}{\vec{Z}_{im}} \tag{6}$$

$$\vec{V}_{cm} = V_{dc}\vec{K}\vec{M} \tag{7}$$

$$\vec{I}_{cm} = \frac{\vec{V}_c}{-j\,X_{cfm}} \tag{8}$$

and

$$\vec{I}_{lm} = \frac{\vec{V}_c}{\vec{Z}_{lm}} \tag{9}$$

where $\vec{M}$ is the phasor representation of the modulating signal $M\sin(\omega_m t)$ and$\vec{I}_{im}, \vec{V}_{cm}, \vec{I}_{cm}, \vec{I}_{lm}$ are the steady-state variables of the inverter output current, capacitor voltage and current, and load current at the modulating signal frequency, ω_m, respectively

$$\vec{Z}_{im} = \frac{X_{lm}X_{cfm} + X_{lfm}(X_{cfm} - X_{lm}) + jR_l(X_{lfm} - X_{cfm})}{R_l + j(X_{lm} - X_{cfm})} \tag{10}$$

$$\vec{K} = \frac{X_{lm} - X_{cfm} - jR_lX_{cfm}}{X_{lm}X_{cfm} + X_{lfm}(X_{cfm} - X_{lm}) + j(R_lX_{lfm} - R_lX_{cfm})}. \tag{11}$$

Equations (6)–(9) give the system steady-state variables in terms of the load parameters and filter components and represent the steady-state quiescent operating point of the system.

III. Stability Analysis of the UPS System

In order to ensure that the UPS system will produce the nominal load voltage, irrespective of disturbances such as variations in the input supply voltage, perturbations in the switching times, and the load, a real-time feedback control scheme is proposed. However, to successfully implement the real-time feedback control scheme, the power circuit incremental dynamics are examined with a view to selecting the appropriate feedback variables. It is assumed that the incremental variation in the control signal is much slower than the bandwidth of the control loop. Hence, a quasistatic approach is used to carry out the investigation [10], [11]

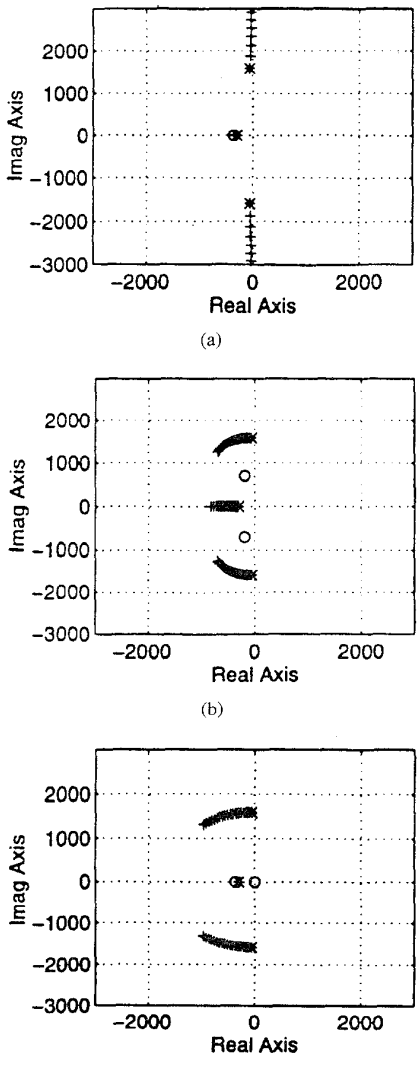


Fig. 3. Locus of the roots of the power circuit incremental dynamics for a load impedance of 10 Ω at 0.7 power factor lagging loads, $L_f = 5.0$ mH, $C_f = 100$ μF, and $V_{dc} = 100.0$ V.

The system equation given by (4), though time continuous, is nonlinear. The nonlinearity arises from the terms $(r_l(t)/l_l(t))i_l(t), (v_c(t)/l_l(t))$, and $m(t)v_{dc}(t)$. In order to develop a dynamic model of the UPS system, the system equations are first linearized around a nominal steady-state operating point. This is carried out using perturbation technique and small-signal approximation. The resulting small-signal dynamic model can be written as

$$\frac{\begin{bmatrix}\tilde{i}_i\\ \tilde{v}_c\\ \tilde{i}_c\end{bmatrix}}{\tilde{m}} = \frac{\dfrac{V_{dc}}{L_f}\begin{bmatrix}\left(s^2+\dfrac{R_l}{L_l}s+\dfrac{1}{L_lC_f}\right)\\ \dfrac{1}{C_f}\left(s+\dfrac{R_l}{L_l}\right)\\ s\left(s+\dfrac{R_l}{L_l}\right)\end{bmatrix}}{s^3+\dfrac{R_l}{L_l}s^2+\dfrac{1}{C_f}\left(\dfrac{1}{L_l}+\dfrac{1}{L_f}\right)s+\dfrac{R_l}{L_fL_lC_f}} \tag{12}$$

where $\tilde{i}_i, \tilde{v}_c, \tilde{i}_c$ indicate incremental changes in the inverter output current, capacitor voltage, and current, respectively, as a result of incremental changes in the duty cycle, $\tilde{d}$ and hence the modulation index, $\tilde{m}$ [see (2)]. Equation (12) shows that the location of the system poles is dependent on the input dc voltage (V_{dc}), the system parameters (L_l, R_l, L_f and C_f), and the incremental change in the modulation index, $\tilde{m}$ or implicitly, the duty cycle, $\tilde{d}$.

Fig. 3(a) shows the locus of the roots of the incremental dependence of the capacitor voltage due to 10% incremental change in the modulation index $\tilde{m}$. The figure shows that employing the capacitor voltage as the feedback variable makes the system dominant poles move along the imaginary axis of the s-plane. The figure also shows that the location of the system poles are not only dependent on the system parameters, but they are also time varying. For the circuit parameters given in Fig. 3, it can be seen that the frequency of the dominant poles can be as high as 4530 rad/s. This has the effect of producing high-frequency oscillations in the load voltage. Such behavior is not acceptable for UPS applications. As a result, the capacitor voltage cannot be employed as the feedback variable for the closed-loop operation of the UPS system.

Fig. 3(b) shows that closing the loop around the inverter output current makes the system poles move farther into the left half of the s-plane, resulting in stable closed-loop operation of the UPS system. However, in order to generate the reference waveform for the feedback control of the inverter output current, the instantaneous value of the load current must be known. This will require an additional current sensor. From the point of view of cost, this control scheme is not attractive.

Fig. 3(c) shows the locus of the roots of the incremental dependence of the capacitor current due to incremental changes in the modulation index. The figure shows that closing the loop around the capacitor current results in moving the system poles farther into the left half of the s-plane. This has the effect of providing active damping to any oscillation that may take place in the power circuit. Consequently, a stable operation of the closed-loop control scheme is achieved. Therefore, the capacitor current is chosen as the feedback variable for the closed-loop operation of the UPS system.

Although choosing the capacitor current as the feedback variable results in a stable operation of the closed loop UPS system and ensures sinusoidal capacitor current, it does not guarantee sinusoidal capacitor (load) voltage, especially when the inverter output voltage is nonsinusoidal (i.e., PWM). Therefore, in order to achieve sinusoidal capacitor voltage and current, an outer capacitor voltage feedback loop is also used.

IV. The Proposed UPS Control System

The resultant configuration of the proposed control scheme offers many advantages for UPS system applications. The inner current loop provides an inherent peak current limit in the power circuit, especially during "cold" start of the system. In addition, since the capacitor current represents the rate of change of the load voltage, the control scheme is capable of predicting and correcting near-future variations in the load voltage and thus providing a fast dynamic response. Furthermore, the outer voltage loop regulates the load voltage and produces a stiff ac voltage supply as well as ensures a sinusoidal load voltage within the acceptable total harmonic distortion (THD).

Fig. 4 shows the UPS system with an inner current loop and an outer voltage loop. The error signal $e(t)$ is obtained from successive comparison of the capacitor voltage and current with their respective reference signals. The inverter switching pattern is then obtained from a comparison of $e(t)$ and a fixed high-frequency (4.0 kHz) triangular waveform. The resultant switching pattern, which has a fixed switching frequency with variable duty cycle, produces a sinusoidal load voltage with low harmonic content.

V. Analysis and Design of the Feedback Control Scheme

In order to achieve a UPS system with fast dynamic response and small steady-state error between the load voltage and its reference waveform, both regulators of the feedback loop have to be carefully designed. The open-loop transfer function of the inner current loop, $G_{ic}(s)$, is obtained from the third row of (12) as

$$G_{ic}(s) = \frac{\tilde{i}_c}{\tilde{m}} = \frac{V_{dc}}{L_f}\frac{s\left(s+\dfrac{R_l}{L_l}\right)}{s^3+\dfrac{R_l}{L_l}s^2+\dfrac{1}{C}\left(\dfrac{1}{L_l}+\dfrac{1}{L_f}\right)s+\dfrac{R_l}{L_fL_lC}}. \tag{13}$$

Fig. 5 shows the Bode plot of the inner current loop for various load conditions. The figure shows that the inner current loop exhibits a band-pass filter-like characteristics. The figure also shows that the bandwidth of the inner current loop is not affected by the load variations. It can be seen from the figure that the loop possesses a phase margin of 270° and 90° and a theoretical gain margin of infinity.

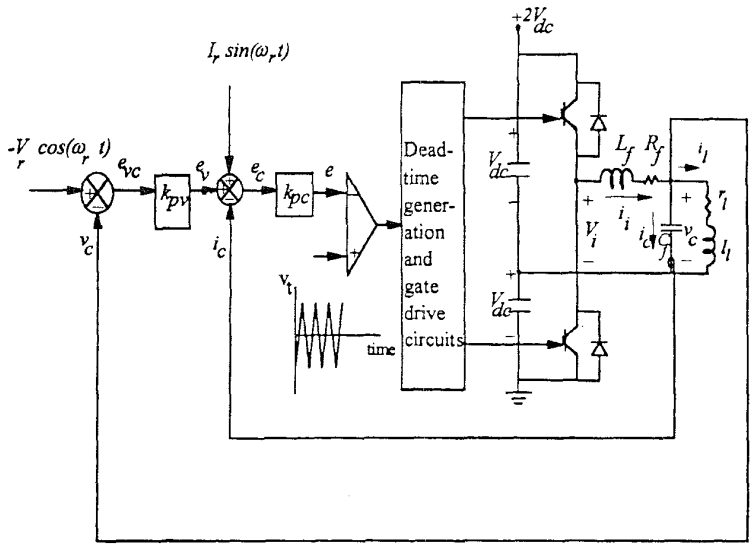


Fig. 4. The proposed control scheme of the single-phase UPS inverter.

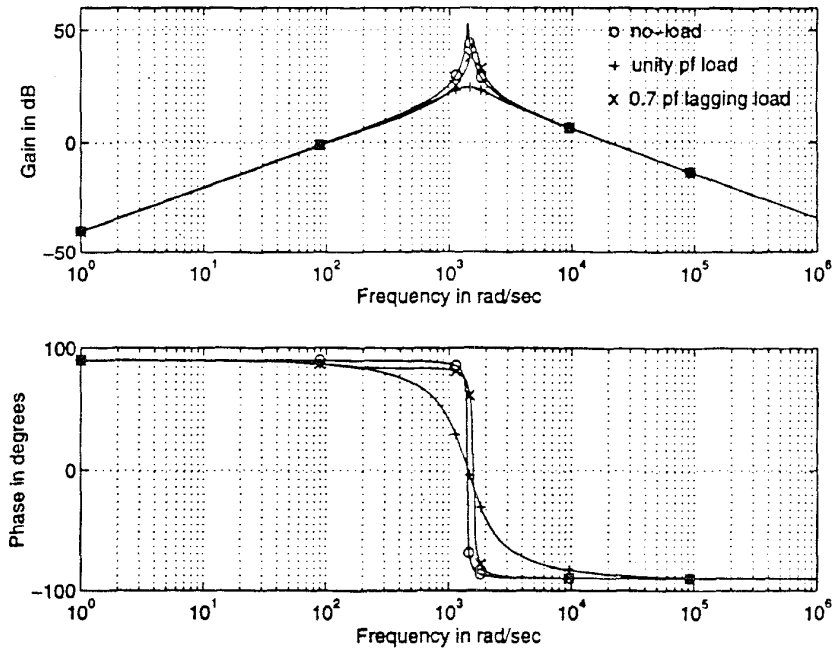


Fig. 5. Bode diagram of the open-loop transfer function of the inner current loop of the UPS system: $L_f = 5.0$ mH, $C_f = 100.0$ μF, and $Z_l = 8.8$ $\Omega, V_{dc} = 100.0$ V.

The closed-loop transfer function of the inner current loop for unity and 0.7 power factor lagging loads is shown in Fig. 6.

The figure shows that the loop possesses a relatively narrow bandwidth with a significant phase error in both cases. The loop bandwidth can be widened by employing proportional controller (k_{pc}) in the feed-forward path of the inner current loop. However, to avoid excessive gain in the inner current loop and produce a system that is immune to switching noise, k_{pc} is chosen such that the gain of the closed-loop transfer function of the inner current loop exhibits near-unity gain from $\omega \cong 200$ rad/s up to half the inverter switching frequency (i.e., $\omega \cong 12\,500$ rad/s). And, since the bandwidth of the inner current loop is slightly wider for 0.7 power factor lagging loads (see Fig. 6), the choice of k_{pc} is carried out for this condition (i.e., worst-case scenario). It can be shown that for $k_{pc} = 2.0$, the gain of the closed-loop transfer function is 0.94 at $\omega = 12\,500$ rad/s. The Bode diagram of the closed-loop transfer function of the inner current loop with $k_{pc} = 2.0$ is shown in Fig. 7. The figure also shows that the loop

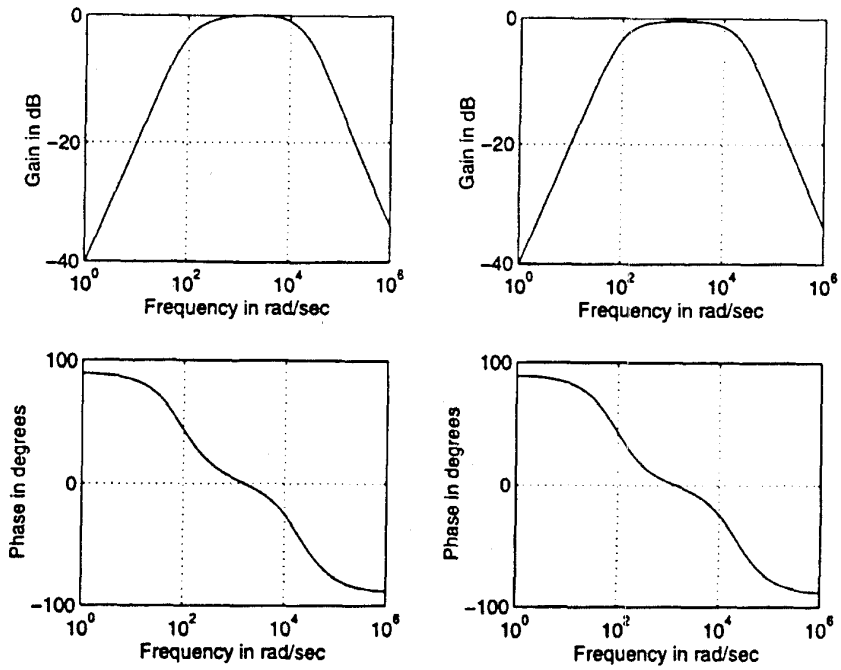


Fig. 6. Bode diagram of the closed-loop transfer function of the inner current loop of the UPS system ($k_{pc} = 1.0$): $L_f = 5.0$ mH, $C_f = 100.0$ μF, and $Z_l = 8.8$ Ω, $V_{dc} = 100.0$ V.

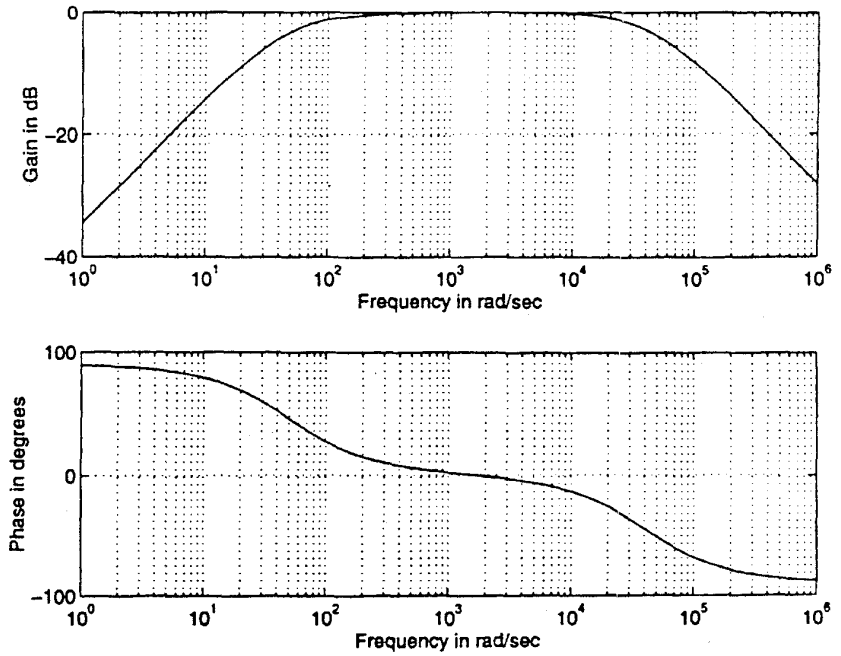


Fig. 7. Bode diagram of the closed-loop transfer function of the inner current loop of the UPS system with $k_{pc} = 2.0$, $L_f = 5.0$ mH, $C_f = 100.0$ μF, and $Z_l = 8.8$ Ω at 0.7 power factor lagging, $V_{dc} = 100.0$ V.

bandwidth has been increased and the error in the phase over the frequency range of interest ($\omega \cong 200$ to 12 500 rad/s) has been reduced.

The small-signal open-loop transfer function of the outer-voltage feedback loop is obtained in terms of the open-loop transfer function of the inner current loop as

$$G_{vc}(s) = \frac{1}{sC_f} \frac{k_{pc}G_{ic}(s)}{1 + k_{pc}G_{ic}(s)} \tag{14}$$

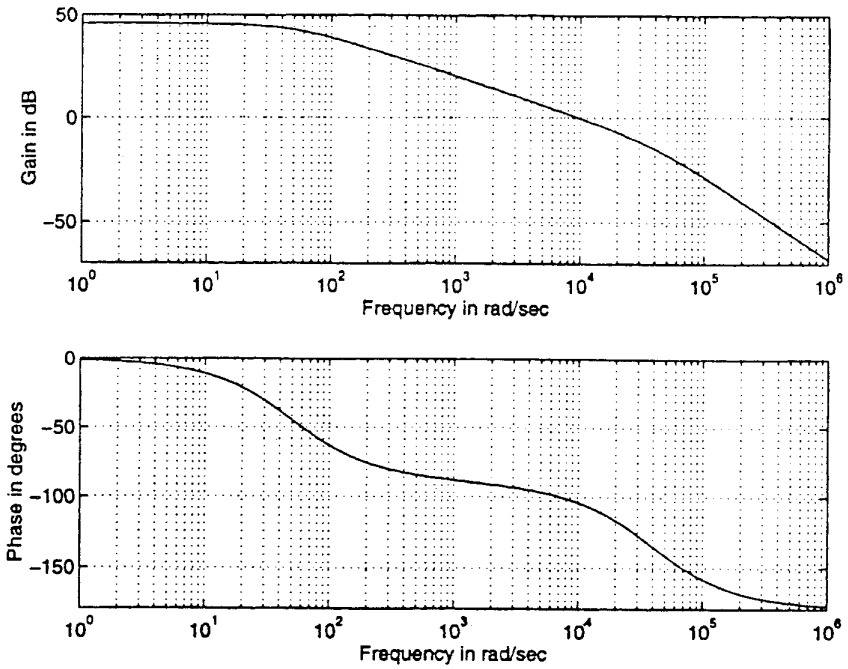


Fig. 8. Bode diagram of the open-loop transfer function of the outer-voltage loop of the UPS system with $k_{pc} = 2.0, L_f = 5.0$ mH, $C_f = 100.0$ μF, and $Z_l = 8.8\ \Omega, V_{dc} = 100.0$ V.

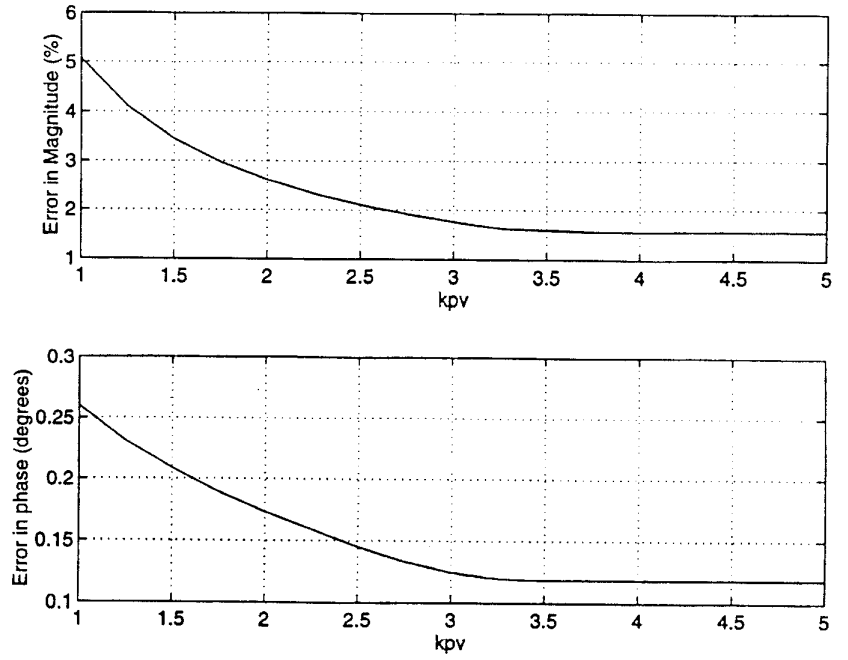


Fig. 9. Error in the magnitude and phase of the capacitor voltage with respect to its reference waveform with $k_{pc} = 2.0, L_f = 5.0$ mH, $C_f = 100.0$ μF, and $Z_l = 8.8\ \Omega, V_{dc} = 100.0$ V.

where $G_{ic}(s)$ is given by (13). The Bode plot of $G_{vc}(s)$ is shown in Fig 8. The figure shows that the loop has a phase margin of 74.5° and a gain margin of 87.1 dB.

In order to reduce the steady-state error between the capacitor voltage and its reference waveform, a proportional-plus-integral (PI) controller may be used in the feed-forward path of the outer capacitor voltage feedback loop. However, since the capacitor voltage is sinusoidally varying, a PI controller will introduce phase errors and deteriorate the effectiveness of the control scheme. Consequently, a proportional controller, k_{pv}, is employed in the outer voltage loop. It can be seen from Fig. 8 that using a proportional controller of high gain

TABLE I
THD OF THE LOAD VOLTAGE AS THE LOAD AND FILTER PARAMETERS CHANGE

	Z_l=10.0 Ω (1.0 pu) at lagging power factor of			0.7 power factor lagging load with Z_l		
	0.6	0.8	1.0	4.0 pu	2.0 pu	1.33 pu
X_{lfm}=0.18 pu X_{cfm}=2.50 pu THD %	0.44	0.41	0.40	0.40	0.42	0.41
X_{lfm}=0.1 pu X_{cfm}=3.0 pu THD %	4.71	3.52	2.19	3.62	3.46	3.28
X_{lfm}=0.1 pu X_{cfm}=5.0 pu THD %	11.16	12.23	5.14	12.32	10.71	11.93

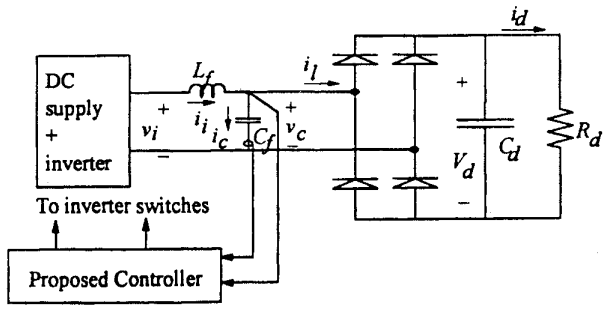


Fig. 10. The proposed UPS with a bridge rectifier as the nonlinear load (C_d = 2500 μF, R_d = 20.0 Ω).

value shifts the system cross-over frequency to a higher value, thus reducing the available gain and phase margin of the outer voltage loop. Hence, the value of k_{pv} is chosen such that the steady-state error between the capacitor voltage and its reference waveform is within an acceptable value (chosen to be less than 2%).

Fig. 9 shows the effect of k_{pv} on the steady-state error between the capacitor voltage and its reference waveform for the closed-loop operation of the UPS system (shown in Fig. 4). The figure shows that the error decreases with increasing values of k_{pv}, and for $k_{pv} \geq 2.75$, the error is less than 2.0%. Thus, k_{pv} is chosen as 2.75.

The performance of the proposed UPS system was investigated by simulating its behavior at various loading conditions. The input capacitor voltage of 100 V is chosen as 1.0 pu, while the load impedance of magnitude 10 Ω is chosen the base value for impedances.

Table I shows the effect of changing the magnitude and phase angle of the load on the THD of the load voltage for various values of filter series inductive reactance, X_{lfm}, and filter shunt capacitive reactance, X_{cfm}. The table shows that for X_{lfm} = 0.18 pu and X_{cfm} = 2.5 the THD of the load voltage is very small. Also, it can be shown that the filter rating/cost for these values is minimum.

The performance of the proposed control scheme under nonlinear load conditions was also investigated. The nonlinear load was chosen as a bridge rectifier with an output dc filter, C_d, and a resistive load as shown in Fig. 10.

TABLE II
THD OF THE FILTER CAPACITOR VOLTAGE WITH A BRIDGE RECTIFIER AS THE NONLINEAR LOAD (V_{dc} = 100.0 V, X_{lfm} = 0.15 pu)

	R_d in pu			
	1.0	2.0	3.0	4.0
X_{cfm}=0.88 pu THD %	5.22	3.48	2.78	2.22
X_{cfm}=0.66 pu THD %	4.62	2.99	2.41	1.96
X_{cfm}=0.53 pu THD %	4.07	2.53	2.01	1.76

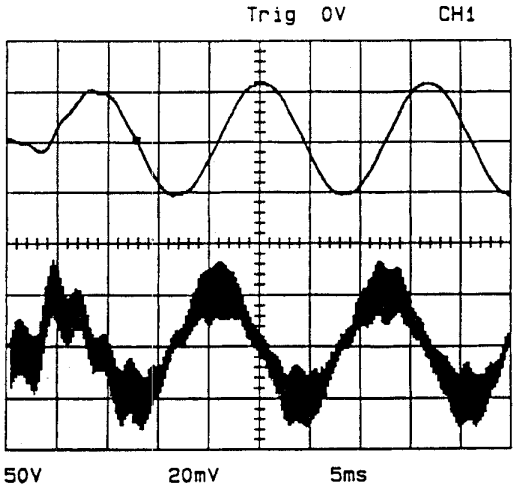


Fig. 11. Experimental results of the transient response of the proposed UPS system.

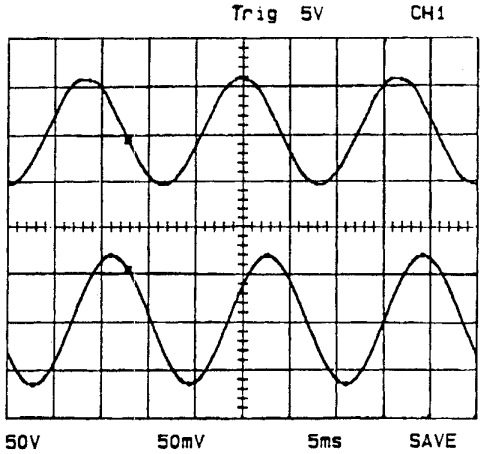
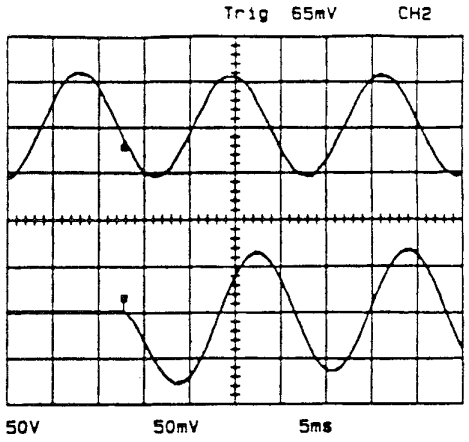
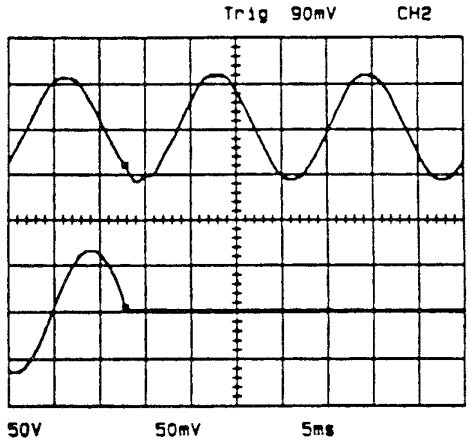


Fig. 12. Experimental results of the steady-state response of the proposed UPS system.

Table II shows the effect of varying the load resistance on the THD of the load voltage for various values of X_{cfm}. The table shows that with larger filter capacitor a load voltage within the acceptable THD can be obtained at adverse loading conditions.



(a)



(b)

Fig. 13. Experimental results of the dynamic response of the proposed UPS system for a 100% step change in the load: (a) 100% application of the load and (b) 100% removal of the load.

VI. Experimental Results

A prototype experimental module of the proposed UPS (Fig. 4) was built to verify the operation of the control strategy. Both the actual capacitor voltage and current in the power circuit were sensed, filtered, and used as the control variables.

Fig. 11 shows the transient response from "cold" start to full load of the proposed UPS system. The upper trace shows the capacitor voltage and the lower trace shows the capacitor current. The capacitor current was recorded by observing the voltage drop across a current shunt of 10.0 mΩ resistance. The figure shows that the system takes about a quarter cycle to reach the steady-state values of the capacitor voltage and current. The steady-state load voltage and current waveforms of the UPS system are depicted in Fig. 12. The figure shows that the control strategy is capable of producing a nearly perfect sinusoidal load voltage at moderate switching frequency. The total harmonic distortion of the capacitor (load) voltage was measured as 2%.

Fig. 13 shows the dynamic response of the UPS system for 100% step change in the load from no load to full load.

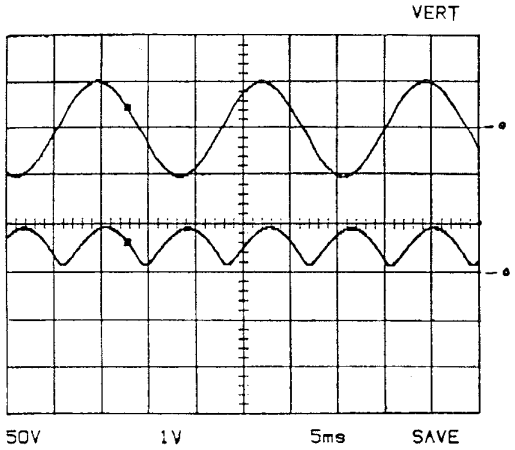


Fig. 14. Experimental results of the proposed UPS system feeding a full-bridge rectifier with an R-L load.

The figure shows that the system exhibits very fast dynamic response with excellent load voltage regulation from no-load to full-load and with very little change in the load voltage at the point of applying the full load, indicating that the control scheme ensures a "stiff" load voltage.

The system performance with nonlinear loads is shown in Fig. 14. The nonlinear load was chosen as a full-bridge rectifier feeding an R-L load ($R = 20.0\ \Omega$ and $L = 16.0$ mH). The load current was recorded by observing the voltage drop across the load resistance using $\frac{1}{50}$ attenuation oscilloscope probe.

Figs. 12–14 show that the proposed control scheme is capable of supplying both linear and nonlinear loads with excellent voltage regulation and minimum distortion in the load voltage.

VII. Conclusion

A multiple feedback loop control strategy for a single-phase voltage-source UPS system has been described in the paper. The system performance under open-loop control strategy was first studied to obtain the steady state performance of the UPS system. The power circuit incremental dynamics was then investigated to assess the system stability and select appropriate feedback variables for the closed-loop control of the system. The stability analysis showed that a feedback control system with an inner capacitor current control loop and an outer capacitor voltage feedback loop results in a successful operation of the UPS system. The proposed control strategy offers many features that are attractive for UPS applications. In addition to the basic features of most feedback control systems, such as insensitivity to parameter variations and robustness, the scheme is capable of producing nearly perfect sinusoidal load voltage at any load power factor with excellent load voltage regulation. The scheme also possesses very fast dynamic response and lends itself to both linear and nonlinear load applications.

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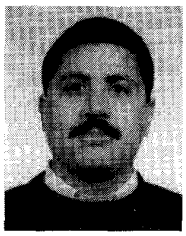

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