



SoC Design and Practice

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Lab 7: Coverage



Recap

- Verification
 - Directed vs. constrained random
 - Coverage-oriented
- Coverage
 - Code coverage
 - Functional coverage





Outline

- Code coverage measurement
- Functional coverage measurement





Code Coverage

Code Coverage in Verdi

Verdi:vdCoverage.1> <vdb: VDB.vdb>@taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Name	Score	Line	Toggle	FSM	Condition	Branch
DMAC_TOP_TB	79.60%	85.40%	66.39%	60.87%	100.00%	
apb_if	73.84%	91.30%	56.37%			
ar_ch	55.21%		55.21%			
aw_ch	60.42%		60.42%			
b_ch	22.22%		22.22%			
r_ch	85.71%		85.71%			
u_DUT	83.43%	91.59%	67.60%	66.67%	100.00%	
u_cfg	82.96%	94.74%	61.29%			
u_engine	84.17%	90.91%	72.67%	66.67%	100.00%	
u_fifo	85.16%	74.19%	99.47%			
u_mem	69.66%	84.26%	63.14%	57.14%		
w_ch	79.55%		79.55%			

CovSrc1: DMAC_TOP_TB.u_DUT.u_engine.u_fifo

Uncovered

e/ScalableArchLab

./RTL/DMAC_FIFO.sv

```

44 wrptr      <= wrptr_n;
45 rdptr      <= rdptr_n;
46
47 if (wren_i) begin
48   data[wrptr[DEPTH_LG2-1:0]] <= wdata_i;
49 end
50
51
52 always_comb begin
53   wrptr_n      = wrptr;
54   rdptr_n      = rdptr;
55
56   if (wren_i) begin
57     wrptr_n      = wrptr + 'd1;
58   end
59
60   if (rden_i) begin
61     rdptr_n      = rdptr + 'd1;
62   end
63
64   empty_n      = (wrptr_n == rdptr_n);
65   full_n       = (wrptr_n[DEPTH_LG2] != rdptr_n[DEPTH_LG2]);
66   &(wrptr_n[DEPTH_LG2-1:0] == rdptr_n[DEPTH_LG2-1:0]);
67 end
68
69 // synthesis translate off
70 always @(posedge clk) begin
71   if (full_o & wren_i) begin
72     $display("FIFO overflow");
73     @(posedge clk);
74     $finish;
75   end
76 end
77
78 always @(posedge clk) begin
79   if (empty_o & rden_i) begin
80

```

CovDetail

Line	Toggle	FSM	Condition	Branch	Assert
Category					
Block					75.00%
Statement					74.19%

Status Name Line No. Source

CovSrc1 Hvp

CovDetail HvpDetail



Login and git update



- `$ git clone https://github.com/2025-Spring-SoC/lab5.git`
- `$ cd lab5/DMAC`

Simulator Options for Code Coverage

- VCS (Synopsys simulator)
 - vcs -cm line+cond+fsm+tgl+branch ...
 - Included in run.compile4cov and run.sim4cov
 - You can simply run run.compile4cov and run.sim4cov
- NCVerilog (Cadence simulator)
 - Ncverilog -coverage <coverage_types> ...
 - Coverage type
 - B (Block)
 - E (Expression)
 - F (FSM)
 - T (Toggle)
 - U (Functional)
 - A(All)

After Compilation and Simulation

- We have a new directory containing coverage database
 - (default) simv.vdb
 - (in our environment) **VDB.vdb**
- Reading the coverage database
 - 1) Create a HTML-based report using Synopsys urg

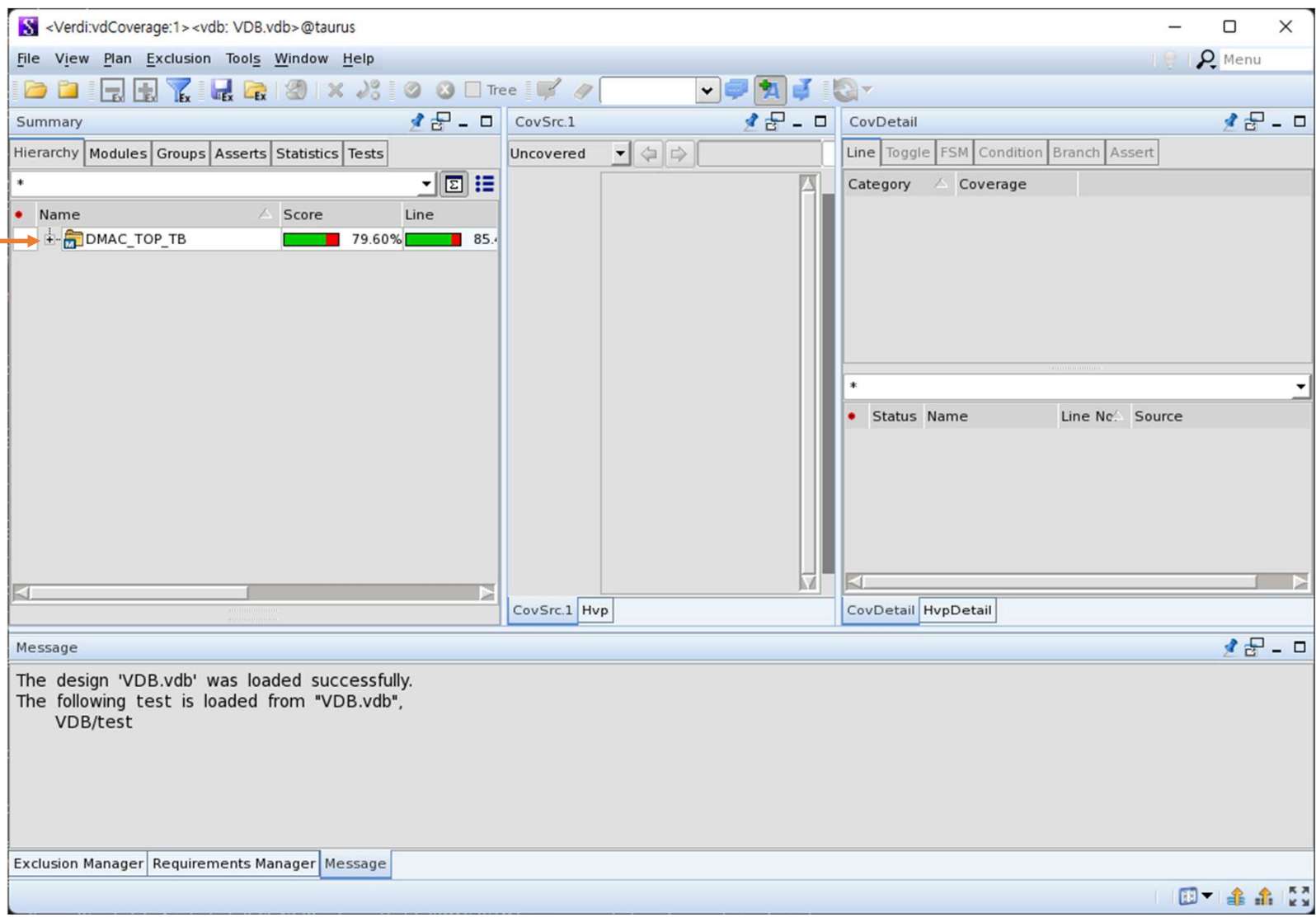
```
$ urg -dir VDB.vdb
```
 - 2) Launch Verdi

```
$ verdi -cov -covdir VDB.vdb
```

Or simply type **./run.verdi4cov**

Code Coverage in Verdi

Click + to expand



The screenshot displays the Verdi IDE interface for code coverage analysis. The main window is titled "<Verdi:vdCoverage:1> <vdb: VDB.vdb>@taurus". The interface is divided into several panes:

- Summary Pane:** Contains a hierarchy tree on the left. The tree shows a folder icon next to "DMAC_TOP_TB" with a score of 79.60% and a line count of 85. An orange arrow points to the "+" icon next to the folder name, indicating it can be expanded.
- CovSrc.1 Pane:** Shows the source code with a "Uncovered" section highlighted.
- CovDetail Pane:** Displays detailed coverage information for the selected source code. It includes tabs for "Line", "Toggle", "FSM", "Condition", "Branch", and "Assert". The "Line" tab is selected, showing a table with columns: Status, Name, Line No., and Source.
- Message Pane:** Located at the bottom, it contains a message: "The design 'VDB.vdb' was loaded successfully. The following test is loaded from 'VDB.vdb', VDB/test".

The bottom of the window features a tabbed interface with "Exclusion Manager", "Requirements Manager", and "Message" tabs. The "Message" tab is currently active.

Code Coverage in DMAC_FIFO

<Verdi:vdCoverage:1> <vdb: VDB.vdb> @taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Name	Score	Line
DMAC_TOP_TB	79.60%	85
apb_if	73.84%	91
ar_ch	55.21%	
aw_ch	60.42%	
b_ch	22.22%	
r_ch	85.71%	
u_DUT	83.43%	91
u_cfg	82.96%	94
u_engine	84.17%	90
u_fifo	85.16%	74
u_mem	69.66%	84

CovSrc.1: DMAC_TOP_TB.u_DUT.u_engine.u_fifo

Uncovered

```

73      $display("FIFO overflow");
74      @(posedge clk);
75      $finish;
76
77      end
78
79      always @(posedge clk) begin
80          if (empty_o & rden_i) begin
81              $display("FIFO underflow");
82              @(posedge clk);
83              $finish;
84          end
85      end
86      // synthesis translate_on
87
88      assign full_o
  
```

CovDetail

Line	Toggle	FSM	Condition	Branch	Assert
Category Coverage					
Block					75.00%
Statement					74.19%

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

Excluding Codes from Calculation

<Verdi:vdCoverage:1> <vdb: VDB.vdb>@taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Name	Score	Line
DMAC_TOP_TB	79.60%	85
apb_if	73.84%	91
ar_ch	55.21%	
aw_ch	60.42%	
b_ch	22.22%	
r_ch	85.71%	
u_DUT	83.43%	91
u_cfg	82.96%	94
u_engine	84.17%	90
u_fifo	85.16%	74
u_mem	69.66%	84

CovSrc:1: DMAC_TOP_TB.u_DUT.u_engine.u_fifo

Uncovered

```

73      $display("FIFO overflow");
74      @(posedge clk);
75      $finish;
76
77      end
78
79      always @(posedge clk) begin
80          if (empty_o & rden_i) begin
81              $display("FIFO underflow");
82              @(posedge clk);
83              $finish;
84          end
85      end
86      // synthesis trap
87
88      assign full_o
  
```

CovDetail

Category	Coverage
Block	75.00%
Statement	74.19%

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

Context Menu:

- Show/Hide Search Widget Ctrl+S
- Show Associated Tests
- Copy Ctrl+C
- Paste Ctrl+V
- Expand All
- Collapse All
- Accept Shift+A
- Reject Shift+R
- Exclude Shift+E**
- Unexclude Shift+U
- Add Exclude Annotation Shift+T
- Delete Exclude Annotation Shift+K
- Sync File and Line to Verdi Debug Ctrl+Shift+C

Recalculate after Exclusion

<Verdi:vdCoverage:1><vdb: VDB.vdb>@taurus

File View Plan Exclusion Tools Window Help

Summary Hierarchy Module

Recalculate Alt+Shift+R
Clear Marks Shift+C
Clear Exclusions
Exclude Shift+E
Unexclude Shift+U
Add Exclude Annotation Shift+T
Delete Exclude Annotation Shift+K
Load Exclusions from File...
Load Exclusions from File List...
Copy Exclusions...
Promote Exclusions to Module...
Save Exclusions for Selected Objects...
Save Exclusions for Selected Trees...
Accept All
Reject All
Clear Reviews

Src:1: DMAC_TOP_TB.u_DUT.u_engine.u_fifo

73-75

```

67
68     end
69
70     // synthesis translate off
71     always @(posedge clk) begin
72         if (full_o & wren_i) begin
73             $display("FIFO overflow");
74             @(posedge clk);
75             $finish;
76         end
77     end
78
79     always @(posedge clk) begin
80         if (empty_o & rden_i) begin
81             $display("FIFO underflow");
82             @(posedge clk);
83             $finish;

```

CovDetail

Line	Toggle	FSM	Condition	Branch	Assert
Category Coverage					
Block					75.00%
Statement					74.19%

* Status Name Line No Source

CovDetail HvpDetail

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from 'VDB.vdb',
VDB/test

Exclusion Manager Requirements Manager Message

Toggle Coverage

<Verdi:vdCoverage:1><vdb: VDB.vdb>@taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Name	Score	Line
DMAC_TOP_TB	79.94%	87
apb_if	73.84%	91
ar_ch	55.21%	
aw_ch	60.42%	
b_ch	22.22%	
r_ch	85.71%	
u_DUT	84.91%	98
u_cfg	82.96%	94
u_engine	85.99%	100
u_fifo	93.76%	100
u_mem	69.66%	84

CovSrc.1: DMAC_TOP_TB.u_DUT.u_engine

Uncovered

```

6 module DMAC_ENGINE
7 (
8   input wire clk,
9   input wire rst_n, // _n
10  means active low
11
12  // configuration registers
13  input wire [31:0] src_addr_i,
14  input wire [31:0] dst_addr_i,
15  input wire [15:0] byte_len_i,
16  input wire start_i,
17  output wire done_o,
18
19  // AMBA AXI interface (AW channel)
20  output wire [3:0] awid_o,
21  output wire [31:0] awaddr_o,
22  output wire [3:0] awlen_o,

```

CovDetail

Variable	Type	Coverage	Disp
rst_i	port	100.00%	
ready	signal	100.00%	
ready_o	port	100.00%	
resp_i[1:0]	port	0.00%	
rst_n	port	50.00%	

Variable

Variable	0->1	1->0
rst_n	✓	✗

In the simulations, reset had only 0->1 transitions.

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

FSM Coverage

<Verdi:vdCoverage:1> <vdb: VDB.vdb> @taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Stat

Name Score

- DMAC_TOP_TB
 - apb_if
 - ar_ch
 - aw_ch
 - b_ch
 - r_ch
 - u_DUT
 - u_cfg
 - u_engine
 - u_fifo
 - u_mem

CovSrc:1: DMAC_TOP_TB.u_DUT.u_engine

Uncovered

```

56   output wire          rready_o
57   );
58
59   // mnemonics for state values
60   localparam
61       S_IDLE   = 3'd0,
62       S_RREQ   = 3'd1,
63       S_RDATA  = 3'd2,
64       S_WREQ   = 3'd3,
65       S_WDATA  = 3'd4;
66   reg [2:0] state, state_n;
67   reg [31:0] src_addr, src_addr_n;
68   reg [31:0] dst_addr, dst_addr_n;
69   reg [15:0] cnt, cnt_n;
70   reg [3:0] went, went_n;
71
72

```

CovDetail

Line Toggle FSM Condition Branch Assert

FSM	Transition	State	Seque
state	66.67%	100.00%	

Show as List Mode: States & Transitions

	0	1	2	3	4
0 S_IDLE	-	-	✓	-	-
1 S_RDATA	✗	-	-	-	✓
2 S_RREQ	✗	✓	-	-	-
3 S_WDATA	✓	-	✓	-	-
4 S_WREQ	✗	-	-	✓	-

From

To

Have not covered reset during operation (e.g., S_RDATA -> S_IDLE)

Note: the numbers here is different from the numbers defined in the local param

The design 'VDB.vdb' was loaded successfully
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

Condition Coverage

<Verdi.vdCoverage:1> <vdb: VDB.vdb>@taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Stat

Name Score

- DMAC_TOP_TB
 - apb_if
 - ar_ch
 - aw_ch
 - b_ch
 - r_ch
 - u_DUT
 - u_cfg
 - u_engine
 - u_fifo
 - u_mem

CovSrc:1: DMAC_TOP_TB.u_DUT.u_engine

Uncovered

```

213 assign awid_o           = 4'd0;
214 assign awaddr_o         = dst_addr;
215 assign awlen_o           = (cnt >= 'd64) ? 4'hF: cnt
    [5:2]-4'h1;
216 assign awsize_o         = 3'b010; // 4 bytes per
    transfer
217 assign awburst_o        = 2'b01; // incremental
218 assign awvalid_o         = awvalid;
219
220 assign wid_o             = 4'd0;
221 assign wdata_o           = fifo_rdata;
222 assign wstrb_o           = 4'b1111; // all bytes wi
    thin 4 byte are valid
223 assign wlast_o           = 1'b1;
224 assign wvalid_o          = wvalid;
225
226 assign breadv_o          = 1'b1;
  
```

CovDetail

Line Toggle FSM Condition Branch Assert

Expression	Coverage
((cnt >= 16'h0040) ? 4'hf : ((cnt[...	100.00%
((cnt >= 16'h0040) ? 4'hf : ((cnt[...	100.00%

((cnt >= 16'h0040) ? 4'hf : ((cnt[5:2] - 4'b1) > 1) ? 4'hf : 4'h0)

Coverage 1

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

Branch Coverage

<Verdi:vdCoverage:1> <vdb: VDB.vdb> @taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Stat

Name Score

- DMAC_TOP_TB
 - apb_if
 - ar_ch
 - aw_ch
 - b_ch
 - r_ch
 - u_DUT
 - u_cfg
 - u_engine
 - u_fifo
 - u_mem

CovSrc1: DMAC_TOP_TB.u_DUT.u_engine

Uncovered

```

182 state_n = S_IDLE;
183 end
184 else begin
185 state_n = S_RREQ;
186 end
187 end
188 else begin
189 wcnt_n = wcnt - 4'd1;
190 end
191 end
192 ==> MISSING_ELSE
193 end
194 ==> MISSING_DEFAULT
195 endcase
196 end
197 DMAC_FIFO u_fifo
  
```

CovDetail

Line Toggle FSM Condition Branch Assert

Name	Coverage	Line No.	-1-	-2-
Item0	100.00%	215		
Item1	100.00%	231		
Item2	100.00%	89		
Item3	93.33%	129		

Line No. Exp. Value

129	state	
132	(start_i & (byte_len_i ...	
143	aready_i	
151	rvalid_i	
153	ract_i	

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

Putting Them Together

<Verdi:vdCoverage:1> <vdb: VDB.vdb>@taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Name	Score	Line	Toggle	FSM	Condition	Branch
DMAC_TOP_TB	79.94%	87.10%	66.39%	60.87%	100.00%	85.33%
apb_if	73.84%	91.30%	56.37%			
ar_ch	55.21%		55.21%			
aw_ch	60.42%		60.42%			
b_ch	22.22%		22.22%			
r_ch	85.71%		85.71%			
u_DUT	84.91%	98.99%	67.60%	66.67%	100.00%	91.30%
u_cfg	82.96%	94.74%	61.29%			92.86%
u_engine	85.99%	100.00%	72.67%	66.67%	100.00%	90.62%
u_fifo	93.76%	100.00%	99.47%			81.82%
u_mem	69.66%	84.26%	63.14%	57.14%		74.07%
w_ch	79.55%		79.55%			

CovSrc...engine

Uncovered

```

182 state_n
    = S_
    IDLE;

183
184 end

else
begin
185

```

CovDetail

Name	Coverage	Line
Item0	100.00%	
Item1	100.00%	
Item2	100.00%	
Item3	93.33%	

Line No.	Exp.	Value
129	state	
132	(start_i & (byte_len_i ...	
143	arready_i	
151	rvalid_i	
153	rlast_i	
161	awready_i	

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

After Excluding TB and Assertions

<Verdi:vdCoverage:1> <vdb: VDB.vdb>@taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Name	Score	Line	Toggle	FSM
DMAC_TOP_TB	83.50%	87.55%	67.62%	66.67%
apb_if				
ar_ch				
aw_ch				
b_ch				
r_ch				
u_DUT	85.74%	98.99%	67.60%	66.67%
u_cfg	82.96%	94.74%	61.29%	
u_engine	87.20%	100.00%	72.67%	66.67%
u_fifo	99.82%	100.00%	99.47%	
u_mem				

CovSrc.1: DMAC_TOP_TB.u_DUT.u_cfg

Uncovered

```

49 // pwrite : _____
50 // paddr : DMA_CMD
51 // pwidth : 1
52 // start : _____

53
54 wire wren
55 = psel_i & penable_i & pwrite_i;
56
57 always @(posedge clk) begin
58     if (!rst_n) begin
59         src_addr
60         dst_addr

```

CovDetail

Line Toggle FSM Condition Branch

FSM Transition State

Show as List Mode: States & Transitions

CovDetail HvpDetail

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

Functional Coverage

Function Coverage Items

- You need to manually create

```

DMAC_TOP_TB.sv (~:/ECE4278_class/lab5/DMAC/SIM/TB) - GVIM@taurus
File Edit Tools Syntax Buffers Window Help
[Icons]
286 // Functional coverage
287 covergroup apb_cov;
288   DIR: coverpoint apb_if.pwrite {
289     bins READ      = {0};
290     bins WRITE     = {1};
291   }
292   ADDR: coverpoint apb_if.paddr {
293     bins DMA_VER    = {'h0};
294     ignore_bins RSVD1 = [{'h4: 'hFC}];
295     bins DMA_SRC    = {'h100};
296     bins DMA_DST    = {'h104};
297     bins DMA_LEN    = {'h108};
298     bins DMA_CMD    = {'h10c};
299     bins DMA_STATUS = {'h110};
300     ignore_bins RSVD2 = [{'h114: $}]; // to maximum value
301   }
302   WDATA: coverpoint apb_if.pwdata {
303     bins ZERO       = {'h0};
304     bins ONE        = {'h1};
305     bins OTHERS     = [{'h2: $}]; // to maximum value
306   }
307   WDATA2: coverpoint apb_if.pwdata[1:0] {
308     bins MOD4_ZERO  = {'h0};
309     bins MOD4_ONE   = {'h1};
310     bins MOD4_TWO   = {'h2};
311     bins MOD4_THREE = {'h3};
312   }
313   SFR_RW: cross ADDR, DIR {
314     bins DMA_VER_RD = binsof(ADDR.DMA_VER) && binsof(DIR.READ);
315     ignore_bins DMA_VER_WR = binsof(ADDR.DMA_VER) && binsof(DIR.WRITE);
316     bins DMA_SRC_RD = binsof(ADDR.DMA_SRC) && binsof(DIR.READ);
317     bins DMA_SRC_WR = binsof(ADDR.DMA_SRC) && binsof(DIR.WRITE);
318     bins DMA_DST_RD = binsof(ADDR.DMA_DST) && binsof(DIR.READ);
319     bins DMA_DST_WR = binsof(ADDR.DMA_DST) && binsof(DIR.WRITE);
320     bins DMA_LEN_RD = binsof(ADDR.DMA_LEN) && binsof(DIR.READ);
321     bins DMA_LEN_WR = binsof(ADDR.DMA_LEN) && binsof(DIR.WRITE);
322     ignore_bins DMA_CMD_RD = binsof(ADDR.DMA_CMD) && binsof(DIR.READ);
323     bins DMA_CMD_WR = binsof(ADDR.DMA_CMD) && binsof(DIR.WRITE);
324     bins DMA_STATUS_RD = binsof(ADDR.DMA_STATUS) && binsof(DIR.READ);
325     ignore_bins DMA_STATUS_WR = binsof(ADDR.DMA_STATUS) && binsof(DIR.WRITE);
326   }
327 endgroup
295, 1 95%

```

Covergroup

- SystemVerilog user-defined type
- Usually contains
 - When to sample
 - What to sample
 - A set of cover points
 - Cross coverage between cover points
- Other options

```

DMAC_TOP_TB.sv (~:/ECE4278_class/lab5/DMAC/SIM/TB) - GVIM@taurus
File Edit Tools Syntax Buffers Window Help
286 // Functional coverage
287 covergroup apb_cov;
288   DIR: coverpoint apb_if.pwrite {
289     bins READ      = {0};
290     bins WRITE     = {1};
291   }
292   ADDR: coverpoint apb_if.paddr {
293     bins DMA_VER    = {'h0};
294     ignore_bins RSVD1 = [{'h4: 'hFC}];
295     bins DMA_SRC    = {'h100};
296     bins DMA_DST    = {'h104};
297     bins DMA_LEN    = {'h108};
298     bins DMA_CMD    = {'h10c};
299     bins DMA_STATUS = {'h110};
300     ignore_bins RSVD2 = [{'h114: $}]; // to maximum value
301   }
302   WDATA: coverpoint apb_if.pwdata {
303     bins ZERO       = {'h0};
304     bins ONE        = {'h1};
305     bins OTHERS     = [{'h2: $}]; // to maximum value
306   }
307   WDATA2: coverpoint apb_if.pwdata[1:0] {
308     bins MOD4_ZERO  = {'h0};
309     bins MOD4_ONE   = {'h1};
310     bins MOD4_TWO   = {'h2};
311     bins MOD4_THREE = {'h3};
312   }
313   SFR_RW: cross ADDR, DIR {
314     bins DMA_VER_RD = binsof(ADDR.DMA_VER) && binsof(DIR.READ);
315     ignore_bins DMA_VER_WR = binsof(ADDR.DMA_VER) && binsof(DIR.WRITE);
316     bins DMA_SRC_RD = binsof(ADDR.DMA_SRC) && binsof(DIR.READ);
317     bins DMA_SRC_WR = binsof(ADDR.DMA_SRC) && binsof(DIR.WRITE);
318     bins DMA_DST_RD = binsof(ADDR.DMA_DST) && binsof(DIR.READ);
319     bins DMA_DST_WR = binsof(ADDR.DMA_DST) && binsof(DIR.WRITE);
320     bins DMA_LEN_RD = binsof(ADDR.DMA_LEN) && binsof(DIR.READ);
321     bins DMA_LEN_WR = binsof(ADDR.DMA_LEN) && binsof(DIR.WRITE);
322     ignore_bins DMA_CMD_RD = binsof(ADDR.DMA_CMD) && binsof(DIR.READ);
323     bins DMA_CMD_WR = binsof(ADDR.DMA_CMD) && binsof(DIR.WRITE);
324     bins DMA_STATUS_RD = binsof(ADDR.DMA_STATUS) && binsof(DIR.READ);
325     ignore_bins DMA_STATUS_WR = binsof(ADDR.DMA_STATUS) && binsof(DIR.WRITE);
326   }
327 endgroup
295,1 95%

```


When to Sample

```
// Functional coverage
covergroup apb_cov @(posedge clk); // sample at posedge
    // more here
endgroup

apb_cov apb_cov_inst = new();
```

OR

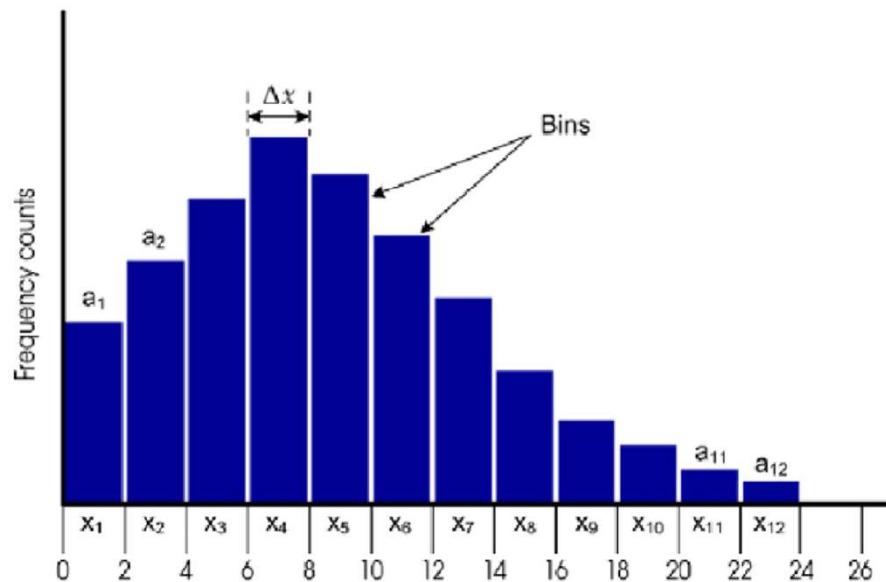
```
// Functional coverage
covergroup apb_cov;
    // more here
endgroup

apb_cov apb_cov_inst = new();

always @(posedge clk) // specify when to sample
    if (rst_n & apb_if.psel & apb_if.penable)
        apb_cov_inst.sample();
```

What to Sample: Coverpoint

- Specify which variable to be sampled
 - Can have a label (with ':')
 - Can have bins



```
DMAC_TOP_TB.sv (~/ECE4278_class/lab5/DMAC/SIM/TB) - GVIM@taurus
File Edit Tools Syntax Buffers Window Help
[Icons]
286 // Functional coverage
287 coverpoint apb_if.pwrite {
288     DIR: coverpoint apb_if.pwrite {
289         bins READ      = {0};
290         bins WRITE     = {1};
291     }
292     ADDR: coverpoint apb_if.paddr {
293         bins DMA_VER    = {'h0};
294         ignore_bins RSVD1 = [{'h4: 'hFC}];
295         bins DMA_SRC    = {'h100};
296         bins DMA_DST    = {'h104};
297         bins DMA_LEN    = {'h108};
298         bins DMA_CMD    = {'h10c};
299         bins DMA_STATUS = {'h110};
300         ignore_bins RSVD2 = [{'h114: $}]; // to maximum value
301     }
302     WDATA: coverpoint apb_if.pwdata {
303         bins ZERO       = {'h0};
304         bins ONE        = {'h1};
305         bins OTHERS     = [{'h2: $}]; // to maximum value
306     }
307     WDATA2: coverpoint apb_if.pwdata[1:0] {
308         bins MOD4_ZERO  = {'h0};
309         bins MOD4_ONE   = {'h1};
310         bins MOD4_TWO   = {'h2};
311         bins MOD4_THREE = {'h3};
312     }
313     SFR_RW: cross ADDR, DIR {
314         bins DMA_VER_RD = binsof(ADDR.DMA_VER) && binsof(DIR.READ);
315         ignore_bins DMA_VER_WR = binsof(ADDR.DMA_VER) && binsof(DIR.WRITE);
316         bins DMA_SRC_RD = binsof(ADDR.DMA_SRC) && binsof(DIR.READ);
317         bins DMA_SRC_WR = binsof(ADDR.DMA_SRC) && binsof(DIR.WRITE);
318         bins DMA_DST_RD = binsof(ADDR.DMA_DST) && binsof(DIR.READ);
319         bins DMA_DST_WR = binsof(ADDR.DMA_DST) && binsof(DIR.WRITE);
320         bins DMA_LEN_RD = binsof(ADDR.DMA_LEN) && binsof(DIR.READ);
321         bins DMA_LEN_WR = binsof(ADDR.DMA_LEN) && binsof(DIR.WRITE);
322         ignore_bins DMA_CMD_RD = binsof(ADDR.DMA_CMD) && binsof(DIR.READ);
323         bins DMA_CMD_WR = binsof(ADDR.DMA_CMD) && binsof(DIR.WRITE);
324         bins DMA_STATUS_RD = binsof(ADDR.DMA_STATUS) && binsof(DIR.READ);
325         ignore_bins DMA_STATUS_WR = binsof(ADDR.DMA_STATUS) && binsof(DIR.WRITE);
326     }
327 endgroup
```

295,1 95%

What to Sample: Cross Coverage

- Derived item from coverpoints
 - Check whether a combination of the cover points are hit
 - Can have bins

```

DMAC_TOP_TB.sv (~/ECE4278_class/lab5/DMAC/SIM/TB) - GVIM@taurus
File Edit Tools Syntax Buffers Window Help
[Icons]
286 // Functional coverage
287 covergroup apb_cov;
288   DIR: coverpoint apb_if.pwrite {
289     bins READ      = {0};
290     bins WRITE     = {1};
291   }
292   ADDR: coverpoint apb_if.paddr {
293     bins DMA_VER    = {'h0};
294     ignore_bins RSVD1 = [{'h4: 'hFC}];
295     bins DMA_SRC    = {'h100};
296     bins DMA_DST    = {'h104};
297     bins DMA_LEN    = {'h108};
298     bins DMA_CMD    = {'h10c};
299     bins DMA_STATUS = {'h110};
300     ignore_bins RSVD2 = [{'h114: $}]; // to maximum value
301   }
302   WDATA: coverpoint apb_if.pwdata {
303     bins ZERO       = {'h0};
304     bins ONE        = {'h1};
305     bins OTHERS     = [{'h2: $}]; // to maximum value
306   }
307   WDATA2: coverpoint apb_if.pwdata[1:0] {
308     bins MOD4_ZERO  = {'h0};
309     bins MOD4_ONE   = {'h1};
310     bins MOD4_TWO   = {'h2};
311     bins MOD4_THREE = {'h3};
312   }
313   SFR_RW: cross ADDR, DIR {
314     bins DMA_VER_RD = binsof(ADDR.DMA_VER) && binsof(DIR.READ);
315     ignore_bins DMA_VER_WR = binsof(ADDR.DMA_VER) && binsof(DIR.WRITE);
316     bins DMA_SRC_RD = binsof(ADDR.DMA_SRC) && binsof(DIR.READ);
317     bins DMA_SRC_WR = binsof(ADDR.DMA_SRC) && binsof(DIR.WRITE);
318     bins DMA_DST_RD = binsof(ADDR.DMA_DST) && binsof(DIR.READ);
319     bins DMA_DST_WR = binsof(ADDR.DMA_DST) && binsof(DIR.WRITE);
320     bins DMA_LEN_RD = binsof(ADDR.DMA_LEN) && binsof(DIR.READ);
321     bins DMA_LEN_WR = binsof(ADDR.DMA_LEN) && binsof(DIR.WRITE);
322     ignore_bins DMA_CMD_RD = binsof(ADDR.DMA_CMD) && binsof(DIR.READ);
323     bins DMA_CMD_WR = binsof(ADDR.DMA_CMD) && binsof(DIR.WRITE);
324     bins DMA_STATUS_RD = binsof(ADDR.DMA_STATUS) && binsof(DIR.READ);
325     ignore_bins DMA_STATUS_WR = binsof(ADDR.DMA_STATUS) && binsof(DIR.WRITE);
326   }
327 endgroup
    
```


Functional Coverage in Verdi

<Verdi:vdCoverage:1> <vdb: VDB.vdb>@taurus

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Avg. Group Score:83.33% U+C:24 U:3 C:21 X:0
Avg. Group Inst. Score:83.33% U+C:24 U:3 C:21 X:0

Group	Score	Instances	U+C	U	C	X	Ge
DMAC_TOP_TB::apb_cov	83.33%		24	3	21	0	10
Cp ADDR	100.00%		6	0	6	0	10
Cp DIR	100.00%		2	0	2	0	10
Cp WDATA	66.67%		3	1	2	0	10
Cp WDATA2	50.00%		4	2	2	0	10
Cr SFR_RW	100.00%		9	0	9	0	10

CovSrc:1: DMAC_TOP_TB::apb_cov

Uncovered

```

312      ADDR: coverpoint apb_if
      .paddr {
313          bins DMA_VER
            = {'h0'};
314          ignore_bins RSVD1
            = {'h4':'hFC'};
315          bins DMA_SRC
            = {'h100'};
316          bins DMA_DST
            = {'h104'};
317          bins DMA_LEN
            = {'h108'};
318          bins DMA_CMD
            = {'h10c'};
319          bins DMA_STATUS
            = {'h110'};
320          ignore_bins RSVD2

```

CovDetail

Cross 2D Proj

Cover Group Item	Score
Cp DIR	100.00%
Cp WDATA	66.67%
Cp WDATA2	50.00%
Cr SFR_RW	100.00%

Status	Bin Nam	Type	At Least
X	DMA_CM...	User	
✓	DMA_CM...	User	
✓	DMA_DST...	User	
✓	DMA_DST...	User	
✓	DMA_LEN...	User	

Message

The design 'VDB.vdb' was loaded successfully.
The following test is loaded from "VDB.vdb",
VDB/test

Exclusion Manager Requirements Manager Message

Assignment: AWLEN Functional Coverage

- Goal:
 - Check whether our simulations cover all AWLEN values
 - AWLEN=0 → burst 1, AWLEN=1 → burst 2, ..., AWLEN=15 → burst 16
- How
 - Add coverage items to SIM/TB/DMAC_TOP_TB.sv
 - Steps
 1. Create a coverage group
 2. Create a coverpoint for AWLEN (label: AWLEN_CP)
 3. Create 16 bins (one for each AWLEN) for the coverpoint
 - Bins name : AWLEN=0 → LEN01, AWLEN=1 → LEN02, ..., AWLEN=15 → LEN16
 4. Instantiate the coverage group (covergroup name: aw_cov)
 5. Make the coverage group to be sampled at AW handshake
 - i.e., rst & AWVALID & AWREADY

Expected Output

CovDetail

*

Cover Group Item	Score	Instances	U+C	U	C	X	Goal	Weight	AtLeast	PerInst	Overlap	AutoBin	Missing
DMAC_TOP_TB::aw_cov	100.00%		16	0	16	0	100%	1	1	0	1	64	64
AWLEN_CP	100.00%		16	0	16	0	100%	1	1		1	0	

Status	Bin Name	Type	At Least	Size	Hit Count
✓	LEN01	User	1	1	1
✓	LEN02	User	1	1	1
✓	LEN03	User	1	1	1
✓	LEN04	User	1	1	1
✓	LEN05	User	1	1	1
✓	LEN06	User	1	1	1
✓	LEN07	User	1	1	1
✓	LEN08	User	1	1	1
✓	LEN09	User	1	1	1
✓	LEN10	User	1	1	1
✓	LEN11	User	1	1	1
✓	LEN12	User	1	1	1
✓	LEN13	User	1	1	1
✓	LEN14	User	1	1	1
✓	LEN15	User	1	1	1
✓	LEN16	User	1	1	64



Submission



- Upload DMAC_TOP_TB.sv on icampus
 - Do not change the file name
 - It is okay to have -1, -2, ... at the end of the file name
- Due: Sun. 4/13, 23:59