This document is presented to you by YILMAZ and it is the property of YILMAZ. Use it as it is. I do not take any responsibility. You are free to us it, because this has been made without any investment of FONTYS.

Working method by Digital Audio System:

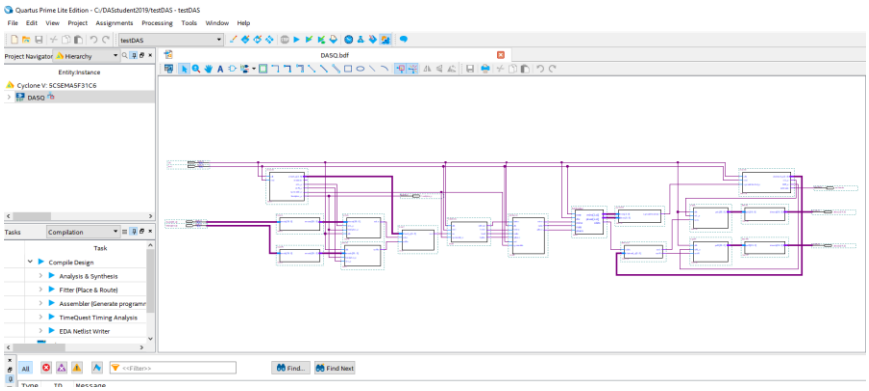
Please note that you can make use of the reference model if you have Quartus Prime Version 17.0.0 Build 595 04/25/2018 SJ Lite Edition and Modelsim – INTEL FPGA STARTER EDITION 10.5b. This is what provided from Fontys University. Other versions will not be supported and there will be no models for the other versions. There is a zip file under the practical directory of DD3 on the portal. If you extract it, you will get the following file structure.

Figure 1. File structure

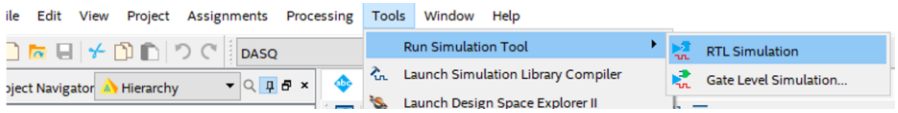
Please note that there is a work directory under simulation. This is the place where we have the reference model. Please do not change anything as far as the work directory concerned. If you did something wrong please copy work-orig to work to get the starting point again.

Steps to verify the reference model of Digital Audio System:

1. Extract the zip file. Very long names or complex directory names or path names with special characters in it can give you some troubles.
2. Go to the place where you have the project. See file structure.
3. Double click on the project file to open the project. Your window will look like the following.

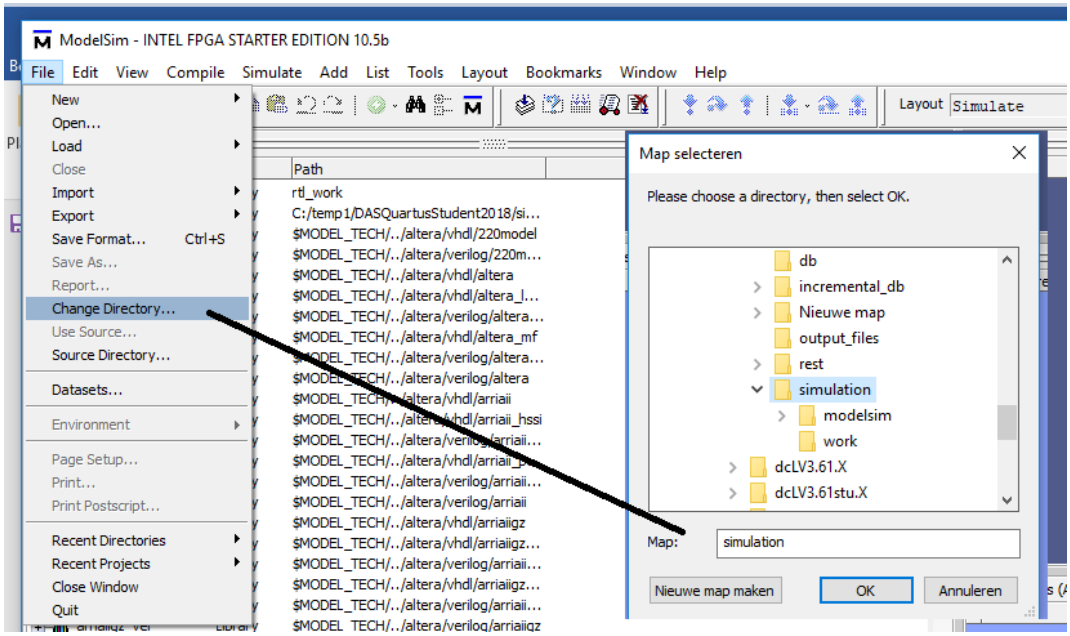


4. You can now simulate the reference model by clicking on the **Run simulation tool ->RTL simulation from the Tools menu.**



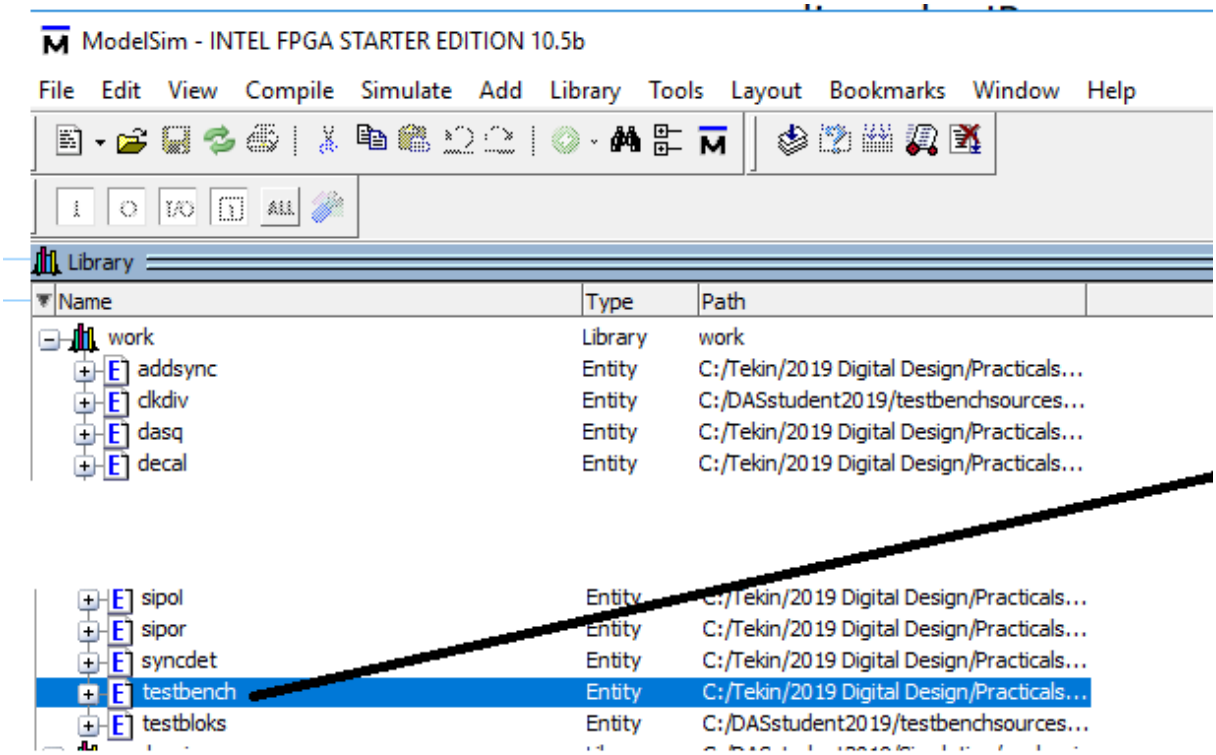
Now Modelsim has been started. Please wait till everything has been compiled.

5. Now, go to File in the Modelsim window and click on Change Directory. Select Simulation in the new window and click ok.

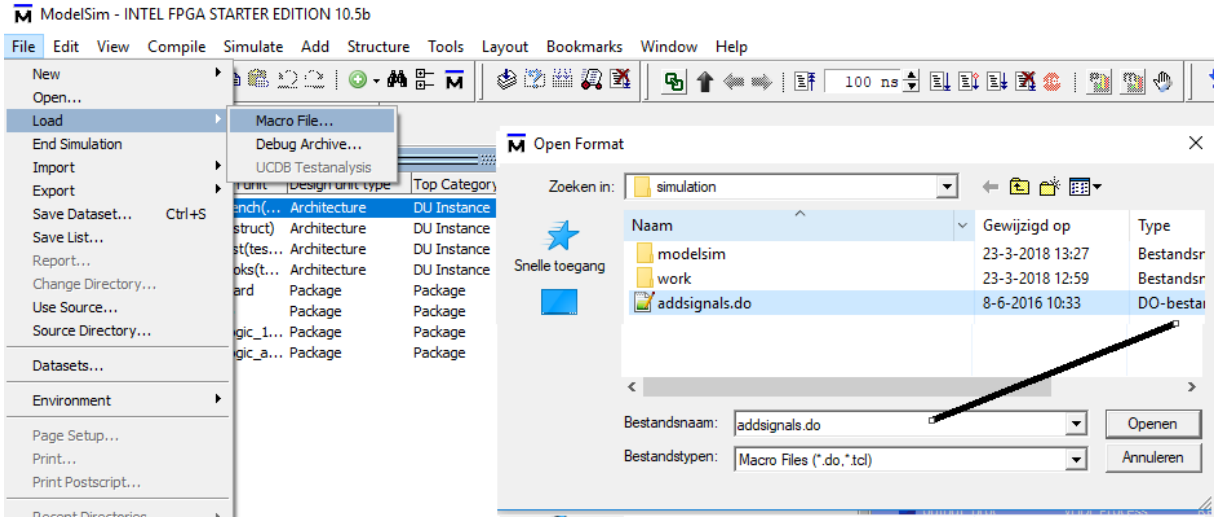


Please note that the directories depend on the extracted place of your project. Hence, know what you are doing.

6. Double click on testbench from the work->testbench to start simulation



7. Select the necessary inputs and outputs that you want to observe and add them to the wave window. If you want to use the one that lecturer has made please run the following macro.
   Go to File->Load and click on Macro File. In the opened window select addsignals.do and click on Open(en).

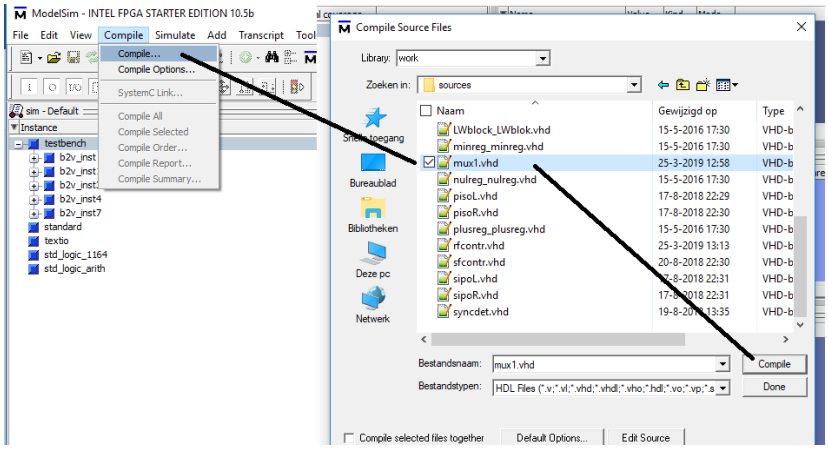


8. Of course, you can add any other signal or variable to the simulation to observe it. Because the lecturer has made a testbench, the signals at the input side will be generated automatically. The signals at the output side will be shown with an extra signal called ok. If the OK signal is 1 then your system is working correctly. If it is 0, it fails. Rest to run the simulation with RUN <any number>. For example
   RUN 8000000
9. Following the steps above will give you the correct behavior of the Digital Audio System. If not you did not follow the steps correctly.
10. Now you know how the DAS works you can start making your own design. Please note that you can make use of any of the following design methods.
    - truth table (DD1)
    - function table (DD1)
    - state diagram (DD2)
    - state table (DD2)
    - ASM (DD3)
    - Functional (DD1)
    - RTL (DD2)
    - Structural (DD3)
    - Concurrent statements (DD3)
    - procedures and functions (DD3)
    - Mix of the above

    Every block can now be designed separately one by one and tested in the environment. To do this use the steps below

Steps to design and verify the blocks one by one of Digital Audio System:

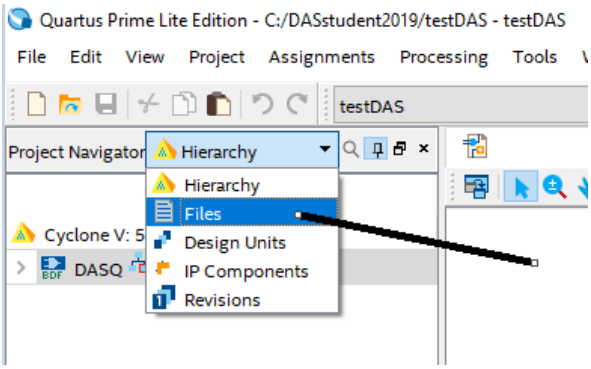
1. From Quartus open any block for example mux1 and design it according to one of the following methods (Read the comments and obey the design rules):
   - truth table (DD1)
   - function table (DD1)
   - state diagram (DD2)
   - state table (DD2)
   - ASM (DD3)
   - Functional description (DD1)
   - RTL description (DD2)
   - Structural description (DD3)
   - Concurrent statements (DD3)
   - procedures and functions (DD3)
   - Mix of the above
2. Start Moelsim if it is not yet started and change directory to simulation (step 4 and 5 from the first part: **Steps to verify the reference model of Digital Audio System**)
3. Compile the designed block for example mux1.vhd from the Modelsim (component) and click on Done.



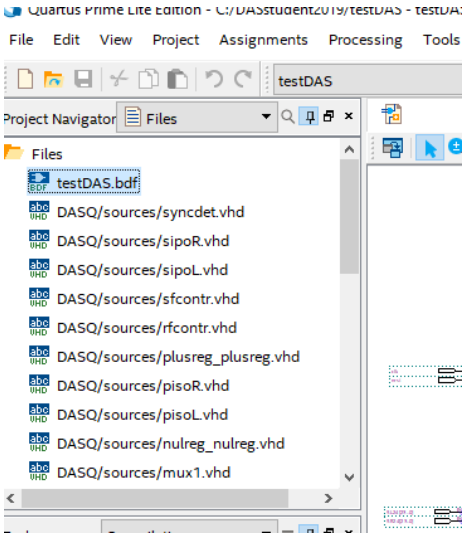
4. Double click on testbench from the work->testbench to start simulation(step 6 from the first part: **Steps to verify the reference model of Digital Audio System**).
5. Select the necessary inputs and outputs that you want to observe and add them to the wave window. If you want to use the one that lecturer has made please run the following macro.
   Go to File->Load and click on Macro File. In the opened window select addsignals.do and click on Open(en)(step 7 from the first part: **Steps to verify the reference model of Digital Audio System**)
6. Check simulation result to see whether the system is working as in case of the reference model. If so, your block has been designed correctly. If not, block is not correctly designed. Correct it and repeat the steps above.
7. Repeat the above steps also for the other blocks one by one to complete the whole design.

Steps to test and demonstrate the DAS(Digital Audio System):

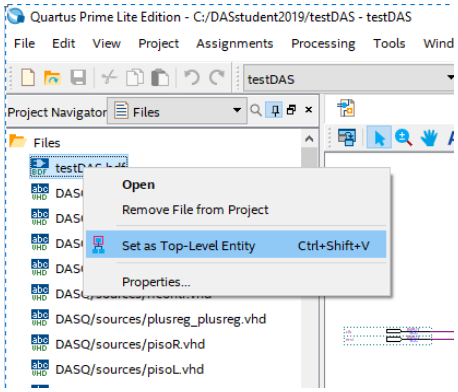
1. Open the project by double clicking on testDAS.qpf if it is not opened yet.
2. Go to Hierarchy and select files



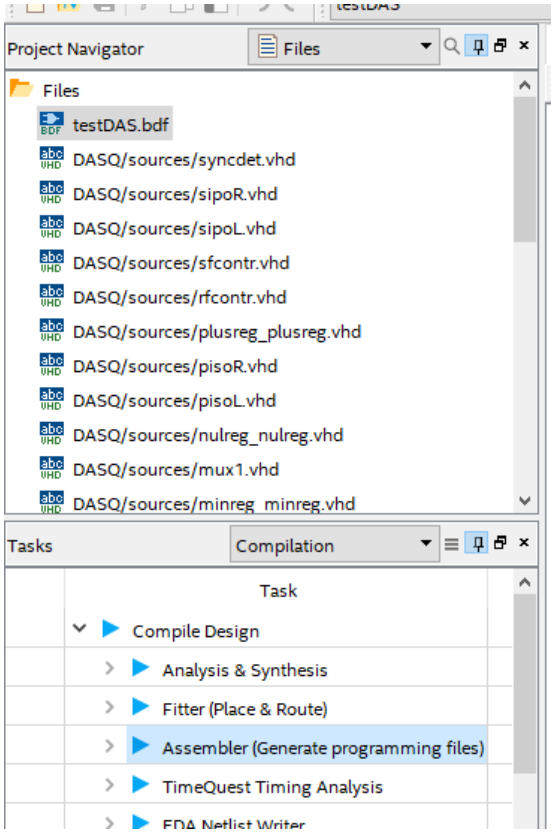
Your project navigator will look like the following:



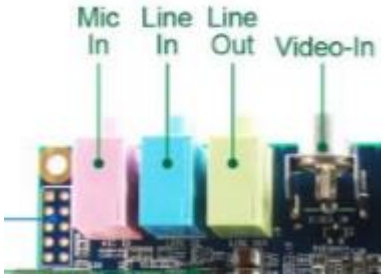
3. Select testDAS.bdf and right click on mouse and click on Choose Set as Top-Level Entity.



4. Double click on Assembler (Generate Programming Files)



5. After compilation program and test your device. Use Line In and Line Out.



Deliverables:

1. A working demonstration of Digital Audio System

2. A report containing the following

- a brief introduction
- design
- research encryption, decryption, HDB3, sampling and frame
- analysis and verification of the design
- a brief conclusion
- annex: must include all of the sources like VHDL, ASM, state diagram, truth table, block diagram etc.

PLEASE PREPARE the subjects as indicated in the manual. If you did not succeed after one(1) hour of preparation, please put everything what you have done in this one hour, on paper and send it to lecturer. Without this, you didn't do any preparation and did not spend any effort/hours in this course.

GOOD LUCK