Design should be fine. Checked gain and frequency response (fc can be decreased if desired, but this fr is recomended by the datasheet)

+12V
V1
{C}
V2
{C}
-12V

.OPTIONS nomarch
.options plotwinsize 0
.options numdgt 7
;options maxstep 10n
.param C=12
.param U=9.75

.options maxstep 1u
.savebias stab.txt internal time=500u repeat
.tran 0 10m 5m uic

.ac dec 1000 10 1MEG
*.loadbias stab.txt

Fc=-3dB=218kHz

Gain here increases CMRR
Just place footprints of Rf1, Rg1 & Rg2 on PCB

Charge glitch reservoir for the ADC

Input range is 0 to 5V, referenced to 2.5V

HOT

V3
SINE(0 {U} 1k 0)
AC 1

V6
AC 1
PULSE(0 {U/2} 0 1n 1n 500u 1m 10)

V4
SINE(0 {U} 1k 0)
AC 1

SINE(0 {U} 1k 0)
PULSE(0 {U} 0 1u 1u 0 1m 10)

COLD

R7   220
R12 47k
C4   3n3

R14 2Meg2
Rf1 1k

R13 47k
R9   220
C5   3n3

-12V
LM4562
LT6220
U3
+12V
Rg1 0

+12V
U4
Rg2 0
-12V
LT6220
LM4562

R1 1k
R2 1k

C1 1n
U1
VDCM
OPA1632
C2 1n

R3 270
R5 39
R6 39
R4 270

+12V
-12V

C3 2n7

PCM1804
RI- 10k
RI+ 10k

VCOM
V5 2.5

U2
+12V
LT6220
LM4562
-12V
fc=1592Hz
R10 1k
C10 100n