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Plan of Approach

Audio digital signal processor

BeCreative Minor

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Abbreviation List

Abbreviation	Explanation
DSP	Digital Signal Processor
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter

Chapter 1: Background

When listening to music it is of great importance that the speakers are tuned to the environment and the position of the listener. This is necessary to achieve the best experience. If the speakers are not correctly tuned to the surrounding environment, a digital signal processor (DSP) is used to correct this. A DSP is a specialized processor which is used for digital signal processing.

In the audio world a DSP is used to optimize a sound system. For example some speakers have some imperfections and a DSP can be used to correct for these imperfections. It is also often used to add more dynamics to sound.

Chapter 2: Project result

The goal of this project is to research how to make an audio-DSP. This raises the main research question: **"How to design an audio-DSP?"**. In the process of researching this an actual audio-DSP will be developed. From the main research question the following sub-research questions are derived:

- What is the best method for creating digital filters?
- What is the best method for creating digital effects?
- What is the most suitable anti-aliasing filter?
- What is the optimal needed roll-off for the anti-aliasing filter for a given bandwidth such that the noise can be negligible?
- What is the minimum sample frequency needed to capture the desired frequency spectrum?
- What is the minimum frequency range to be sampled to achieve sufficient detailed audio?
- What is the lowest allowable noise for decent audio?
- What ADC resolution is needed such that the quantization error and noise level are on par?
- What ADC and DAC architecture is most suitable for this application?
- What kind of processor is most suitable for this application?
- What is the permittable jitter for accurate audio?
- What is the maximum allowable ripple on the reference voltage for the ADC and DAC?
- How much RAM does the system need?
- How much flash does the system need?
- What power supply topology is best suited for each part of the system?

The project is conducted during the minor BeCreative at Fontys. This minor takes 20 weeks and allows the students to have a budget of €300,-. Thus after 20 weeks starting from 6-2-2023 an audio-DSP will be delivered within a budget of €300,-.

The audio system has some requirements to specify the final result. These requirements are derived with the "MoSCoW" method. It must be noted that the following requirements will be confirmed by the research that will be conducted.

2.1 Must have (to be confirmed by research)

- Two RCA audio inputs which work on a line level of 4 dBu (±1,74 V).
- Two 6,35 mm TRS plug audio inputs which work on a line level of 4 dBu (±1,74 V).
- Two XLR audio inputs which work on a line level of 22 dBu (±9,75 V).

- USB type B audio input
- Two RCA audio outputs which work on a line level of 4 dBu (±1,74 V).
- Two 6,35 mm TRS plug audio outputs which work on a line level of 4 dBu (±1,74 V).
- Four XLR signal outputs work on a line level of 22 dBu (±9,75 V).
- The system has a bandwidth (±3 dB) of at least 20 Hz up and till 20 kHz without any filters applied.
- The system has an audio sample rate of at least 44.1 kHz.
- The ADC resolution should be at least 16-bit.
- The DAC resolution should be at least 16-bit.
- propagation time delay of less than 100 ms without any filters applied.
- User can select what input will be used via an user interface
- User can select up to 4 effects to be active in one channel at the same time
- User can configure each effects
- The system must work stand alone and be configurable via a basic graphical user interface.
- Effects configurable per output channel at least four different sound effects should be able to be applied to each signal output signal at the same time:
  - Distortion
  - Reverb
  - Gain
  - Equalizer
  - Delay

2.2 Should have (to be confirmed by research)

- The system should have a bandwidth (±1 dB) of at least 20 Hz up and till 20 kHz without any filters applied.
- Audio sample rate of at least 96 kHz
- The ADC resolution should be at least 24-bit.
- The DAC resolution should be at least 24-bit.
- Six XLR signal outputs work on a line level of 22 dBu (±9,75 V).
- User can select up to 10 effects to be active in one channel at the same time.
- Low enough jitter to not influence the audio quality to much.
- Filters:
  - Tremelo
  - Flanger
  - Fuzz
  - Overdrive
  - Chorus
  - Compressor
  - Wah
  - Looper
  - Overdrive

  - Wow and flutter
  - Modulator
  - Echo
  - Fade in

2.3 Could have (to be confirmed by research)

- Audio sample rate of at least 192 kHz
- Touch screen user interface.

2.4 Won't have (to be confirmed by research)

- Self-made mains power supply.

Chapter 3: Project activities

In order to realise this project, the activities need to be devised. describing the end-product in precise terms will make it easier to devise those tasks. These activities are:

- Planning
- Research
- Designing
- Testing
- Writing documentation
- Budget tracking

3.1 Planning

The planning is one of the most important stages within the project activities, this gives you the broad overview over the whole project and what it is going to look like. In order to determine the activities, progress, costs, duration and delay of a project, a planning is of the essence. The planning will be divided into two separate parts:

- Global planning
- Personal (weekly or daily) planning

The global planning will be made in Gantt-chart style. The personal planning is freer of choice depended on the team member itself.

3.2 Research

In chapter 2 Project result the research questions are described. Those questions need to be answered before specifying the things that are needed to start working on this project. This phase is especially important because of its responsibility that it carries in future development of the project. The better the research is done, the less wrongly things will be executed in the future stage of the project, which will save time. The research questions will be separated in two categories:

- The research questions that will be split into the team members that have the interest in the specific subject based on their PDP.
- The research questions that needed to be discussed in a group matter, so everyone is on par with the research and knowledge.

3.3 Designing

During this stage most of the research will have been completed and the tasks will be divided into the team members. Depended on the PDP and the preferred modules the team members will work either together or alone on a module. While designing the other team members will be updated in the weekly meetings.

3.4 Testing

After the design phase the modules will be put together and will be tested based on the test report.

3.5 Writing Documentation

If all the necessary requirements (user and functional) are fulfilled and testing is done, the evidence will be put in the final report.

3.6 Budget tracking

Fontys has provided us with a budget of €300, - for the completion of this project. The most expensive parts expected will be the processor, the ADC's and the DAC's.

3.7 Activities

- Reporting
  - Creating SRD
  - Creating SDD
  - Creating MDD
  - Creating final report
- Researching research questions
  - Creating research document
- Designing
  - Design firmware:
    - Design input MUX
    - Design sampler
    - Design USB decoder
    - Design output MUX
    - Design signal processor:
      - Design effect manager
      - Design/model/simulate effects
      - Design/model/simulate filters

        * Design controller
    - Design hardware:
        * Design input selector
        * Design anti-aliasing filters
        * Design output filter
        * Design buffer
        * Design XLR balanced-to-unbalanced converter
        * Design XLR unbalanced-to-balanced converter
        * Design processor core
        * Design local power supplies
        * Design housing
    - Design user interface
- Realisation
    - Program firmware:
        * Program ADC and DAC interface
        * Program sampler
        * Program USB decoder
        * Program MUX
        * Program signal processor:
            · Program effect manager
            · Program filters
            · Program effects
        * Program controller
    - Create hardware:
        * Create housing
        * Realize PCB
    - Program user interface
- Testing
    - Verify firmware:
        * Verify ADC and DAC interface
        * Verify Sampler
        * Verify USB decoder
        * Verify MUX
        * Verify signal processor:
            · Verify effects manager
            · Verify filters
            · Verify effects
        * Verify controller
    - Verify hardware

– Verify user interface

Chapter 4: Project boundaries

¡¡¡¡¡¡¡ Updated upstream The needed mains power supply will not be made during this project and will be bought externally.

For the power supply a transformer is used to make a safe voltage. ======= The needed mains power supply will not be made during this project and will be bought externally. For the power supply a transformer is used to make a safe voltage. ¿¿¿¿¿¿¿ Stashed changes

Chapter 5: Milestones

¡¡¡¡¡¡¡ Updated upstream The following milestones will be achieved as a result of the project activities as in Chapter 3.

- Reports:
  - Research document
  - SRD
  - SDD
  - MDD
  - Final report
- Designs:
  - Firmware design:
    - Input MUX design
    - Sampler design
    - USB decoder design
    - Output MUX design
    - signal processor design
      - Effect manager design
      - Effects design/model
      - Filters design/model
    - controller design
  - Hardware design:
    - Input selector design
    - Anti-aliasing filters design
    - Output filter design
    - Buffer design
    - XLR balanced-to-unbalanced converter design
    - XLR unbalanced-to-balanced converter design
    - processor core design
    - Local power supplies design
    - Housing design
  - User interface design

- Realistation:
  - Firmware:
    - Program ADC and DAC interface
    - Program sampler
    - Program USB decoder
    - Program MUX
    - Program signal processor
      - Program effect manager
      - Program filters
      - Program effects
    - Program controller
  - Hardware:
    - Housing
    - PCB
  - User interface

======= The following milestones will be achieved as a result of the project activities described in chapter 3.

- Reports
  - Research document
  - SRD
  - SDD
  - MDD
  - Creating final report
- Designs
  - Firmware design:
    - Input MUX design
    - Sampler design
    - USB decoder design
    - Output MUX deisgn
    - Signal processor design:
      - Effect manager design
      - Effects design/model
      - Filter design/model
    - Controller design
  - Hardware design:
    - Input selector design
    - Anti-aliasing filters design
    - Output filter design

        * Buffer design
        * XLR balanced-to-unbalanced converter design
        * XLR unbalanced-to-balanced converter design
        * Processor core design
        * Local power supplies design
        * Housing design
    - User interface design
- Realisation
    - Firmware:
        * Program ADC and DAC interface
        * Program sampler
        * Program USB decoder
        * Program MUX
        * Program signal processor:
            · Program effect manager
            · Program filters
            · Program effects
        * Program controller
    - Create hardware:
        * Housing
        * PCB
    - User interface

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Chapter 6: Quality assurance

¡¡¡¡¡¡¡ Updated upstream To assure that the quality is monitored the following things will be done:

- Version-control with GitHub
- Documents will be written in LaTeX
- Weekly activities will be monitored to guard the process.
- The PCB design will be made in KiCad
- C++ code is written with Microsoft Visual Studio ======= To assure that the quality is monitored the following things will be done:

  - Version-control with GitHub
  - Documents will be written in LaTeX
  - Weekly activities will be monitored to guard the process
  - The PCB design will be made in KiCad
  - C++ code is written with Microsoft Visual Studio ¿¿¿¿¿¿¿ Stashed changes

Chapter 7: Project organisation

¡¡¡¡¡¡¡ Updated upstream

- Weekly meetings
- Roles within the project:
  - Communicator
  - Minute-taker
  - Chairman/project-leader
  - Accountant

Role	**Assigned person**	**Back-up person**
Communicator	Robin van den Dungen	Silas Kamphuis
Minute-taker	Ahmed Abdelrahim	Mahmud Gürler
Chairman/project-leader	Youri Tils	Robin van den Dungen
Accountant	Hein Verhallen	Silas Kamphuis
Editor	Busse Lommers	Hein Verhallen
Version-controller	Hein Verhallen	Youri Tils

Table 7.1: Role division

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- Weekly meetings
- Roles within the project:
  - Communicator
  - Minute-taker
  - Chairman/project-leader
  - Accountant (keep track of orders and budget)

Role	**Assigned person**	**Back-up persons**
Communicator	Robine van den Dungen	Silas Kamphuis
Minute-taker	Ahmed Abdelrahim	Mahmud Gürler
Chairman/project-leader	Youri Tils	Robin van de Dungen
Accountant	Hein Verhallen	Silas Kamphuis
Editor	Busse Lommers	Hein Verhallen
Version-controller	Hein Verhallen	Youri Tils

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Chapter 8: Planning

Chapter 9: Cost-benefit overview

Chapter 10: Risk Analysis

There are many risks and reasons why a project might fail or go bad, A change in organizational priorities is the most common reason. A change in project objectives is also common as poor communication and unclear risk definition.

- Unclear or shifting goals.
- lack of planning.
- lack of follow up.
- timing issues
- Lack of risk management.
- Unsuitable tools.
- Too many unsuitable tools

For these reasons and many more, we've created an overall table with ratings which rate the opportunity/effect and risk.

Scale

Ratings that can be seen below are from 1 to 9. Where 1 is low risk and 9 is high risk.

Risk	Opportunity	Effects	Risk	Measure to prevent / Remedy it	Change after	Consequences afterwards	Ultimate risk
A group member lacks in work / failed deadlines.	4	2	8	Code of conduct created and singed by everyone	3	3	4
Clear file locations and easy to map.	3	3	6	Weekly document tracking and documentation is taken.	2	3	3
Behind schedule for lack of knowledge or confusion.	4	3	7	Ask for help in time from fellow group members or teachers.	1	2	2
Running low on budget.	1	6	5	Budget is documented.	1	3	1
There is insufficient communication in the group.	2	3	6	Meetings will be scheduled 2-3 times a week, minutes and notes are taken and uploaded up to date.	1	3	3
Clear results are missing.	4	6	9	The strip planning clearly states which part you need to complete to be on schedule with each part of the project.	2	3	6
Shortage in components	2	9	3	A delay in ordering or receiving parts	6	6	9
The planning of Fontys teaching material is incorrect.	4	5	9	Read documents carefully	4	7	7

Table 10.1: Risk analysis

Appendix A: Appendix A