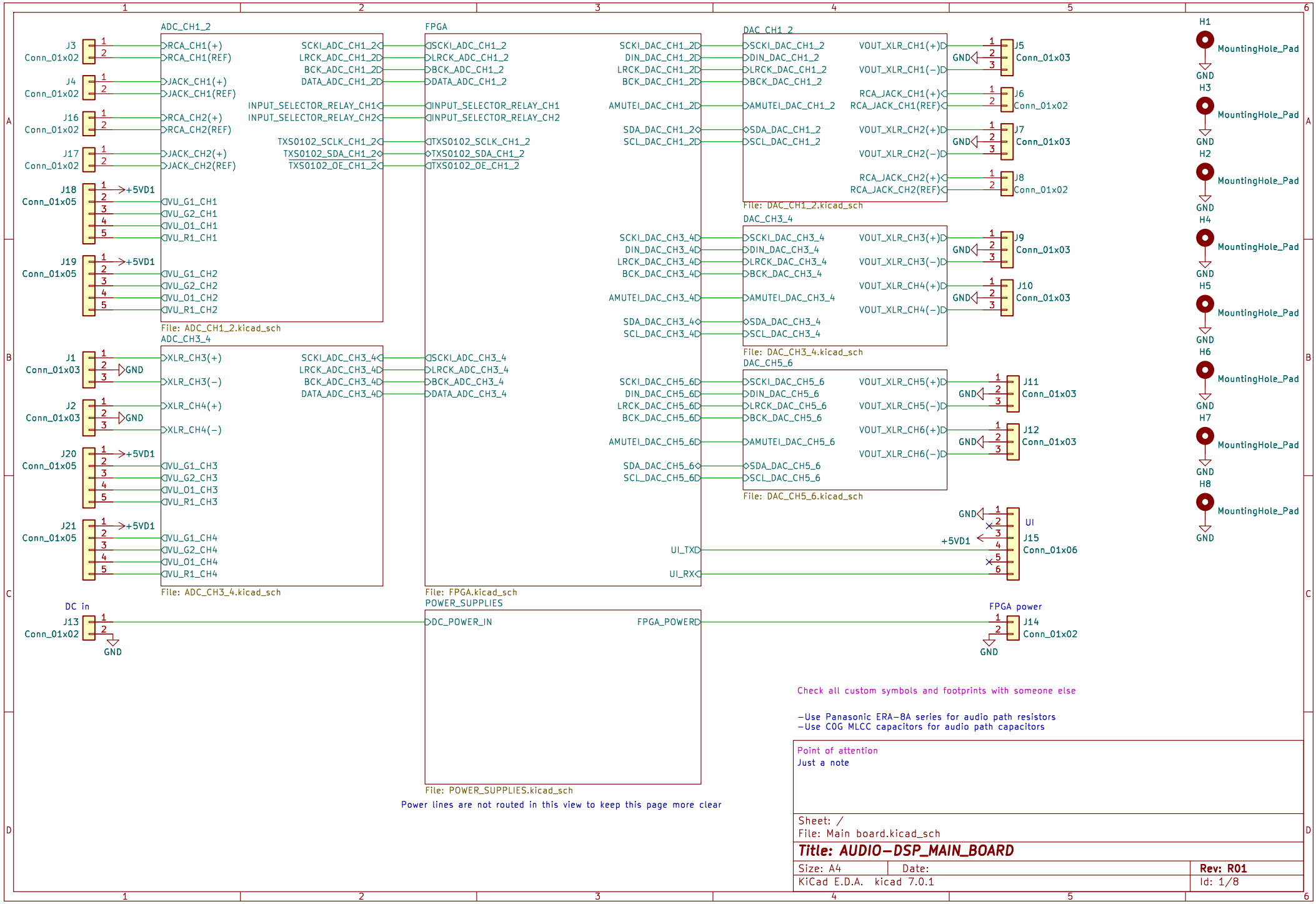
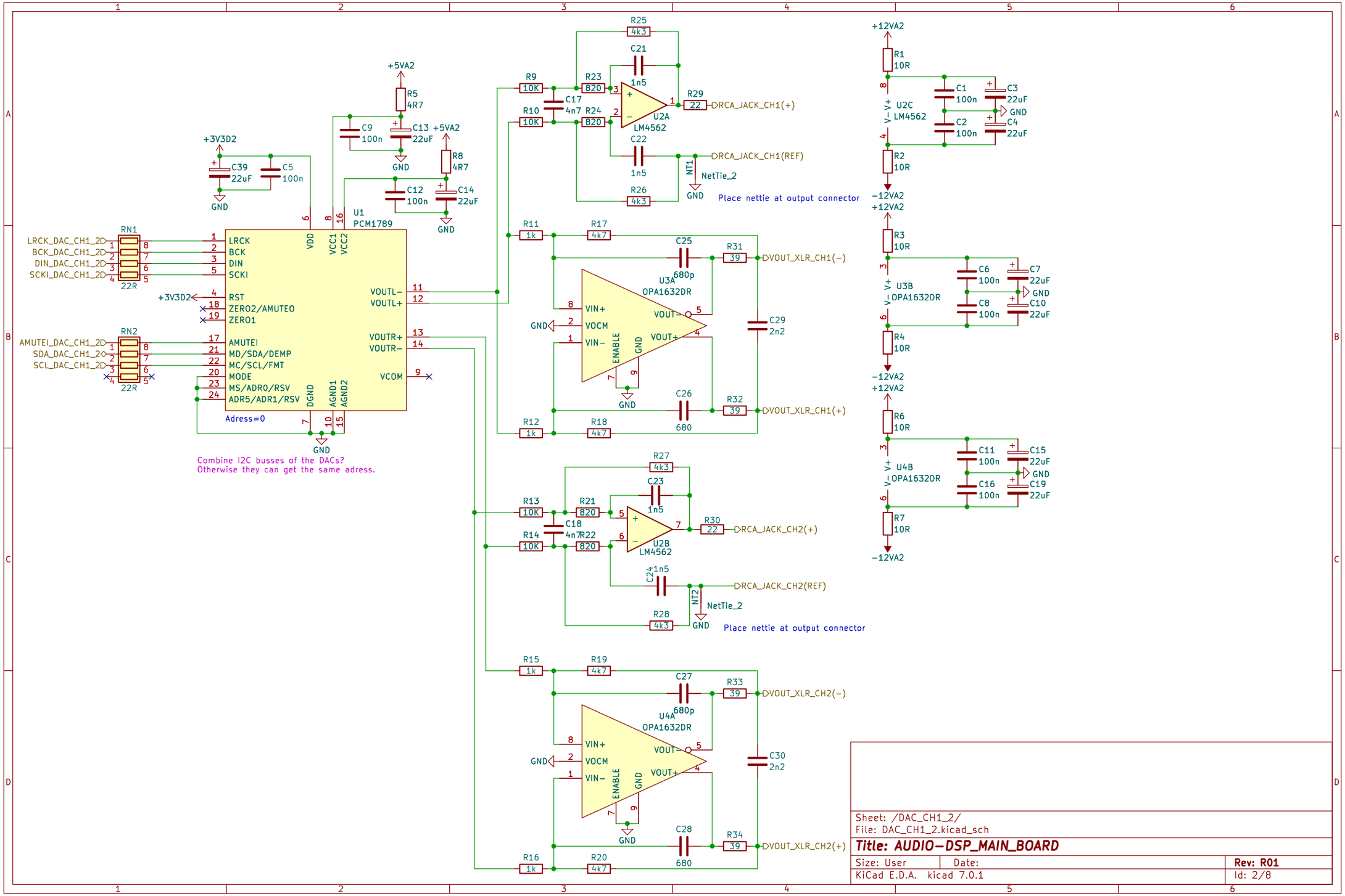
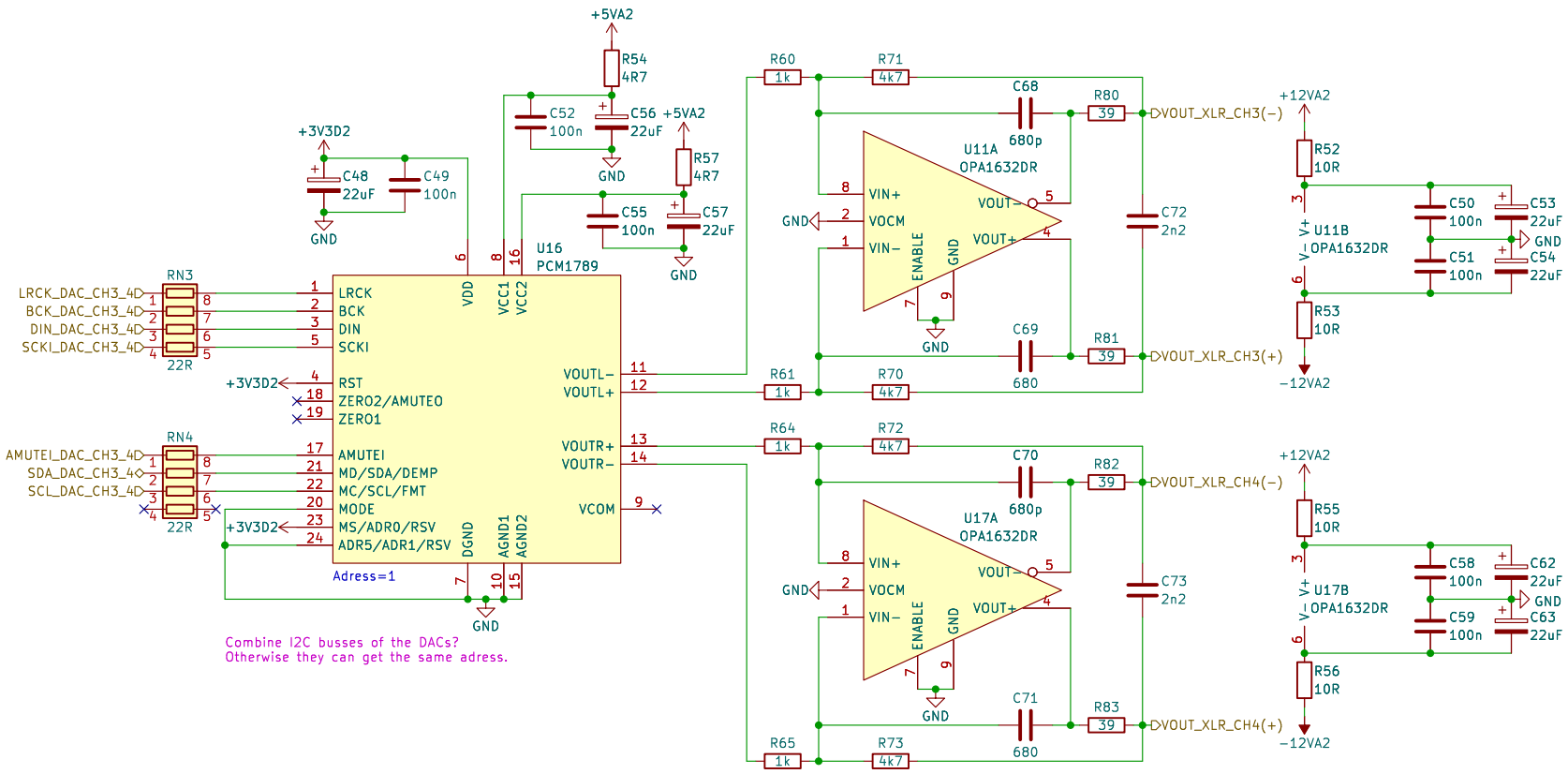

ADC_CH1_2
RCA_CH1(+)
RCA_CH1(REF)
JACK_CH1(+)
JACK_CH1(REF)
RCA_CH2(+)
RCA_CH2(REF)
JACK_CH2(+)
JACK_CH2(REF)
VU_G1_CH1
VU_G2_CH1
VU_O1_CH1
VU_R1_CH1
VU_G1_CH2
VU_G2_CH2
VU_O1_CH2
VU_R1_CH2
SCKI_ADC_CH1_2
LRCK_ADC_CH1_2
BCK_ADC_CH1_2
DATA_ADC_CH1_2
INPUT_SELECTOR_RELAY_CH1
INPUT_SELECTOR_RELAY_CH2
TXS0102_SCLK_CH1_2
TXS0102_SDA_CH1_2
TXS0102_OE_CH1_2
File: ADC_CH1_2.kicad_sch
ADC_CH3_4
XLR_CH3(+)
XLR_CH3(−)
XLR_CH4(+)
XLR_CH4(−)
VU_G1_CH3
VU_G2_CH3
VU_O1_CH3
VU_R1_CH3
VU_G1_CH4
VU_G2_CH4
VU_O1_CH4
VU_R1_CH4
SCKI_ADC_CH3_4
LRCK_ADC_CH3_4
BCK_ADC_CH3_4
DATA_ADC_CH3_4
File: ADC_CH3_4.kicad_sch
FPGA
SCKI_DAC_CH1_2
DIN_DAC_CH1_2
LRCK_DAC_CH1_2
BCK_DAC_CH1_2
AMUTEI_DAC_CH1_2
SDA_DAC_CH1_2
SCL_DAC_CH1_2
SCKI_DAC_CH3_4
DIN_DAC_CH3_4
LRCK_DAC_CH3_4
BCK_DAC_CH3_4
AMUTEI_DAC_CH3_4
SDA_DAC_CH3_4
SCL_DAC_CH3_4
SCKI_DAC_CH5_6
DIN_DAC_CH5_6
LRCK_DAC_CH5_6
BCK_DAC_CH5_6
AMUTEI_DAC_CH5_6
SDA_DAC_CH5_6
SCL_DAC_CH5_6
UI_TX
UI_RX
File: FPGA.kicad_sch
DAC_CH1_2
VOUT_XLR_CH1(+)
VOUT_XLR_CH1(−)
RCA_JACK_CH1(+)
RCA_JACK_CH1(REF)
VOUT_XLR_CH2(+)
VOUT_XLR_CH2(−)
RCA_JACK_CH2(+)
RCA_JACK_CH2(REF)
File: DAC_CH1_2.kicad_sch
DAC_CH3_4
VOUT_XLR_CH3(+)
VOUT_XLR_CH3(−)
VOUT_XLR_CH4(+)
VOUT_XLR_CH4(−)
File: DAC_CH3_4.kicad_sch
DAC_CH5_6
VOUT_XLR_CH5(+)
VOUT_XLR_CH5(−)
VOUT_XLR_CH6(+)
VOUT_XLR_CH6(−)
File: DAC_CH5_6.kicad_sch
J3 Conn_01x02
J4 Conn_01x02
J16 Conn_01x02
J17 Conn_01x02
J18 Conn_01x05
J19 Conn_01x05
J1 Conn_01x03
J2 Conn_01x03
J20 Conn_01x05
J21 Conn_01x05
+5VD1
GND
J5 Conn_01x03
J6 Conn_01x02
J7 Conn_01x03
J8 Conn_01x02
J9 Conn_01x03
J10 Conn_01x03
J11 Conn_01x03
J12 Conn_01x03
UI
J15 Conn_01x06
H1 MountingHole_Pad
H2 MountingHole_Pad
H3 MountingHole_Pad
H4 MountingHole_Pad
H5 MountingHole_Pad
H6 MountingHole_Pad
H7 MountingHole_Pad
H8 MountingHole_Pad
DC in
J13 Conn_01x02
POWER_SUPPLIES
DC_POWER_IN
FPGA_POWER
File: POWER_SUPPLIES.kicad_sch
Power lines are not routed in this view to keep this page more clear
FPGA power
J14 Conn_01x02
Check all custom symbols and footprints with someone else
−Use Panasonic ERA−8A series for audio path resistors
−Use C0G MLCC capacitors for audio path capacitors
Point of attention
Just a note
Sheet: /
File: Main board.kicad_sch
Title: AUDIO−DSP_MAIN_BOARD
Size: A4
Date:
Rev: R01
KiCad E.D.A. kicad 7.0.1
Id: 1/8

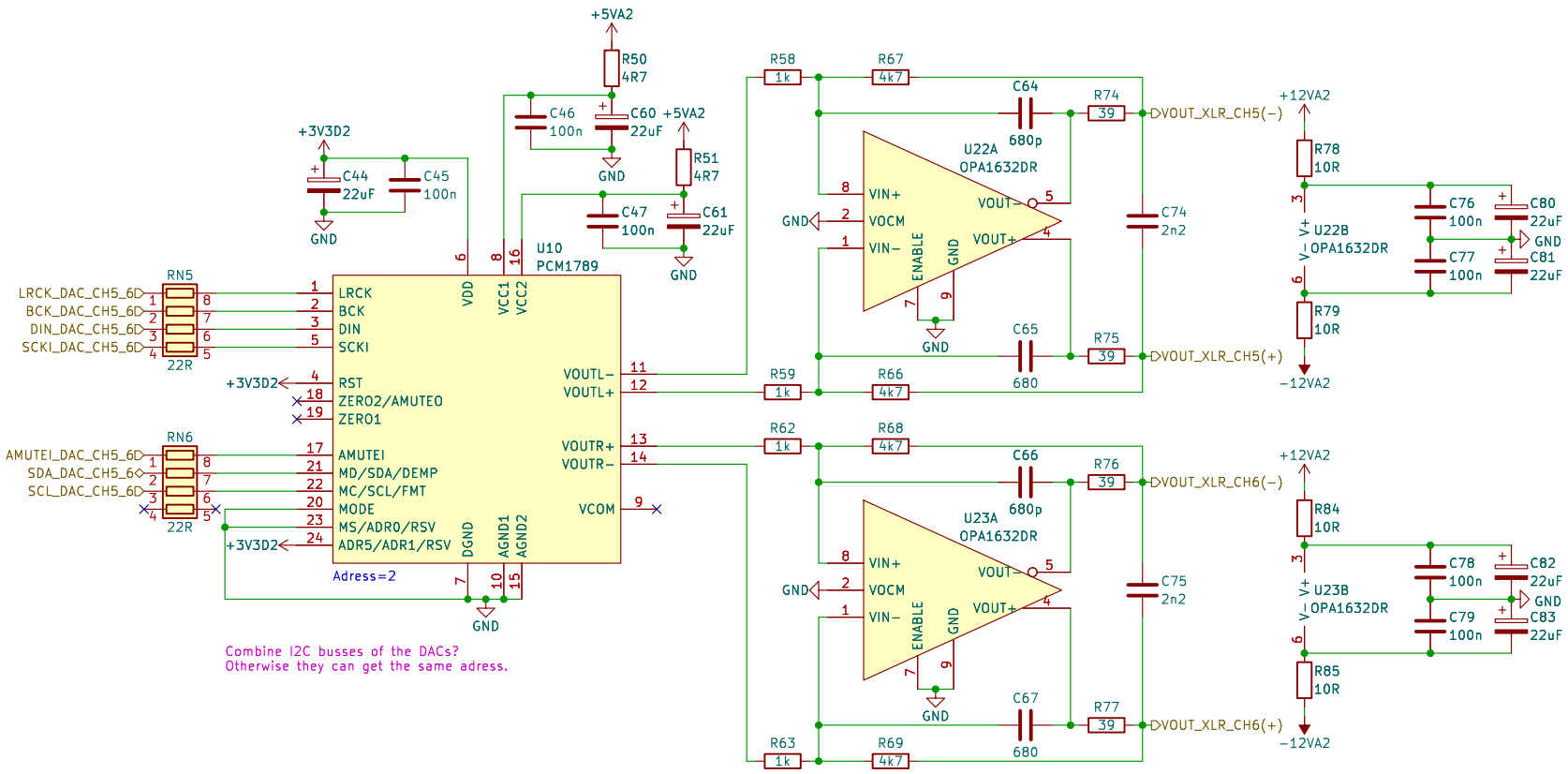

U1
PCM1789
LRCK
BCK
DIN
SCKI
RST
ZERO2/AMUTEO
ZERO1
AMUTEI
MD/SDA/DEMP
MC/SCL/FMT
MODE
MS/ADR0/RSV
ADR5/ADR1/RSV
VDD
VCC1
VCC2
DGND
AGND1
AGND2
VOUTL−
VOUTL+
VOUTR+
VOUTR−
VCOM
Adress=0
RN1
RN2
22R
LRCK_DAC_CH1_2
BCK_DAC_CH1_2
DIN_DAC_CH1_2
SCKI_DAC_CH1_2
AMUTEI_DAC_CH1_2
SDA_DAC_CH1_2
SCL_DAC_CH1_2
+3V3D2
+5VA2
GND
Combine I2C busses of the DACs?
Otherwise they can get the same adress.
U2A
U2B
U2C
U3A
U3B
U4A
U4B
LM4562
OPA1632DR
VIN+
VOCM
VIN−
ENABLE
VOUT−
VOUT+
RCA_JACK_CH1(+)
RCA_JACK_CH1(REF)
RCA_JACK_CH2(+)
RCA_JACK_CH2(REF)
VOUT_XLR_CH1(−)
VOUT_XLR_CH1(+)
VOUT_XLR_CH2(−)
VOUT_XLR_CH2(+)
NetTie_2
Place nettie at output connector
+12VA2
−12VA2
Sheet: /DAC_CH1_2/
File: DAC_CH1_2.kicad_sch
Title: AUDIO−DSP_MAIN_BOARD
Size: User
Date:
Rev: R01
KiCad E.D.A. kicad 7.0.1
Id: 2/8



Sheet: /DAC_CH3_4/
File: DAC_CH3_4.kicad_sch

Title: AUDIO−DSP_MAIN_BOARD

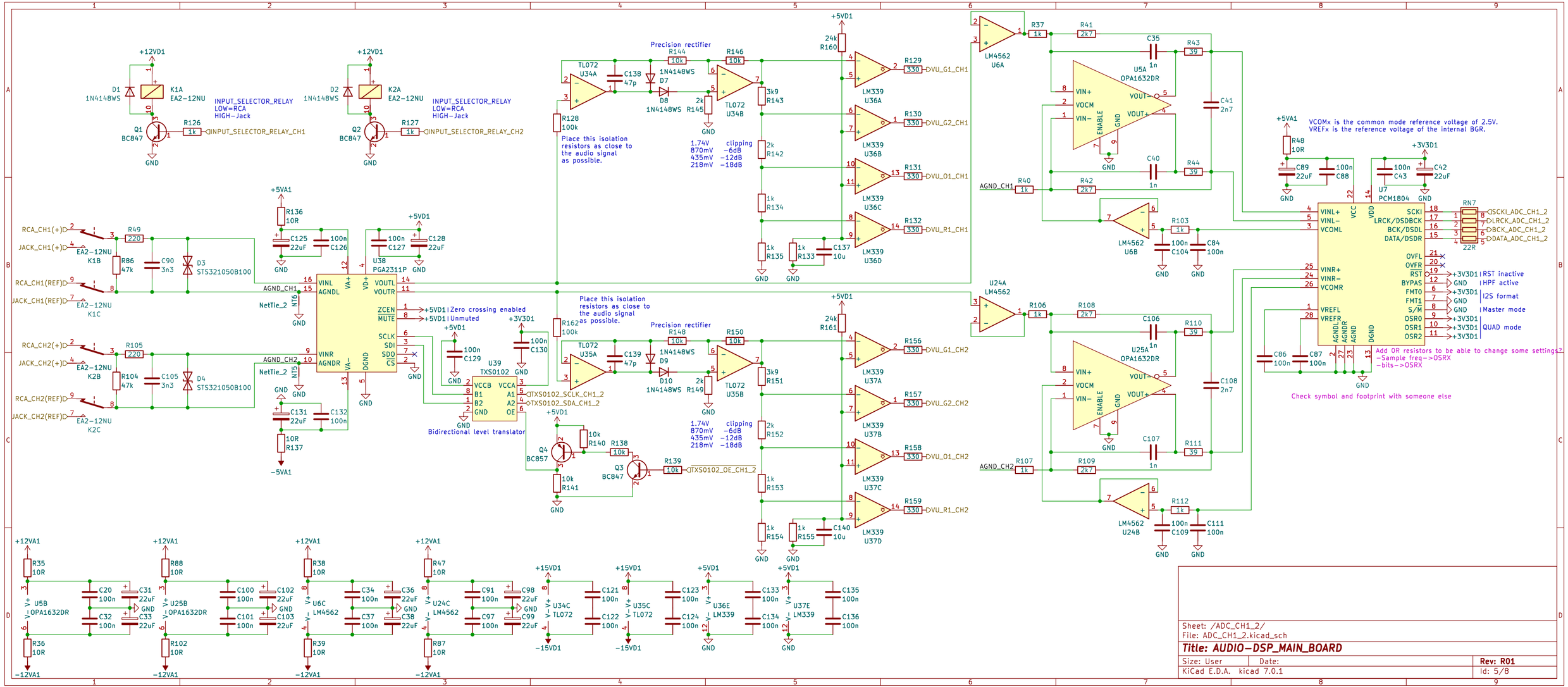
Size: A4	Date:	**Rev: R01**
KiCad E.D.A. kicad 7.0.1		Id: 3/8

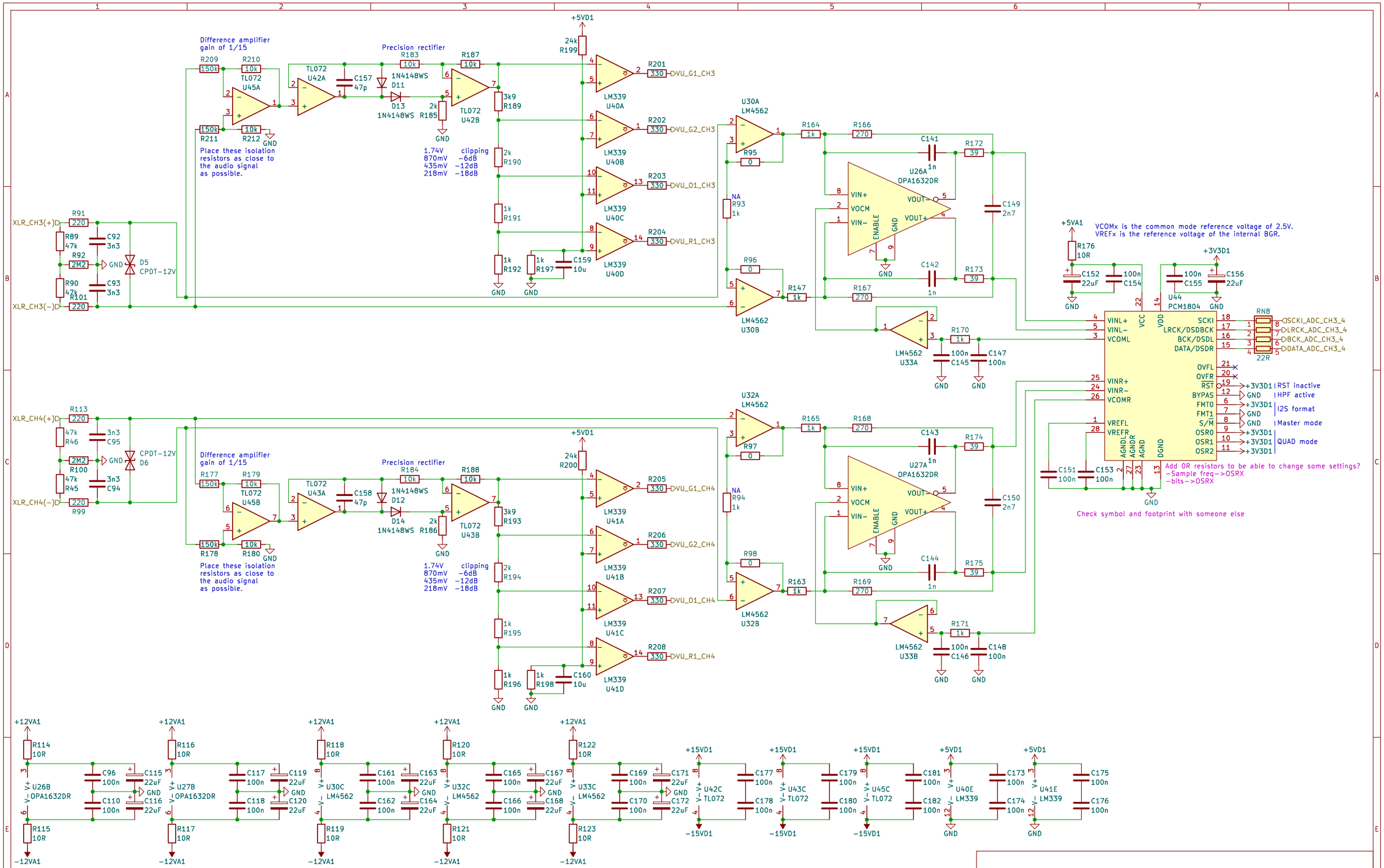


Sheet: /DAC_CH5_6/
File: DAC_CH5_6.kicad_sch

Title: AUDIO−DSP_MAIN_BOARD

Size: A4	Date:	**Rev: R01**
KiCad E.D.A. kicad 7.0.1		Id: 4/8

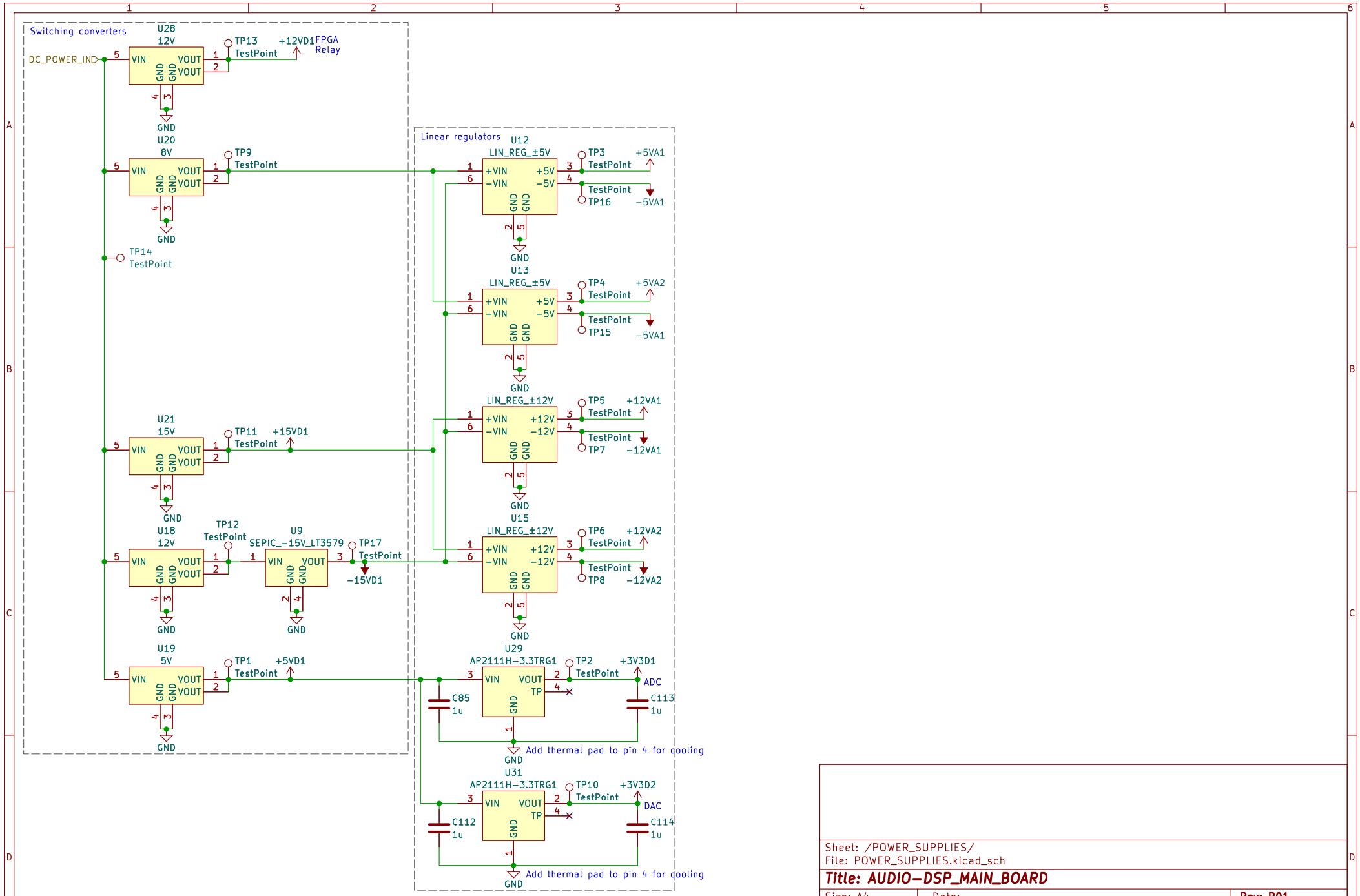

INPUT_SELECTOR_RELAY
LOW=RCA
HIGH=Jack
Precision rectifier
Place this isolation resistors as close to the audio signal as possible.
1.74V 870mV 435mV 218mV
clipping −6dB −12dB −18dB
Zero crossing enabled
Unmuted
Bidirectional level translator
VCOMx is the common mode reference voltage of 2.5V.
VREFx is the reference voltage of the internal BGR.
RST inactive
HPF active
I2S format
Master mode
QUAD mode
Add OR resistors to be able to change some settings
−Sample freq−>OSRX
−bits−>OSRX
Check symbol and footprint with someone else
Sheet: /ADC_CH1_2/
File: ADC_CH1_2.kicad_sch
Title: AUDIO−DSP_MAIN_BOARD
Size: User
Date:
Rev: R01
KiCad E.D.A. kicad 7.0.1
Id: 5/8



Sheet: /ADC_CH3_4/
File: ADC_CH3_4.kicad_sch

Title: AUDIO−DSP_MAIN_BOARD

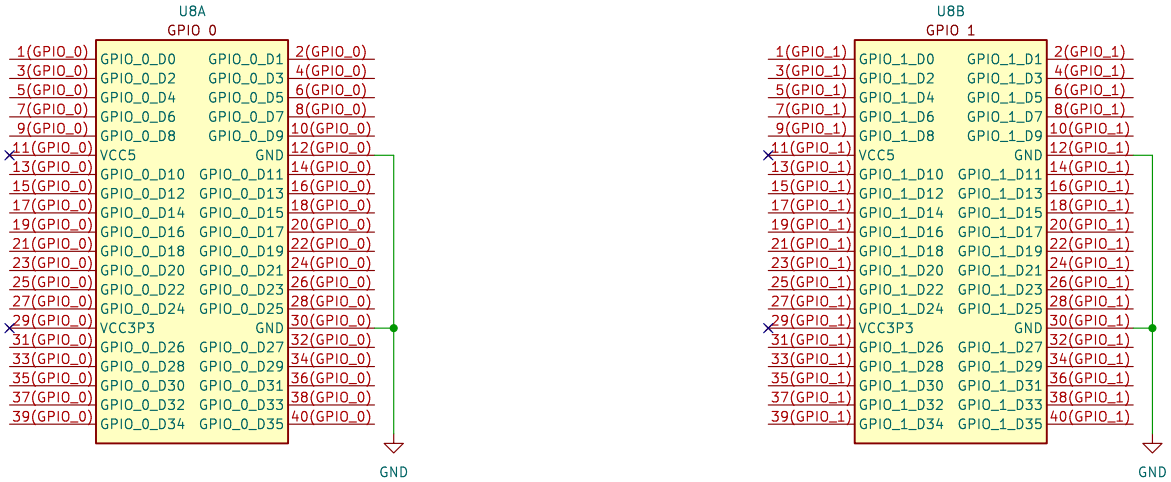
Size: User	Date:	Rev: R01
KiCad E.D.A. kicad 7.0.1		Id: 6/8



Sheet: /POWER_SUPPLIES/
File: POWER_SUPPLIES.kicad_sch

Title: AUDIO-DSP_MAIN_BOARD

Size: A4	Date:	Rev: R01
KiCad E.D.A. kicad 7.0.1		Id: 7/8



DAC_CH1_CH2
- SCKI_DAC_CH1_2
- DIN_DAC_CH1_2
- LRCK_DAC_CH1_2
- BCK_DAC_CH1_2
- AMUTEI_DAC_CH1_2
- SDA_DAC_CH1_2
- SCL_DAC_CH1_2

DAC_CH3_CH4
- SCKI_DAC_CH3_4
- DIN_DAC_CH3_4
- LRCK_DAC_CH3_4
- BCK_DAC_CH3_4
- AMUTEI_DAC_CH3_4
- SDA_DAC_CH3_4
- SCL_DAC_CH3_4

DAC_CH5_CH6
- SCKI_DAC_CH5_6
- DIN_DAC_CH5_6
- LRCK_DAC_CH5_6
- BCK_DAC_CH5_6
- AMUTEI_DAC_CH5_6
- SDA_DAC_CH5_6
- SCL_DAC_CH5_6

UI
- UI_RX
- UI_TX

- INPUT_SELECTOR_RELAY_CH1
- INPUT_SELECTOR_RELAY_CH2

- TXS0102_SCLK_CH1_2
- TXS0102_SDA_CH1_2
- TXS0102_OE_CH1_2

- SCKI_ADC_CH1_2
- LRCK_ADC_CH1_2
- BCK_ADC_CH1_2
- DATA_ADC_CH1_2

- SCKI_ADC_CH3_4
- LRCK_ADC_CH3_4
- BCK_ADC_CH3_4
- DATA_ADC_CH3_4

I will make these last connections as soon as the PCB design is a bit further.
Because of the flexibility of the FPGA, the PCB design can be made easier by
choosing these connections wisely.

USB port of DE1-SOC board can be used as USB audio input.

-Checken of deze pin assignment mogelijk is dmv een test programma?
-Checken hoe erg de crosstalk aanwezig is dmv een test programma?

Sheet: /FPGA/
File: FPGA.kicad_sch

Title: AUDIO-DSP_MAIN_BOARD

Size: A4	Date:	**Rev: R01**
KiCad E.D.A. kicad 7.0.1		Id: 8/8