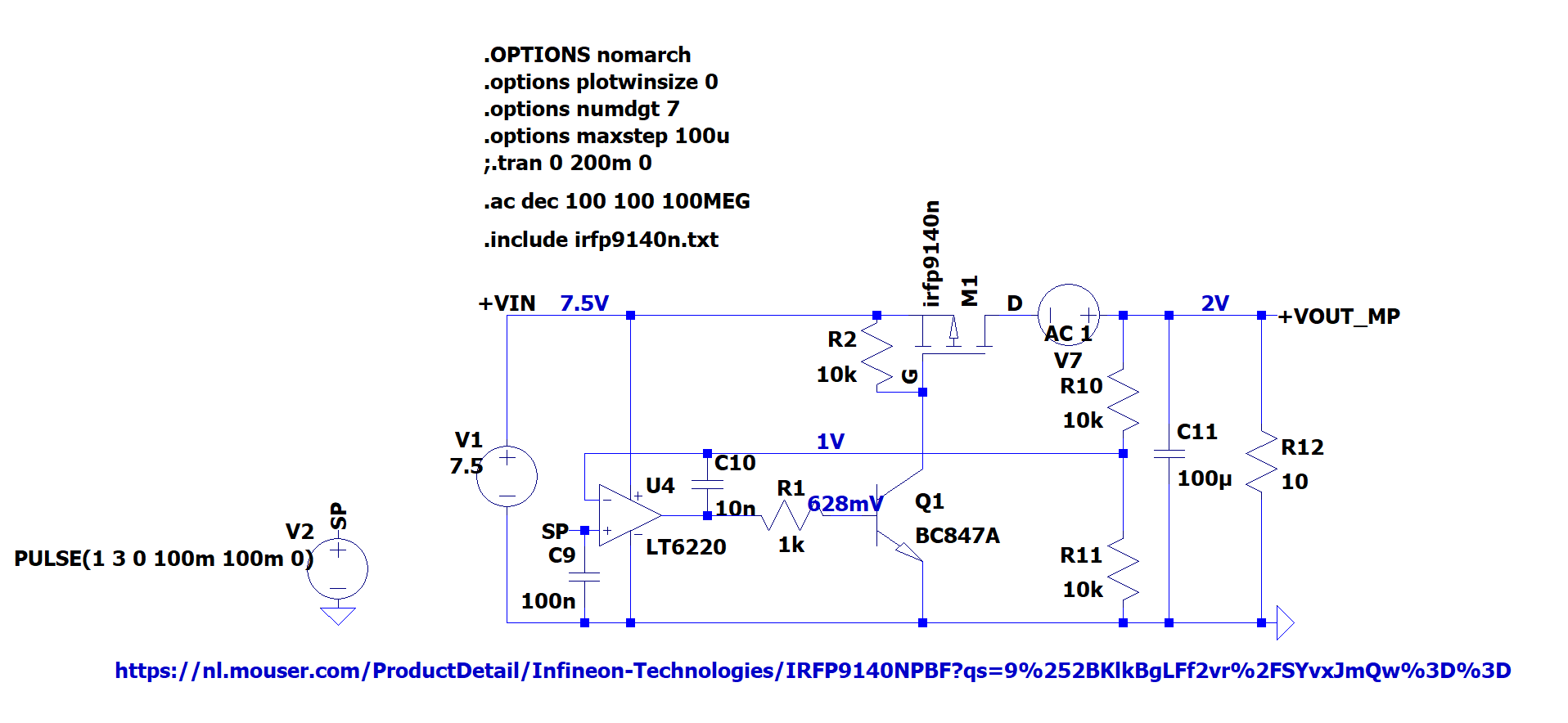
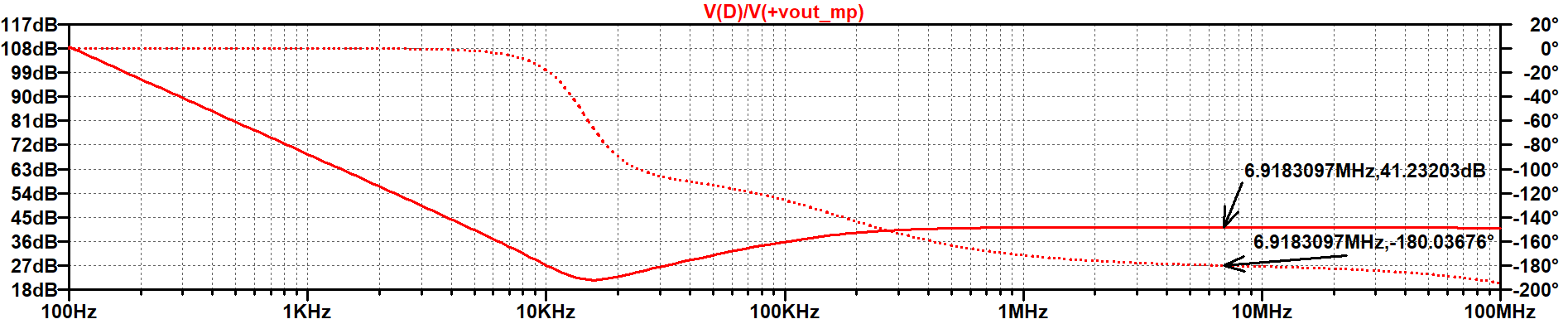
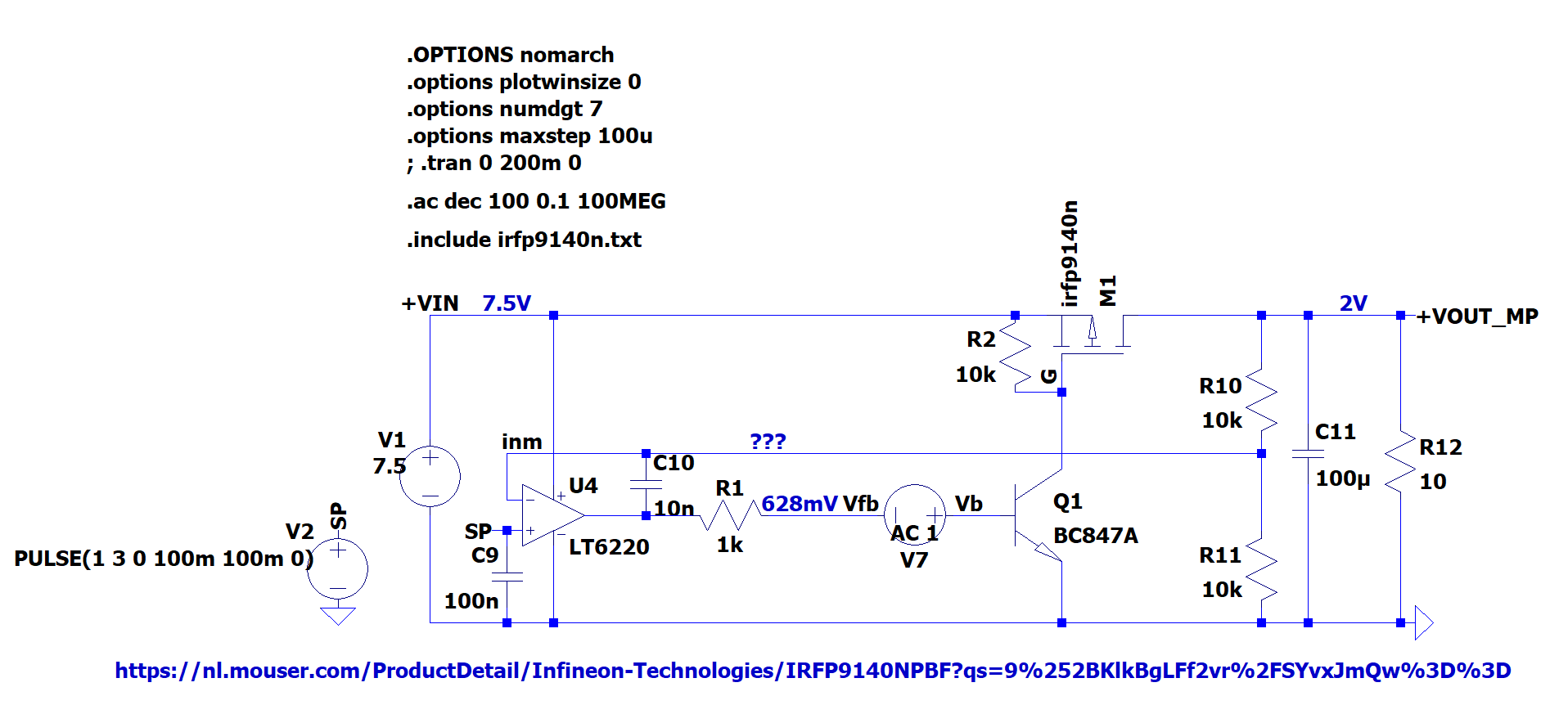
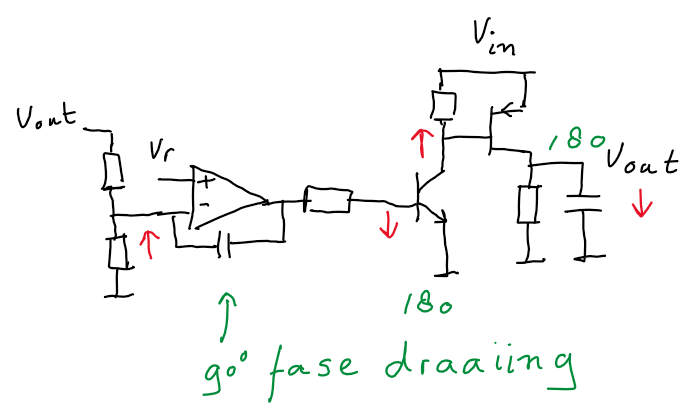
V1:

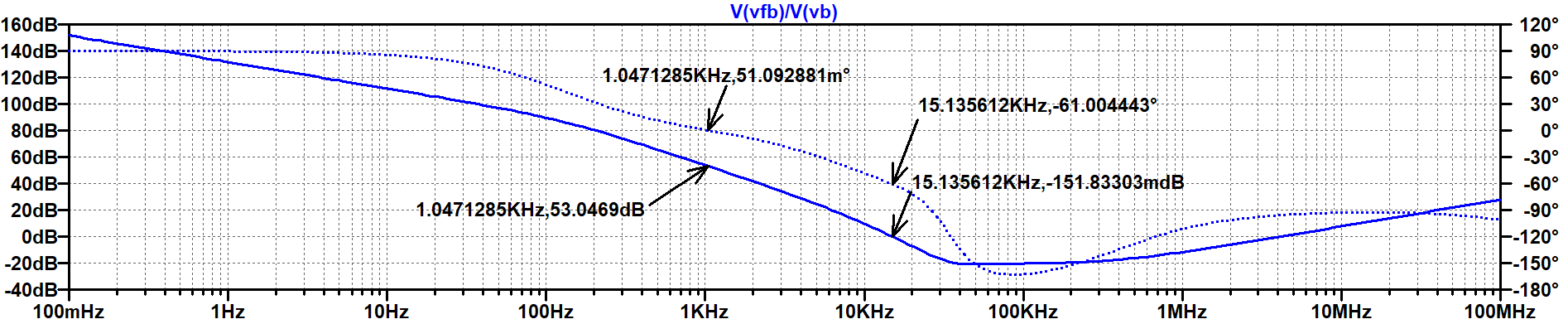




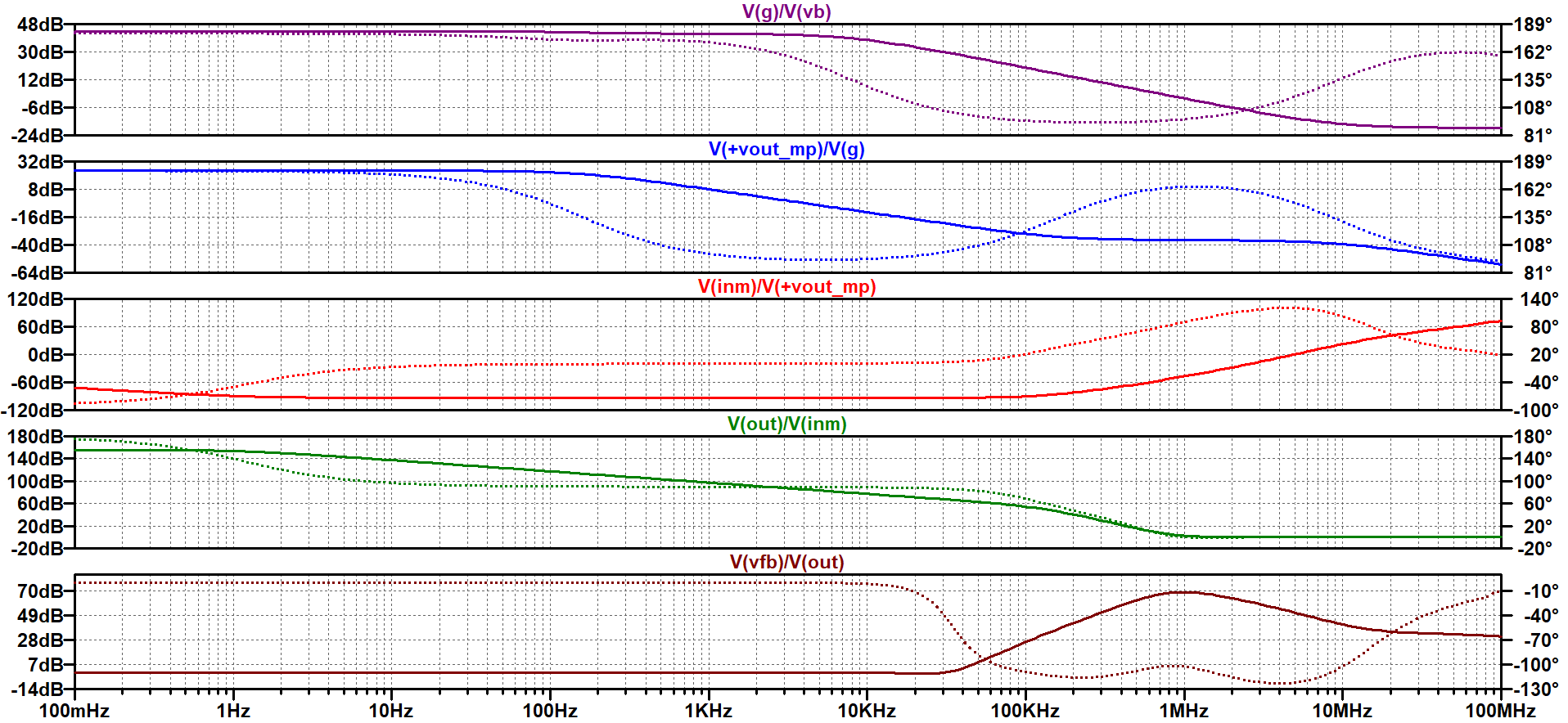
V2:







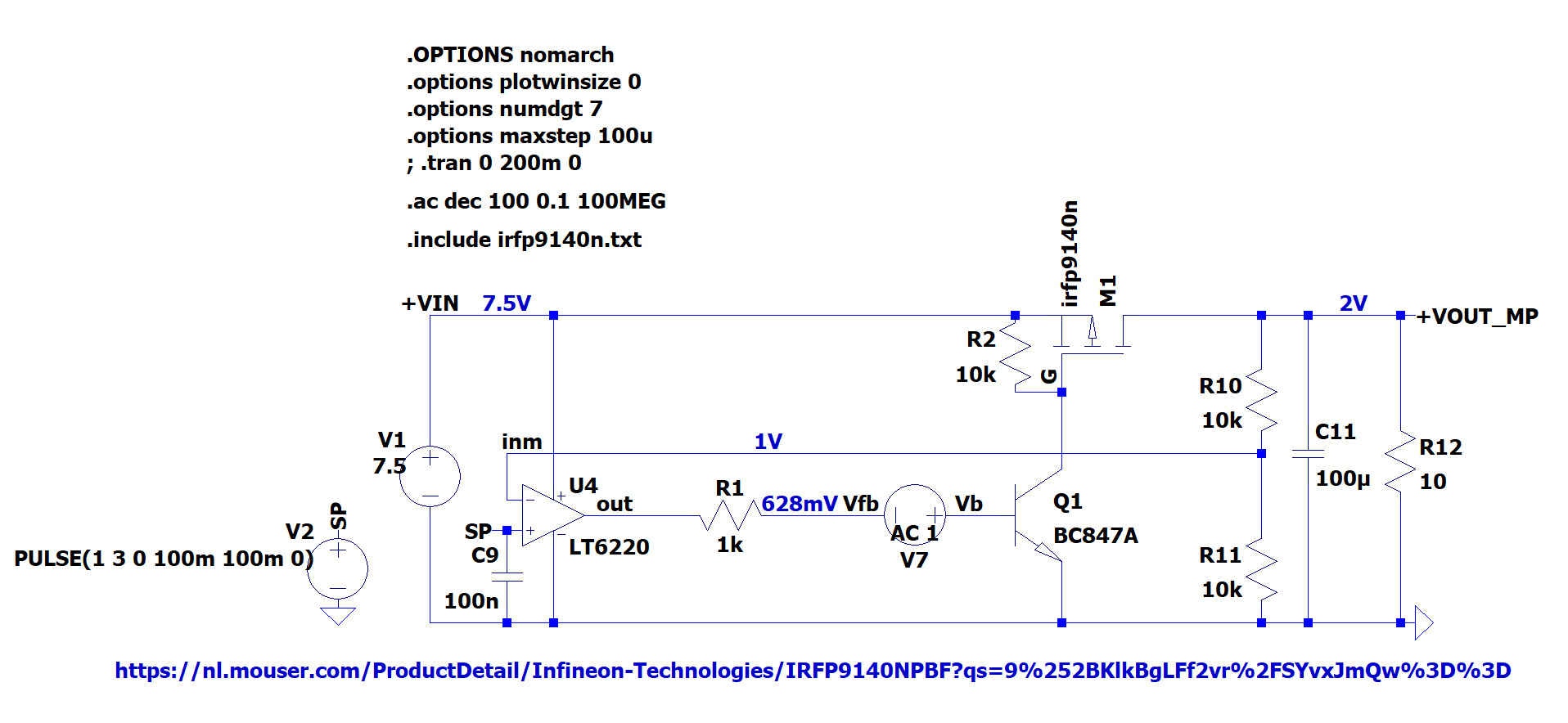
Verschillende tussen overdrachten:

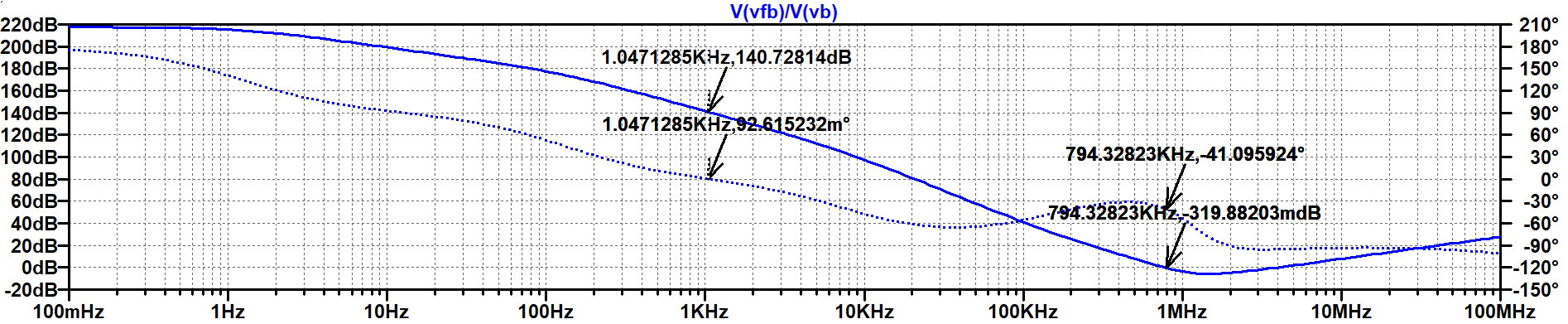


V(out)/V(inm) is dominant, daarna V(+vout\_mp)/V(g) en vervolgens V(g)/V(vb).

3e orde, te veel fase draaiing.

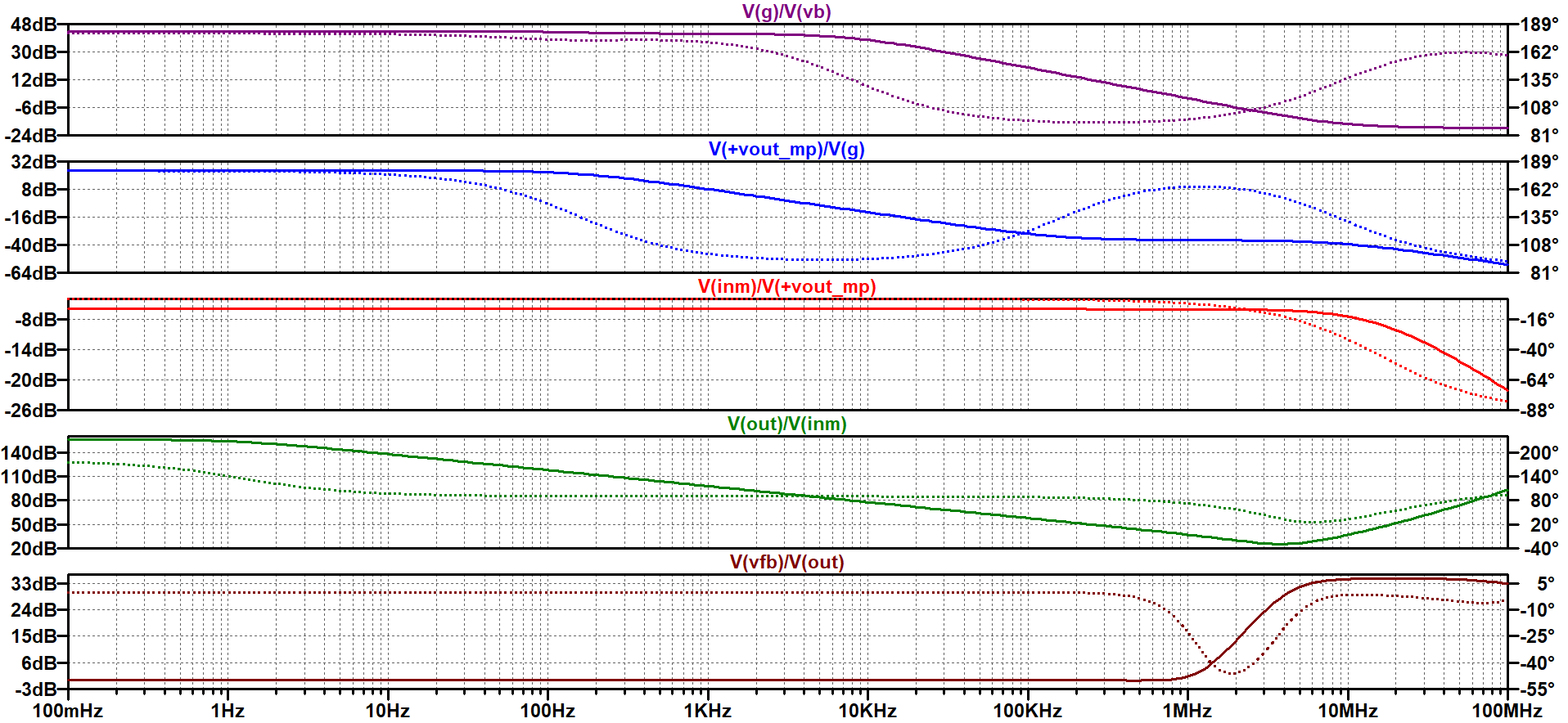
V3: Zonder C10





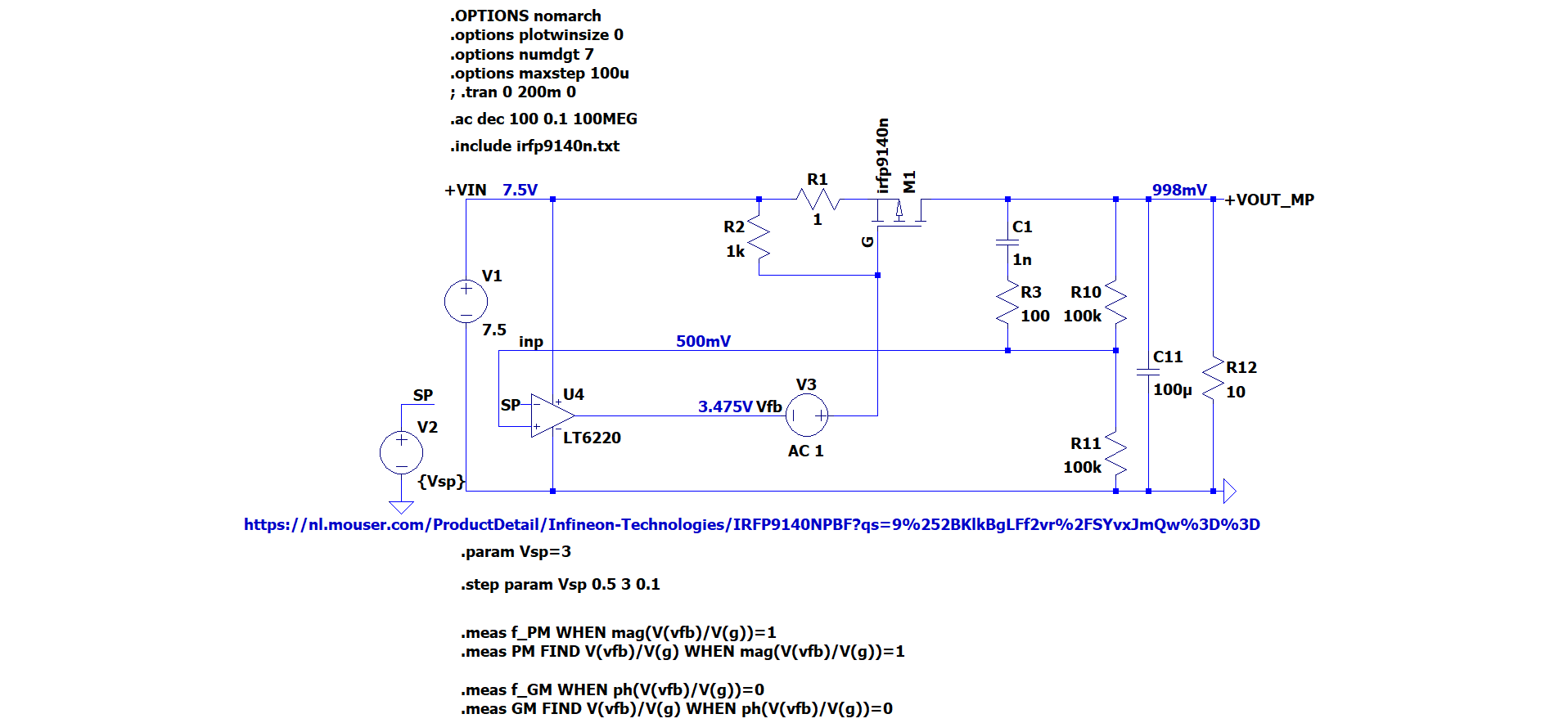
Te veel loopgain.

Verschillende tussen overdrachten:

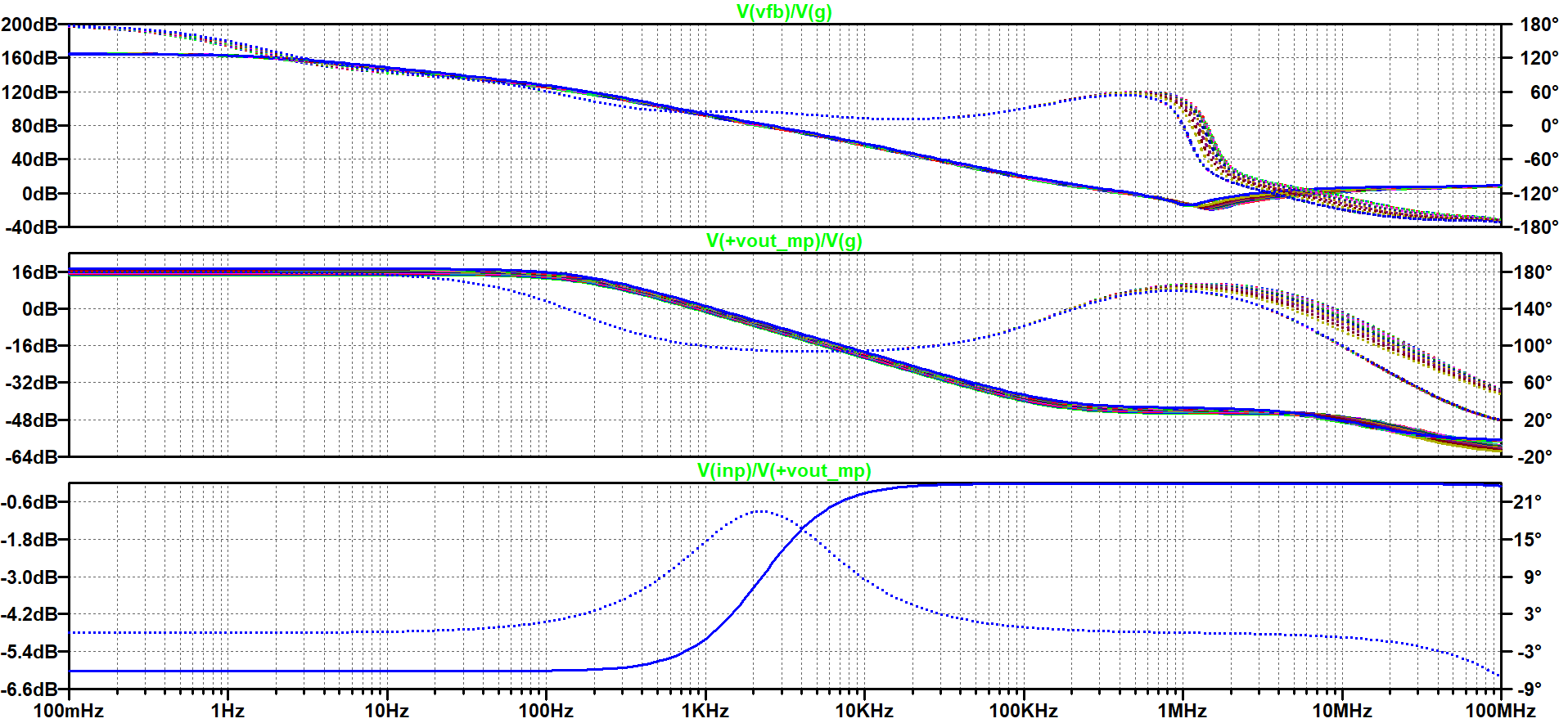


V4:

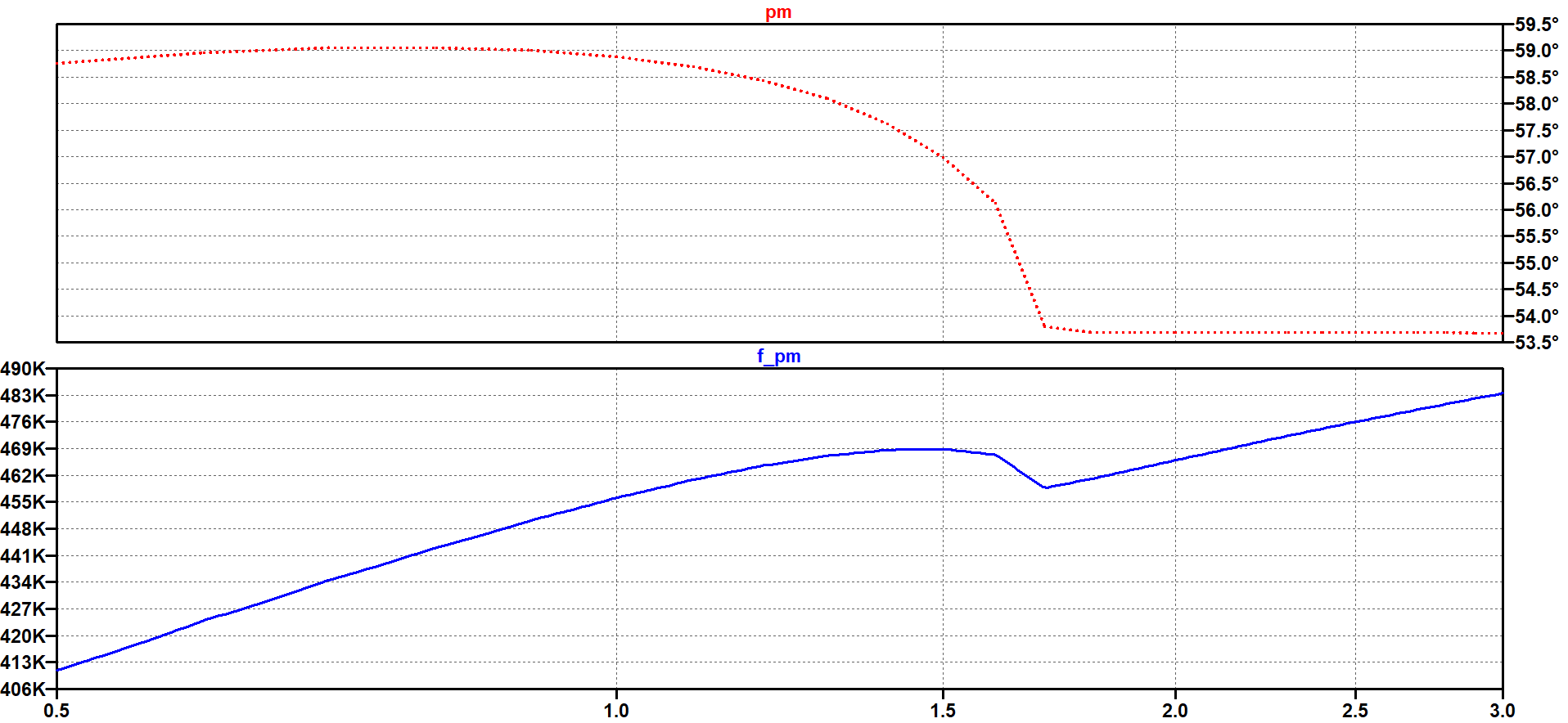
Transistor verwijderd.



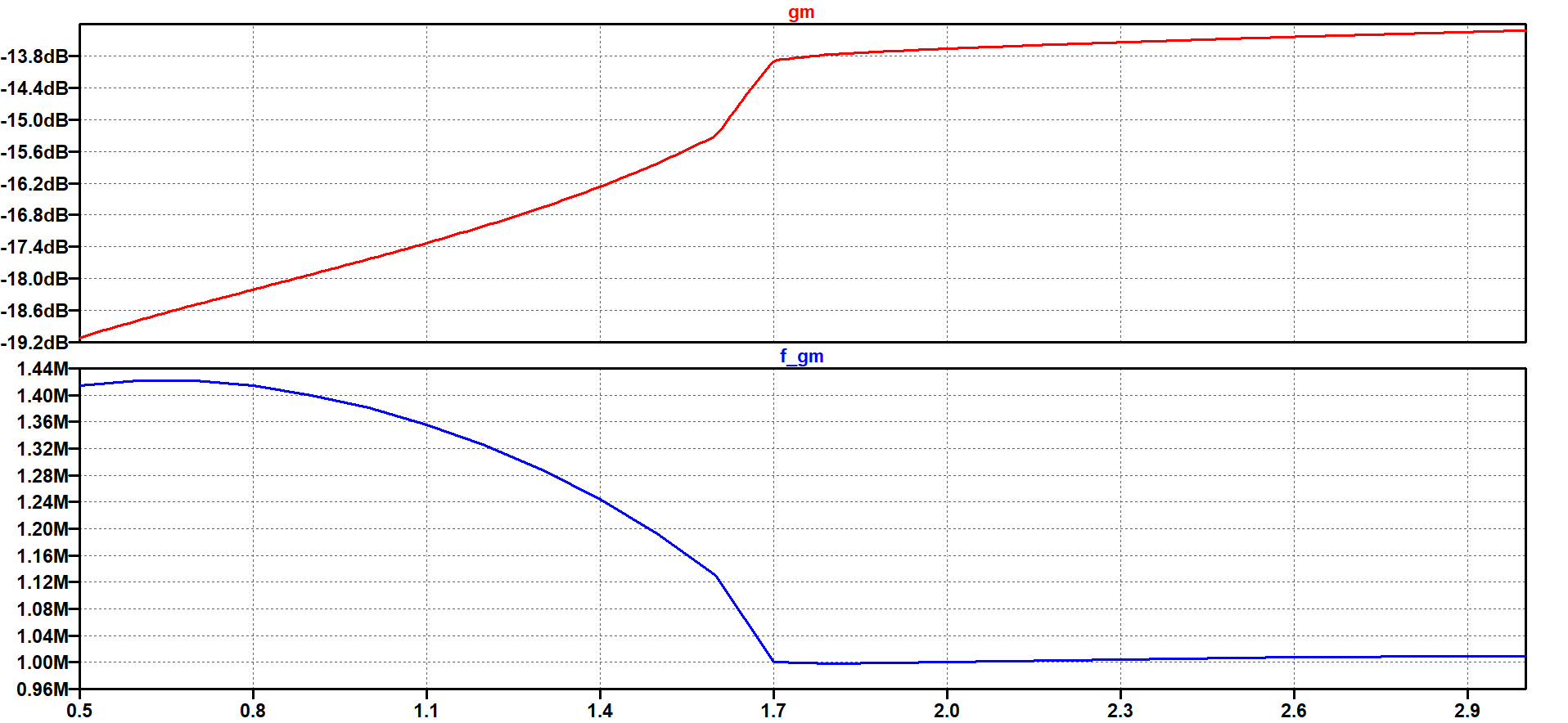
Figuur : Stabiliteitsanalyse met variërend set-point (0.5 – 3V)



Figuur : Simulatie resultaat van setup weergegeven in Figuur 1

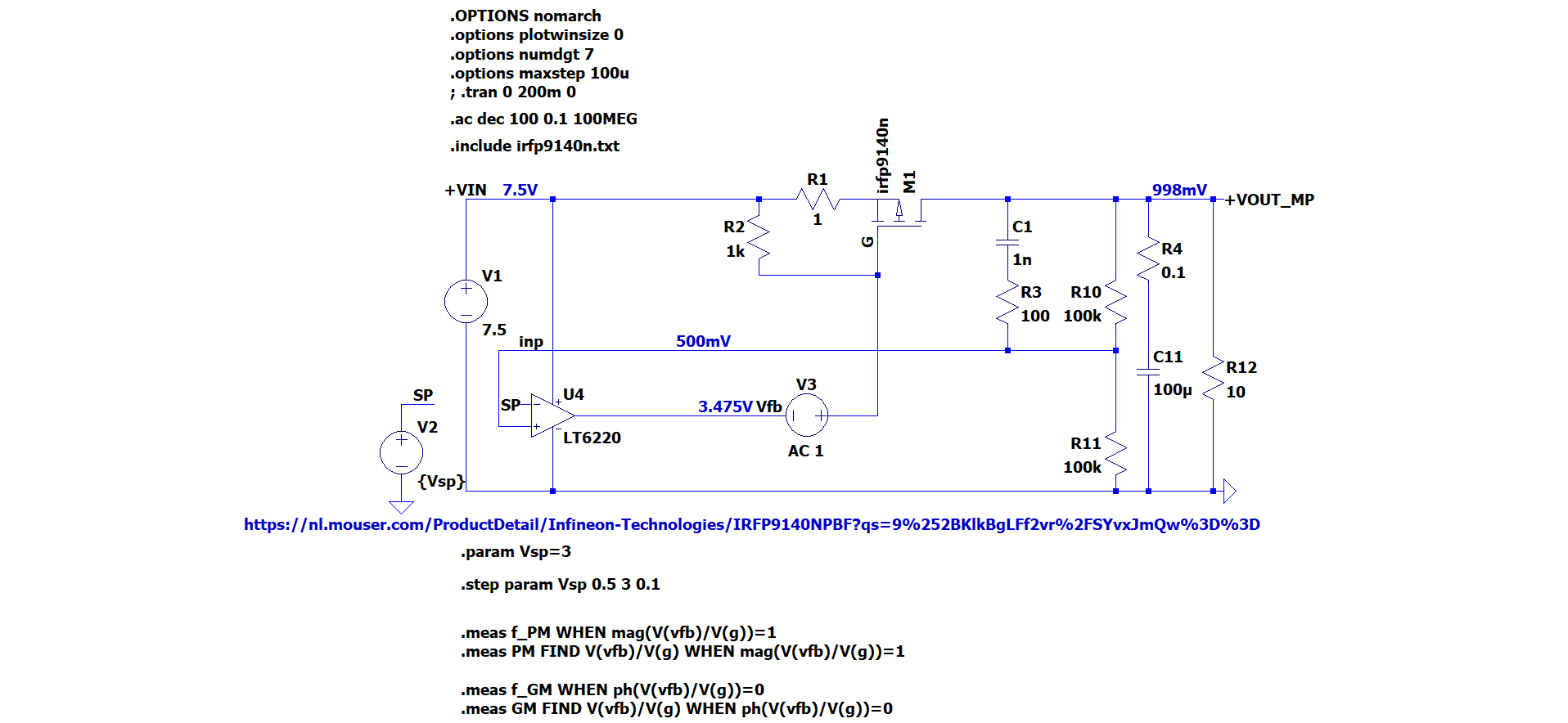


Figuur : Fase marge en bijbehorende frequentie

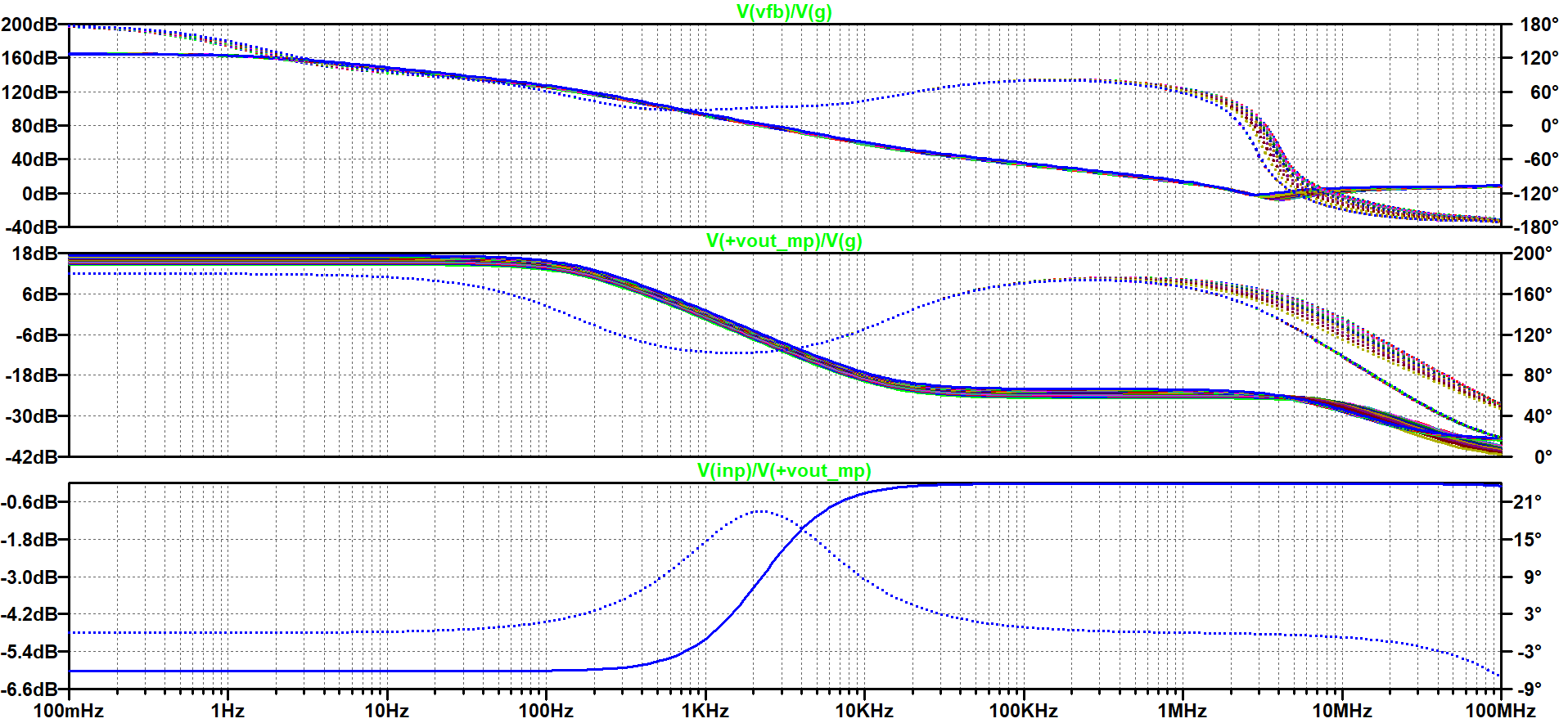


Figuur : Versterkings marge en bijbehorende frequentie

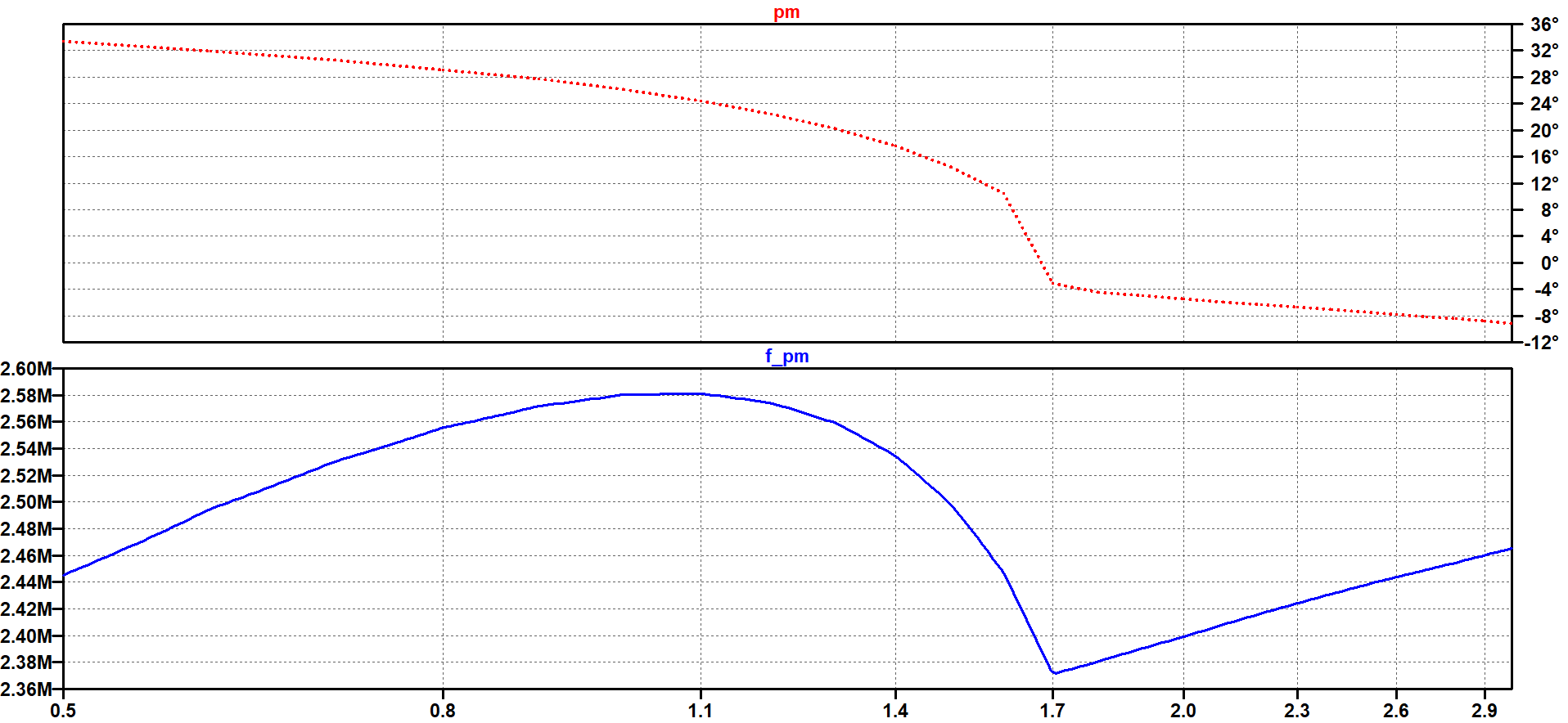
Invloed van ESR.



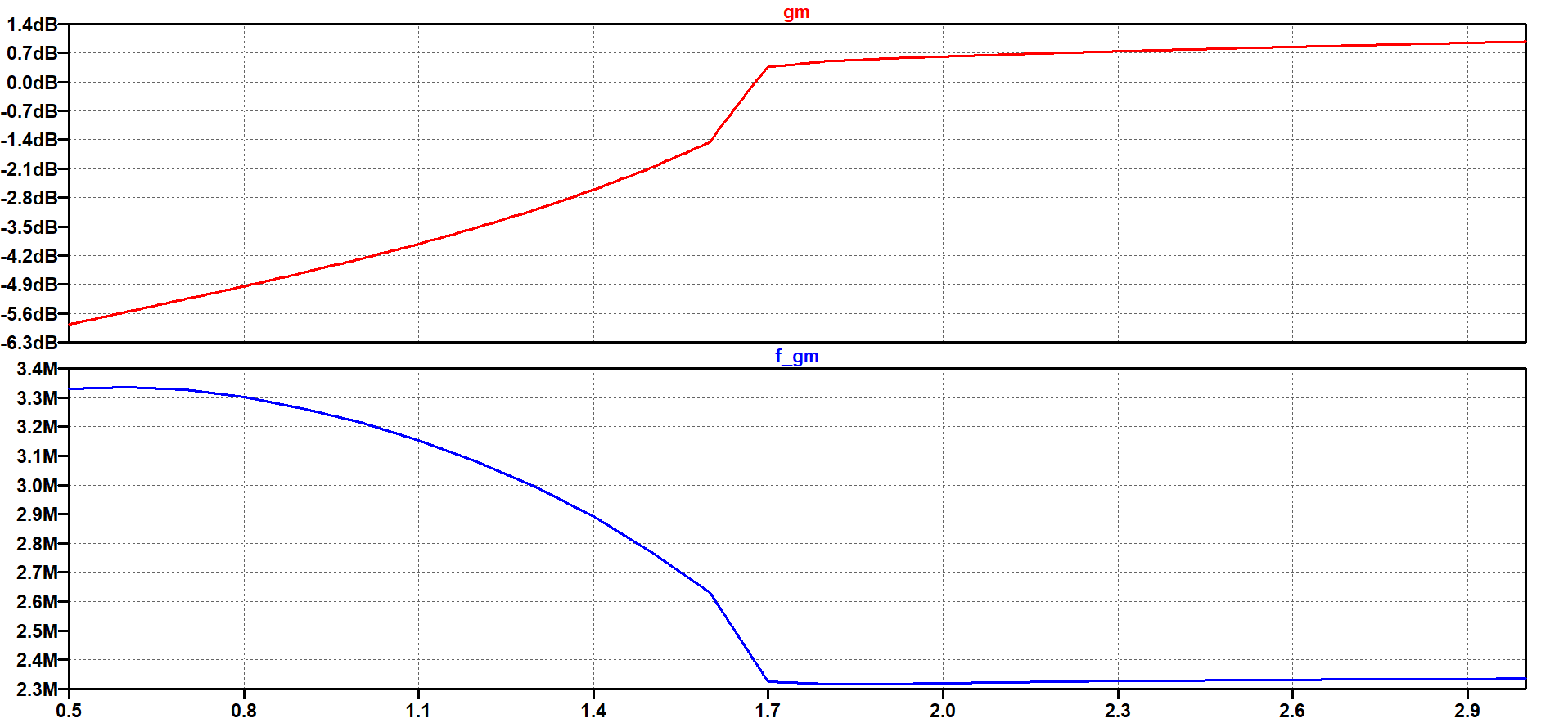
Figuur 5: Stabiliteitsanalyse met ERS en variërend set-point (0.5 – 3V)



Figuur 6: Simulatie resultaat van setup weergegeven in Figuur 5



Figuur 7: Fase marge en bijbehorende frequentie



Figuur 8: Versterkings marge en bijbehorende frequentie