```
module ALU (A,B,OUT,control);
 input [1:0] A,B;
 input [2:0] control;
 output [3:0] OUT;
 reg [1:0] INI;
 reg [3:0] hold;

 integer i;

 always @(A,B,control)begin
  hold = 0;
 case (control)
 0: hold = A+B;
 1: begin
 if (B > A)begin
 hold = 0; end
 else begin hold = A-B; end
 end
 2: begin
   INI = A;
 for (i = 0; i<B; i = i + 1) begin
 hold = hold + INI;
 end
 end
 3: begin
 INI = A;

 for (i = 0; i < 4; i = i + 1) begin
 if (INI >= B) begin
 INI = INI - B;
 hold = hold+1; end
 end
 end

 4: hold = ~A;
 5: hold = A|B;
 6: hold = A&B;
 7: hold = A^B;
endcase
 end
 assign OUT = hold;
endmodule
```

```
module ALU_test();
```

```
reg [1:0] A,B;
reg [2:0] control;
wire [3:0] OUT;
ALU T (A,B,OUT,control);
initial begin
  A= 0;
  B = 0;
  control = 0;
end
initial begin
  #5 control = 0; A = 2; B = 3;
  #5 control = 1; A = 3; B = 3;
  #5 control = 2; A = 2; B = 3;
  #5 control = 3; A = 3; B = 3;
  #5 control = 3; A = 3; B = 2;
  #5 control = 3; A = 2; B = 3;
  #5 control = 4; A = 2; B = 0;
  #5 control = 5; A = 0; B = 2;
  #5 control = 6; A = 2; B = 2;
  #5 control = 6; A = 0; B = 2;
  #5 control = 6; A = 0; B = 0;
  #5 control = 7; A = 2; B = 2;
  #5 control = 7; A = 2; B = 1;
  #5 control = 7; A = 0; B = 2;
 end
endmodule
```