1. [3 pts] Develop a Verilog module for a 4-bit synchronous binary counter. The counter should have an asynchronous reset input signal that resets the counter to zero when set to 1.
2. [2 pts] Update the module of Q1 such that the counter has a synchronous enable input signal. When the enable is set to 1 the counter should be counting normally, and otherwise the counter holds its old value.
3. [1 pts] Develop a Verilog module for a 4-bit Binary-coded decimal (BCD) to 7-segment display decoder.
4. [2 pts] [Research Q] What does a clock divider module do?
5. [2 pts] [Research Q] How is it possible to display 4 different digits on the 4-digit 7-segment display that has common cathodes?

4) A clock divider module takes an input clock signal and produces an output clock signal at a lower frequency, dividing the input clock frequency by a factor.

5) It is possible to display 4 different digits on the 7-segment display by using multiplexing. This involves connecting the cathodes of all the segments across the four digits together and then controlling the anodes of each segment individually. A microcontroller cycles through each digit by setting the correct combination of segments for the desired number and turning on the corresponding anode while the others remain off. It then looks like the 4 digits are visible simultaneously.