Lab 2
Logic Gates Characteristics

1. Objectives

- Measure the propagation delay of CMOS logic gates
- Measure V_{IL} and V_{IH} of CMOS logic gates
- Introduce the Analog Discovery Kit and its usage in testing logic circuits made out of CMOS chips

2. Material

- 74HC00 (Quad 2-input NAND)
- 74HC08 (Quad 2-input AND)
- Analog Discovery Kit
- Digital Logic Trainer
- Wires

3. Introduction

a. The physical characteristics of logic gates

The physical characteristics of logic gates often play an important role in the design of digital circuits. These include:

- Voltage and current levels
- Noise margin
- Fan-out and loading
- Propagation delay
- Threshold Voltage

Some of these physical characteristics are discussed below.

i. Current Direction:

According to IEEE standards, currents are directed into devices. Therefore, if a current in a specification is positive, it is entering the device. If a current in a specification if negative, it is leaving the device.

ii. Propagation Delay

Propagation delay is the time that it takes a gate to switch logic levels. Logic gates often have a different propagation delay switching from LOW to HIGH than from HIGH to LOW, so two types of delay are defined:

t_{PLH} = propagation delay when the OUTPUT switches from LOW to HIGH calculated at 50% of input-output transition, i.e. maximum time from the input change crossing 50% to the output LOW to HIGH change crossing 50%.

t_{PHL} = propagation delay when the OUTPUT switches from HIGH to LOW calculated at 50% of input-output transition, i.e. maximum time from the input change crossing 50% to the output HIGH to LOW change crossing 50%.

Figure 1 demonstrates propagation delay. The average propagation delay tp = ½ (t_{PLH} + t_{PHL}).

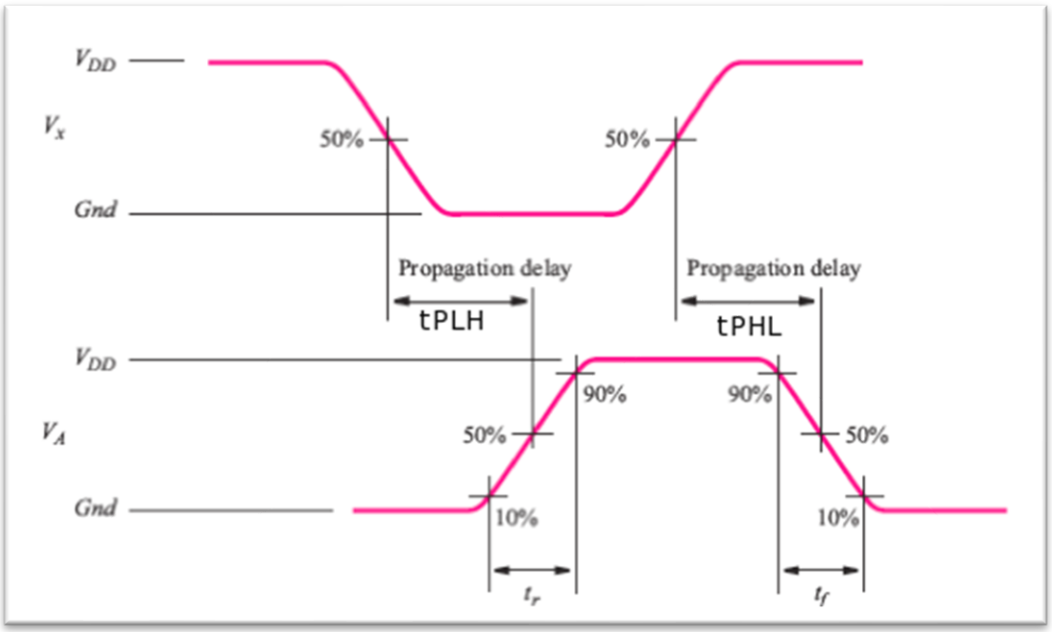


Figure 1. Propagation Delay calculation

iii. Voltage and Current Levels:

Several voltage and current levels are of interest when working with logic gates, including:

- V_{OL} = Low-level output voltage (output voltage when the output of the gate is logic 0)
- V_{OH} = High-level output voltage (output voltage when the output of the gate is logic 1)
- V_{IL} = Low-Level input voltage
- V_{IH} = High-level input voltage
- I_{OL} = Low-level output current
- I_{OH} = High-level output current
- I_{IL} = Low-level input current
- I_{IH} = High-level input current

iv. Noise Margins

Noise margin is a quantitative measure of noise immunity offered by a logic family. Noise margin allows you to determine the allowable noise voltage on the input of a gate so that the output will not be corrupted. The specification most commonly used to describe noise margin (or noise immunity) uses two parameters: the logic low noise margin, ***NM_L***, and the logic high noise margin, ***NM_H***.

With reference to Figure 2, NM_L is the difference in maximum LOW input voltage recognized by the receiving gate and the maximum LOW output voltage produced by the driving gate.

Thus, **NM_L = LOW level noise margin = V_{IL}(max) – V_{OL}(max)**

Where V_{IL}(max) is the maximum LOW input voltage and V_{OL}(max) is the maximum LOW output voltage.

This implies that, when the LOW voltage output of one device feeds the input of another, there is an available margin of NM_L. That is, any positive voltage spikes of amplitude less than or equal to NM_L on the signal line do not cause any spurious transitions.

Also the value of NM_H is the difference between the minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognized by the receiving gate.

Thus, **NM_H = HIGH level noise margin = V_{OH}(min) – V_{IH}(min)**

Where V_{IH}(min) is the minimum HIGH input voltage and V_{OH}(min) is the minimum HIGH output voltage.

This implies that, when the HIGH voltage output of one device feeds the input of another, there is an available margin of NM_H. That is, any negative voltage spikes of amplitude less than or equal to NM_H on the signal line do not cause any spurious transitions.

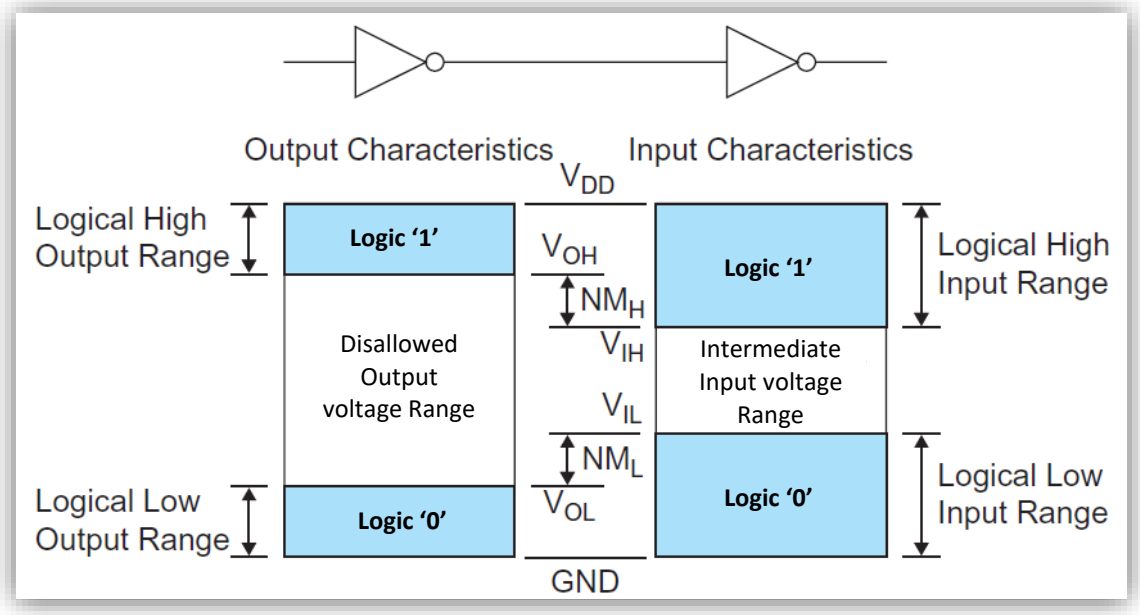


Figure 2. CMOS High and Low Noise Margins definitions

As seen in Figure 2, V_{OL} (max) is lower than V_{IL} (max) to allow for noise and signal deterioration. Similarly, V_{OH} (min) is higher than V_{IH} (min). These differences in voltages are those referred to as noise margins. If either NM_L or NM_H for a gate are too small, the gate may be disturbed by noise that occurs on the inputs. Typically, in a CMOS inverter V_{OH} will equal V_{DD} and V_{OL} will equal the ground potential. In practice, noise margins are the amount of noise that a logic circuit can withstand. Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or outright failure.

Inputs between V_{IL} and V_{IH} are said to be in the indeterminate region or forbidden zone and do not represent legal digital logic levels. Therefore, it is generally desirable to have V_{IH} as close as possible to V_{IL}.

b. Analog Discovery Kit

The Digilent Analog Discovery is a multi-function instrument that can measure, record and generate analog and digital signals. The small, portable and low-cost Analog Discovery was created so that engineering students could work with analog and digital circuits anytime, anywhere - right from their PC.

The Analog Discovery Kit (shown in Figure 3) provides all capabilities necessary for test and measurement of circuits. It provides the ability to apply voltages (signals) to a circuit or device and measure the response. The Analog Discovery combines a dual-channel oscilloscope, a two-channel waveform generator, a 16-channel logic analyzer and many other instruments into a USB-powered, low-cost device. The Analog Discovery works with the **Waveforms** software that offers intuitive interfaces to the oscilloscope, waveform generator, etc.

The Analog discovery kit will be used in different lab experiments to generate digital signals and observe the waveforms generated from logic circuits. The connector has the following pins (as shown in Figure 3):

- **V+ & V-**: Fixed power supplies (+5 V (+50 mA) and -5 V (+50 mA))
- **W1 & W2**: variable power supplies (Wave function generator)
- **1+,1- ,2+ & 2-**: Two channel voltage measurement (oscilloscope)
- **0 to 15**: Digital input output (I/O) (D0, D1, …., D15)
- ↓: Ground

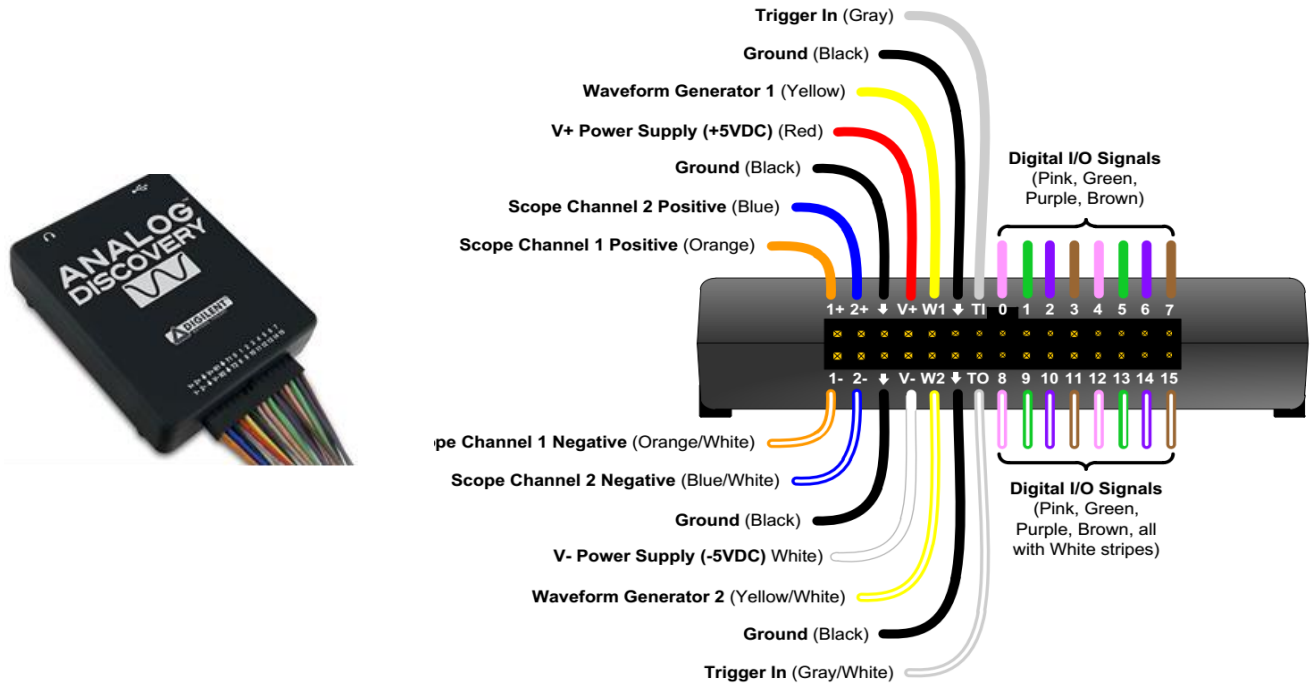


Figure 3. The Analog Discovery Kit and its pin-out

4. Pre-lab Questions

Use Logisim software to connect the circuit shown in Figure 4 using pin-to-pin diagram. Use the proper chips from the 7400 lib. DO NOT USE individual gates. Provide a screenshot of the circuit on Logisim along with the .circ file.

5. Experiments

1. Measuring the Propagation Delay at 5V input supply:

a. Connect the circuit as shown in Figure 4. Connect pin 14 to +5V from the power supply area on the logic trainer and connect the pin 7 to 'GND'.

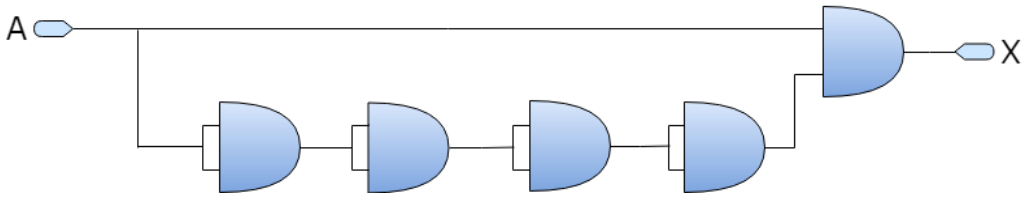
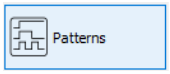


Figure 4. A simple circuit

b. Connect the Analog discovery pins 'D0' & 'D1' to 'A' and 'X' respectively. Also, connect the Analog discovery pin ↓ to your circuit ground to create a common ground.

c. Open the **WaveForms** software (C:\Program Files (x86)\Digilent\WaveForms3)

d. Apply a square wave to 'A' with "**Pattern Generator**" 

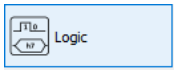
instrument:

i. Add → Signal → select DIO 0, as shown in Figure 5

ii. Change the signal parameters as follows
- Type: Clock
- Output: PP
- Parameter1: 5MHz

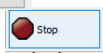
iii. Press 

to start generating the signal

e. View the 'A' and 'X' signals using the '**Logic Analyzer**' 

instrument :

i. Change the parameters as follows
- Base: 500 ns/div
- Press 'Run' 

ii. After a few seconds press 

Double click to enable the hot track to be able to measure data from signals. Click on the point where you want to start recording and click again to finish recording.

iii. Use the track to record the propagation delays as shown in Figure 6

f. Record the values in Table 1 in the Lab Report.

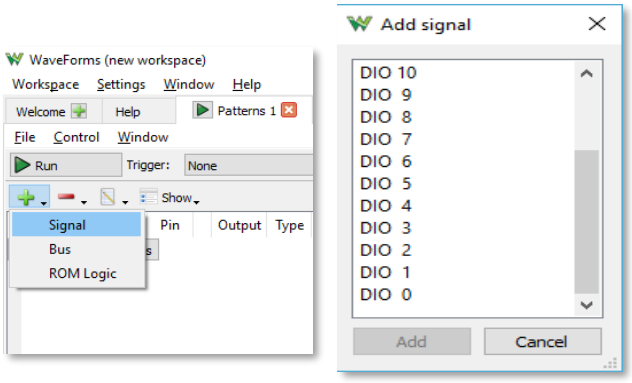


Figure 5. Adding a signal in WaveForms Digital Input mode

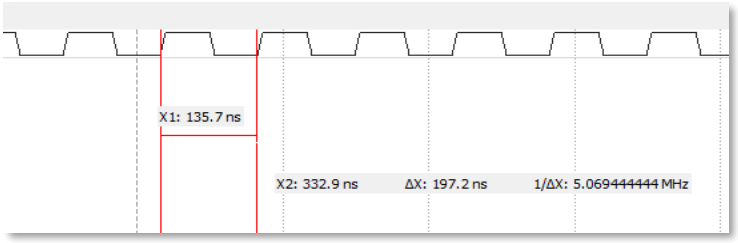


Figure 6. Zooming hot tracks in WaveForms

2. Measuring V_{IL_max} and V_{IH_min}:

a. Connect the circuit as shown in Figure 7, and select a good V_{cc} value as in the datasheet.

b. Set the potentiometer knob initially to 0V.

c. Use the "**Voltmeter**" instrument of the Analog Discovery to measure the signals at B & X; connect '1+' to B, '2+' to X, '1-' and '2-' to your circuit ground.

d. Turn the knob gradually to increase the input voltage while monitoring the voltage on X. Keep doing that till the voltage at X is greater than V_{OH_min} (check the datasheet).

e. Record V_{IH_min} = _____

f. Set the potentiometer knob to 5V.

g. Turn the knob gradually to decrease the input voltage while monitoring the voltage on X. Keep doing this till the voltage on X is less than V_{OL_max} (check the datasheet).

h. Record V_{IL_max} = _____

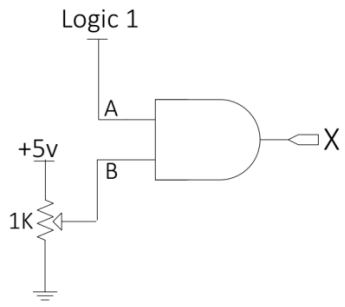


Figure 7. A simple circuit

6. Lab Report [10 Pts]

(Deadline: Tuesday of next week 2:00pm) (Individual submission)

1. [1.5 Pts] Record the values obtained in Experiment question 1 in Table 1 below.

Table 1

Propagation delay (t_{P_LH})	
Propagation delay (t_{P_HL})	
Average propagation delay t_p	
Propagation delay (t_{P_LH}) per gate	
Propagation delay (t_{P_HL}) per gate	
Average t_p per gate (measured)	
Average t_p per gate (from datasheet)	

Is the recorded t_p value per gate same as in the datasheet? If not then how can you explain this difference?

2. [1.5 Pts] Record the values obtained in Experiment question 2 in Table 2 below.

Table 2

V_{OH} (from datasheet)	
V_{OL} (from datasheet)	
V_{IH_min}	
V_{IL_max}	

Are the recorded values same as in the datasheet? If not then how can you explain this difference?

3. [2 Pts] Why should V_{IL_max} be greater than V_{OL_max}? And similarly why should V_{OH_min} be greater than V_{IH_min}?

4. [2.5 Pts] Research question: Describe briefly in 1-2 sentences the following physical characteristics of a logic gate. Also mention the problems that may arise if their values surpass their thresholds.
   a. Fan-out
   b. Current levels I_{OL} , I_{OH} , I_{IL} , I_{IH}

5. [2.5 Pts] Extract for the AND IC datasheet attached on BB the typical values for the following physical characteristics. Mention any conditions required to replicate these values in lab.
   a. Fan-out
   b. Current levels I_{OL} , I_{OH} , I_{IL} , I_{IH}