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Due: 19/09/23

Digital Design Lab Report

Basic Logic Gates

1. [2 Pts] What is wrong about the position of the IC in Figure 13 below? What will happen if the chip is powered on with that setup?

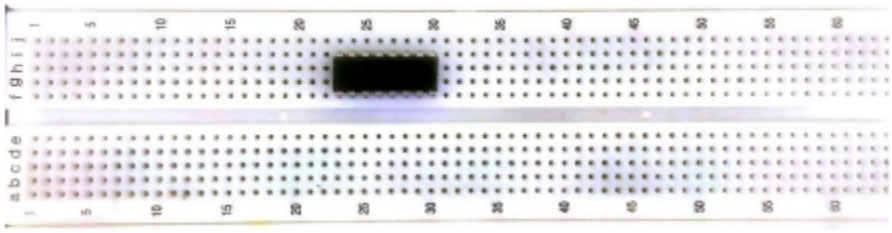


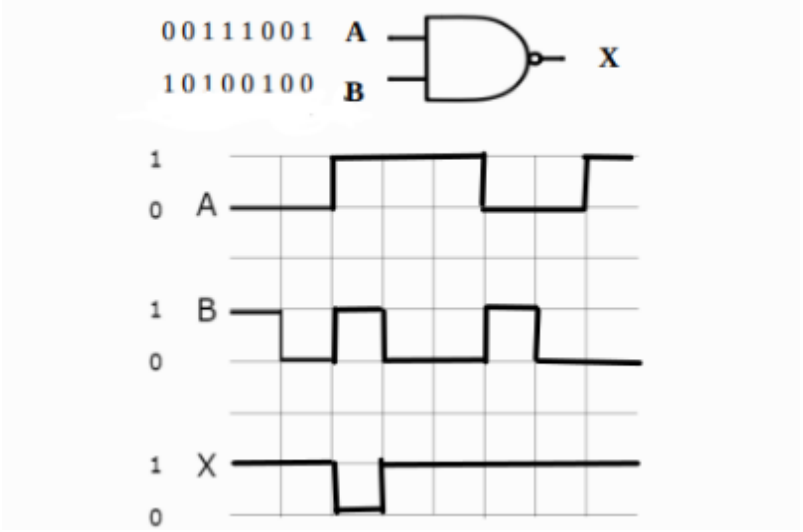
Figure 13. A wrong placement of a DIP chip on breadboard

The position of the IC in Figure 13 on the breadboard leads to unintended pin connections due to the columns being connected. To prevent this issue, reposition the IC lower on the board, separating the sets of pins from each other. Powering the chip with the current setup risks multiple power and ground connections, complicating and potentially rendering the circuit unusable.

2. [2 Pts] How can you implement the inversion using a NOR gate? (Research Q) Why do we sometimes prefer to do inversion in NORs and NANDs instead of using the NOT gate?

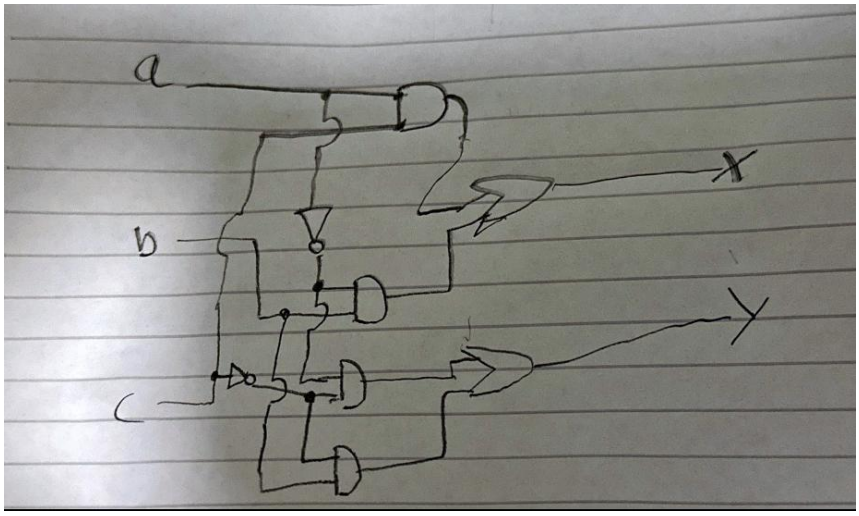
A NOR gate with interconnected inputs from a single source functions as a NOT gate. NANDs and NORs are preferable as they are less expensive and easier to design, while able to implement other gates such as NOT, AND, and NOR making them versatile and efficient choices in digital circuitry.

ɔmplete the timing diagram for the shown inputs sequences in Figure 14.

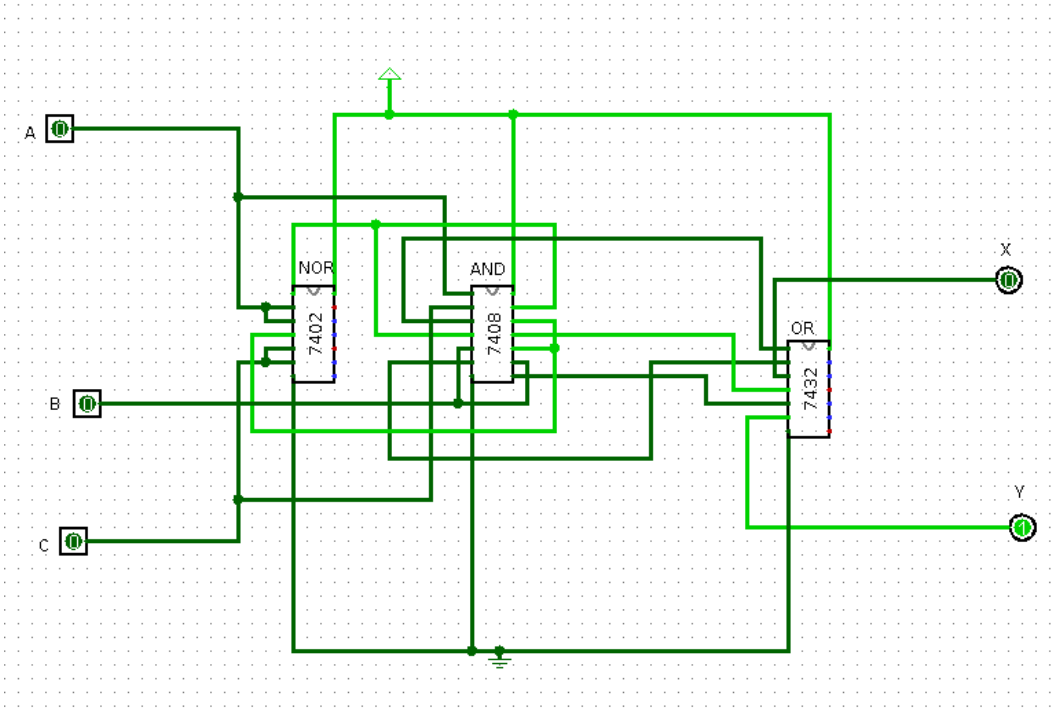


4. [4 Pts] The Boolean expressions of a circuit that has three inputs and two outputs are:
   $X = a\,c + a'\,b$
   $Y = a'\,c' + b\,c'$
   Answer the following questions about this circuit:
   a. Draw the circuit of both signals.
   b. Simulate the circuit using Logisim software. Draw the **pin-to-pin diagram** for the circuit using the proper chips from the 7400-lib (**not** using individual gates). Provide a screenshot of the circuit on Logisim along with the ***. circ*** file.

Circuit Raw Sketch:



Circuit Simulation:



Circuit Analysis:

a	b	c	x	y
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0