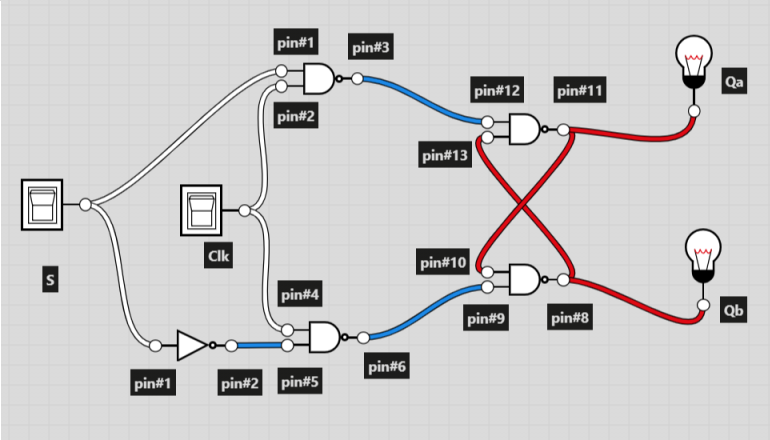
Part Ⅰ

1.

74LS00

NAND2

74LS00

NAND2

74LS00

NAND2

74LS04

not1

74LS00

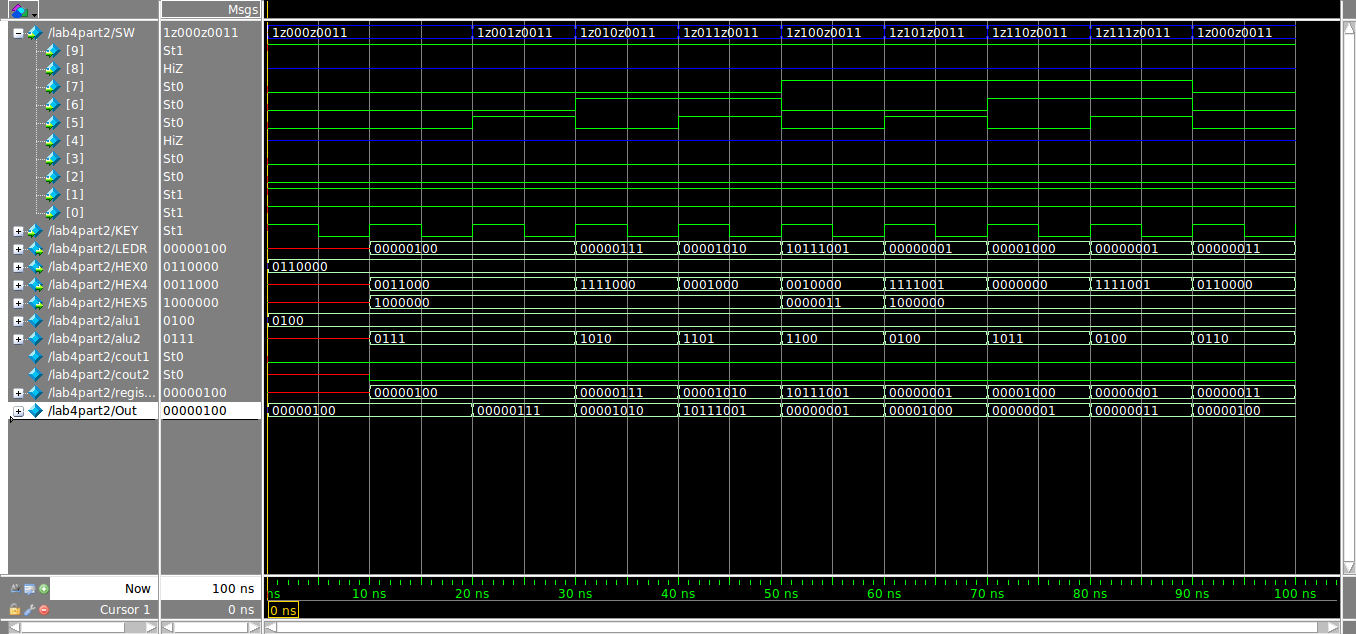
NAND2

3.

The input combination of Clk starting with 0 should not be the first test. If the Clk is 0 at beginning,

the latch will have 1 for both inputs, when the result of Q depends on the last output, and cause error.

Part 2



Part III

1.

Q[7] Q[6] Q[5] Q[4] Q[3] Q[2] Q[1] Q[0]

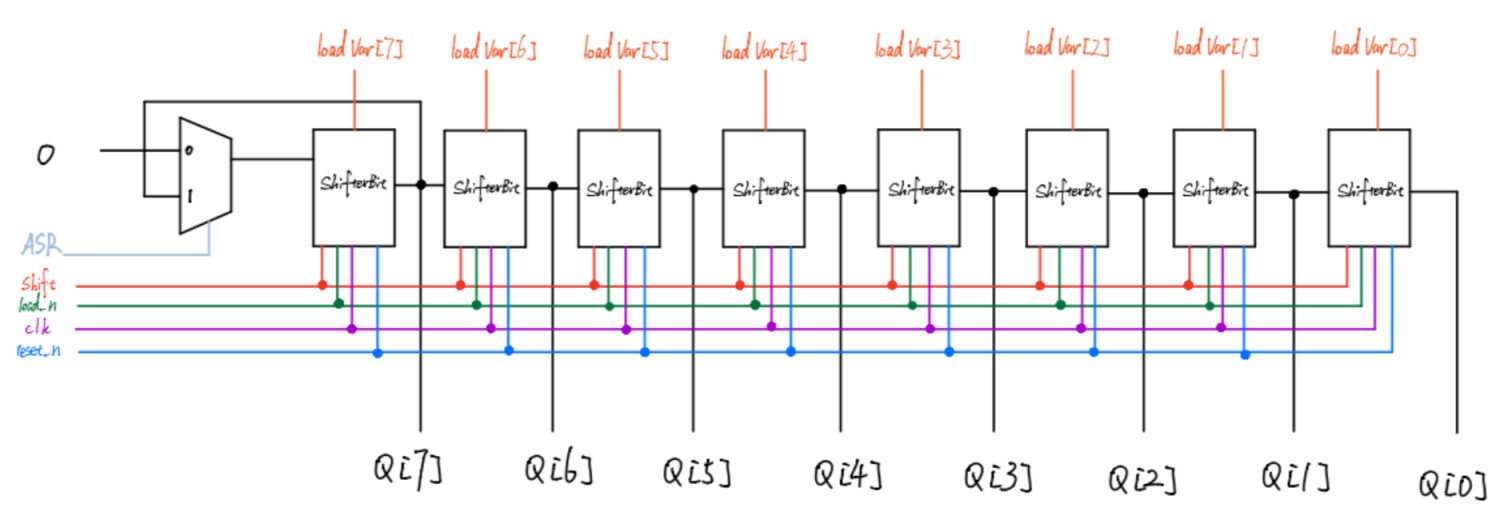
Cycle 0: A7 A6 A5 A4 A3 A2 A1 A0

Cycle 1: A7 A6 A5 A4 A3 A2 A1 A0

Cycle 2: A7 A6 A5 A4 A3 A2 A1 A0

: : :

2.



U8

U7

U6

U5

U4

U3

U2

U1

U0

3.