Examen 4, 5 y 6. VLSI. Individual.

Examen 4: Escritura de código VHDL, Examen 5: Resolución de problemas por tiempo. Examen 6: abstracción y trabajo individual

Problema: SDRAM de tarjeta de10-lite. Crear proyecto que contenga los procesos adecuados y que utilice la plantilla de estados adecuadamente.

Duración: Máximo de calificación x hora. 1 hora: para sacar 10, 1 hr15 para sacar 9, 1h30 para sacar 8, 1h40 para sacar 7, 1h50 para sacar 6. Después ya es 5.

Rúbrica

1) **Escribió código adecuado para tabla de verdad de "comandos" (1 pto.)**
2) **Escribió código adecuado para tabla de verdad de "DQM" (1 pto.)**
3) **Escribió código adecuado para tabla de verdad de "CKE" (1 pto.)**
4) **Escribió código adecuado para tabla "funcional" con TODOS los estados (2 ptos)**
    a. **Escribió código adecuado para tabla de verdad de "idle" (1 pto.)**
    b. **Escribió código adecuado para tabla de verdad de "Row active" (1 pto.)**
    c. **Escribió código adecuado para tabla de verdad de "Read" (1 pto.)**
    d. **Escribió código adecuado para tabla de verdad de "Pre.." (1 pto.)**
    e. **Escribió código adecuado para tabla de verdad de "Row active" (1 pto.)**
    f. **Escribió código adecuado para tabla de verdad de "write recover" (1 pto.)**
    g. **Escribió código adecuado para tabla de verdad de "write recover + Pre.." (1 pto.)**
    h. **Escribió código adecuado para tabla de verdad de "refresh" (1 pto.)**
    i. **Escribió código adecuado para tabla de verdad de "mode register" (1 pto.)**
5) **Escribió código adecuado para TOP (2 ptos.)**
6) **Realizo conexiones PINs a tarjeta FPGA (1 pto.)**
7) **Mostró RTL final (1 pto.)**
8) **Envió proyecto es RAR o ZIP a classroom antes del tiempo vencido (1 pto.)**
9) **Realizó pruebas de funcionamiento (1 pto.)**

Total de puntos: 20 para sacar 10 de calificación

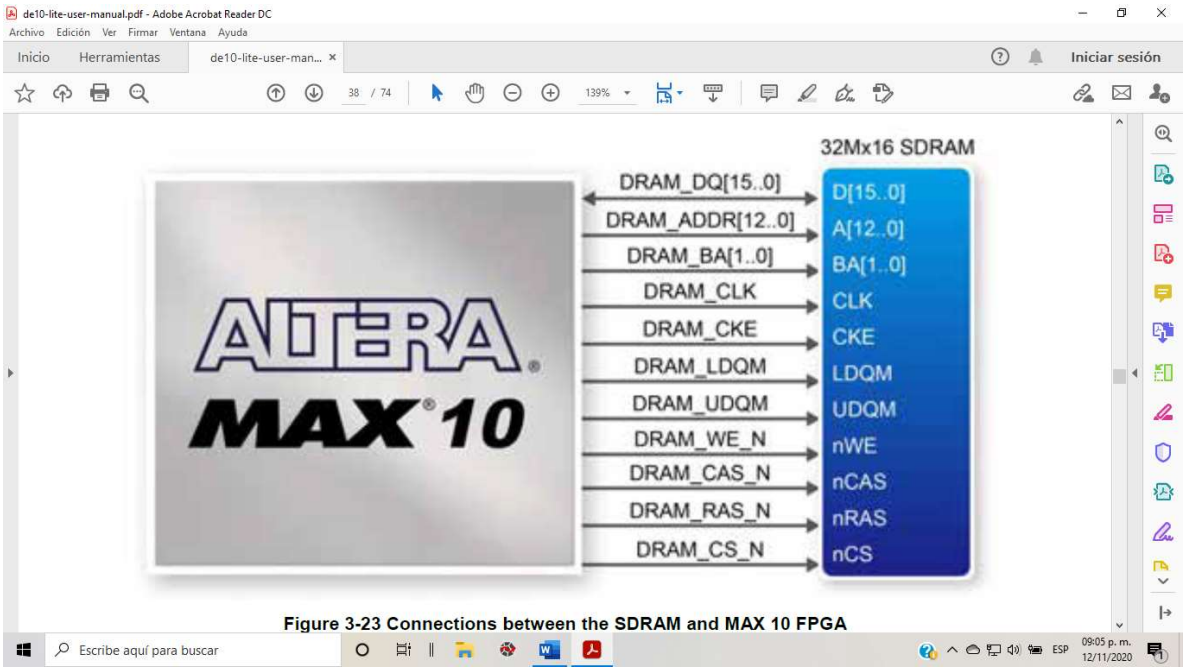
DATOS NECESARIOS A SABER:

Se tiene una memoria en chip de 1,638Kbit M9K

Que se puede organizar en 16Mx32, 32Mx16, 64Mx8, 512Mb

El reloj debe estar a 200 o 166 o 143mhz en lógica positiva

Enseguida se muestran las conexiones



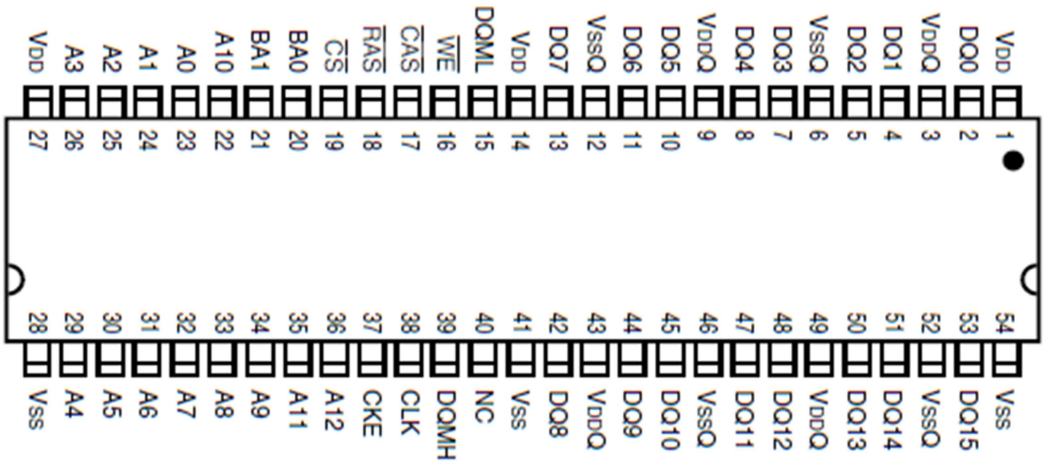
Con los PINS

DRAM_BA0	PIN_T21	SDRAM Bank Address[0]
DRAM_BA1	PIN_T22	SDRAM Bank Address[1]
DRAM_LDQM	PIN_V22	SDRAM byte Data Mask[0]
DRAM_UDQM	PIN_J21	SDRAM byte Data Mask[1]
DRAM_RAS_N	PIN_U22	SDRAM Row Address Strobe
DRAM_CAS_N	PIN_U21	SDRAM Column Address Strobe
DRAM_CKE	PIN_N22	SDRAM Clock Enable
DRAM_CLK	PIN_L14	SDRAM Clock
DRAM_WE_N	PIN_V20	SDRAM Write Enable
DRAM_CS_N	PIN_U20	SDRAM Chip Select

DRAM_DQ0	PIN_Y21	SDRAM Data[0]
DRAM_DQ1	PIN_Y20	SDRAM Data[1]
DRAM_DQ2	PIN_AA22	SDRAM Data[2]
DRAM_DQ3	PIN_AA21	SDRAM Data[3]
DRAM_DQ4	PIN_Y22	SDRAM Data[4]
DRAM_DQ5	PIN_W22	SDRAM Data[5]
DRAM_DQ6	PIN_W20	SDRAM Data[6]
DRAM_DQ7	PIN_V21	SDRAM Data[7]
DRAM_DQ8	PIN_P21	SDRAM Data[8]
DRAM_DQ9	PIN_J22	SDRAM Data[9]
DRAM_DQ10	PIN_H21	SDRAM Data[10]
DRAM_DQ11	PIN_H22	SDRAM Data[11]
DRAM_DQ12	PIN_G22	SDRAM Data[12]
DRAM_DQ13	PIN_G20	SDRAM Data[13]
DRAM_DQ14	PIN_G19	SDRAM Data[14]
DRAM_DQ15	PIN_F22	SDRAM Data[15]

Signal Name	FPGA Pin No.	Description
DRAM_ADDR0	PIN_U17	SDRAM Address[0]
DRAM_ADDR1	PIN_W19	SDRAM Address[1]
DRAM_ADDR2	PIN_V18	SDRAM Address[2]
DRAM_ADDR3	PIN_U18	SDRAM Address[3]
DRAM_ADDR4	PIN_U19	SDRAM Address[4]
DRAM_ADDR5	PIN_T18	SDRAM Address[5]
DRAM_ADDR6	PIN_T19	SDRAM Address[6]
DRAM_ADDR7	PIN_R18	SDRAM Address[7]
DRAM_ADDR8	PIN_P18	SDRAM Address[8]
DRAM_ADDR9	PIN_P19	SDRAM Address[9]
DRAM_ADDR10	PIN_T20	SDRAM Address[10]
DRAM_ADDR11	PIN_P20	SDRAM Address[11]
DRAM_ADDR12	PIN_R20	SDRAM Address[12]

La tarjeta de10 lite contiene este CHIP

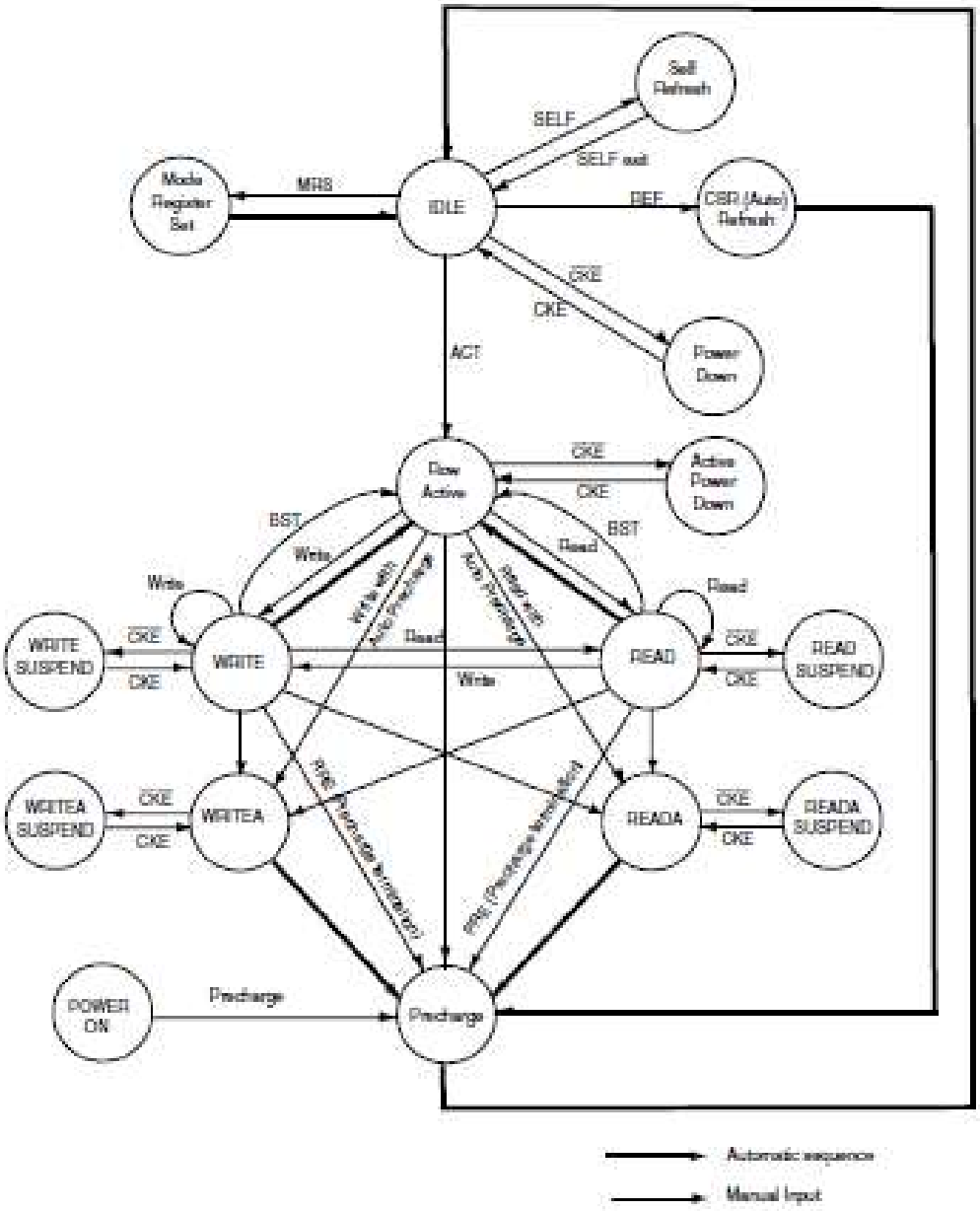


Se tiene:

1) Datos: DQ [15 .. 0] a D[15..0]
2) Direcciones ADDR [12 .. 0] a A[12..0]
3) Selector de banco de direcciones de 2bits BA[1] y Ba[0] (Activo: 00, Read: 01, Write:10, Precarga:11)
4) CLK entrada de reloj
5) Habilitador de reloj. Si CKE=1 valido sino invalido (suspendido)
6) Mascara de los datos de entrada y de salida DQM.
    a. Lectura: si DQML y DQMH=1 es buffer habilitado,
    b. Escritura si es =0 se puede escribir
7) Habilitador de escritura WE_N a WE depende de RAS' y WE'
8) Comando de dirección de columna CAS_N a nCas depende de RAS' y WE'
9) Comando de dirección de renglón RAS_N a nRAS
10) El chip select, cuando el dispositivo es habilitado, CS_N es nCS si es=0 sino deshab.

FAVOR DE ABRIR EL DATA SHEET PARA VER MEJOR LAS IMÁGENES SIGUIENTE QUE FUERON PEGADAS DE AHÍ.

STATE DIAGRAM



COMMAND TRUTH TABLE

Function	CKE n – 1	n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	A10	A12, A11 A9 - A0
Device deselect (DESL)	H	×	H	×	×	×	×	×	×	×
No operation (NOP)	H	×	L	H	H	H	×	×	×	×
Burst stop (BST)	H	×	L	H	H	L	×	×	×	×
Read	H	×	L	H	L	H	V	V	L	V
Read with auto precharge	H	×	L	H	L	H	V	V	H	V
Write	H	×	L	H	L	L	V	V	L	V
Write with auto precharge	H	×	L	H	L	L	V	V	H	V
Bank activate (ACT)	H	×	L	L	H	H	V	V	V	V
Precharge select bank (PRE)	H	×	L	L	H	L	V	V	L	×
Precharge all banks (PALL)	H	×	L	L	H	L	×	×	H	×
CBR Auto-Refresh (REF)	H	H	L	L	L	H	×	×	×	×
Self-Refresh (SELF)	H	L	L	L	L	H	×	×	×	×
Mode register set (MRS)	H	×	L	L	L	L	L	L	L	V

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

DQM TRUTH TABLE

Function	CKE n-1	n	DQMH	DQML
Data write / output enable	H	×	L	L
Data mask / output disable	H	×	H	H
Upper byte write enable / output enable	H	×	L	×
Lower byte write enable / output enable	H	×	×	L
Upper byte write inhibit / output disable	H	×	H	×
Lower byte write inhibit / output disable	H	×	×	H

Note:
1. H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.
2. x16 options shown. x32 DQM0-DQM3 is similar in function.

CKE TRUTH TABLE

Current State /Function	CKE n – 1	n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Activating Clock suspend mode entry	H	L	×	×	×	×	×
Any Clock suspend mode	L	L	×	×	×	×	×
Clock suspend mode exit	L	H	×	×	×	×	×
Auto refresh command Idle (REF)	H	H	L	L	L	H	×
Self refresh entry Idle (SELF)	H	L	L	L	L	H	×
Power down entry Idle	H	L	×	×	×	×	×
Self refresh exit	L	H	L	H	H	H	×
	L	H	H	×	×	×	×
Power down exit	L	H	×	×	×	×	×

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

FUNCTIONAL TRUTH TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Idle	H	X	X	X	X	DESL	Nop or Power Down[3]
	L	H	H	H	X	NOP	Nop or Power Down[3]
	L	H	H	L	X	BST	Nop or Power Down
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL [3]
	L	H	L	L	A, CA, A10	WRIT/ WRITA	ILLEGAL[3]
	L	L	H	H	BA, RA	ACT	Row activating
	L	L	H	L	BA, A10	PRE/PALL	Nop
	L	L	L	H	X	REF/SELF	Auto refresh or Self-refresh[4]
	L	L	L	L	OC, BA1=L	MRS	Mode register set
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	Nop
	L	H	L	H	BA, CA, A10	READ/READA	Begin read [5]
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write [5]
	L	L	H	H	BA, RA	ACT	ILLEGAL [3]
	L	L	H	L	BA, A10	PRE/PALL	Precharge Precharge all banks[6]
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end to Row active
	L	H	H	H	X	NOP	Continue burst to end Row Row active
	L	H	H	L	X	BST	Burst stop, Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read [7]
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write [7,8]
	L	L	H	H	BA, RA	ACT	ILLEGAL [3]
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end Write recovering
	L	H	H	H	X	NOP	Continue burst to end Write recovering
	L	H	H	L	X	BST	Burst stop, Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP [7,8]
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP [7]
	L	L	H	H	BA, RA	RA ACT	ILLEGAL [3]
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging [9]
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA=Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Read with auto Precharging	H	×	×	×	×	DESL	Continue burst to end, Precharge
	L	H	H	H	x	NOP	Continue burst to end, Precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL [11]
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL [11]
	L	L	H	H	BA, RA	ACT	ILLEGAL [8]
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL [11]
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write with Auto Precharge	H	×	×	×	×	DESL	Continue burst to end, Write recovering with auto precharge
	L	H	H	H	×	NOP	Continue burst to end, Write recovering with auto precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL[11]
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL [11]
	L	L	H	H	BA, RA	ACT	ILLEGAL [8,11]
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL [8,11]
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Precharging	H	×	×	×	×	DESL	Nop, Enter Idle after tRP
	L	H	H	H	×	NOP	Nop, Enter Idle after tRP
	L	H	H	L	×	BST	Nop, Enter Idle after tRP
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL [8]
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL [8]
	L	L	H	H	BA, RA	ACT	ILLEGAL[8]
	L	L	H	L	BA, A10	PRE/PALL	Nop Enter Idle after tRP
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Row Activating	H	×	×	×	×	DESL	Nop, Enter bank active after tRCD
	L	H	H	H	×	NOP	Nop, Enter bank active after tRCD
	L	H	H	L	×	BST	Nop, Enter bank active after tRCD
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL [8]
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL [8]
	L	L	H	H	BA, RA	ACT	ILLEGAL [8,9]
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL [8]
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL}, x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA=Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Write Recovering	H	x	x	x	x	DESL	Nop, Enter row active after tDPL
	L	H	H	H	x	NOP	Nop, Enter row active after tDPL
	L	H	H	L	x	BST	Nop, Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	Begin read [9]
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin new write
	L	L	H	H	BA, RA	ACT	ILLEGAL [9]
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL [9]
	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write Recovering	H	x	x	x	x	DESL	Nop, Enter precharge after tDPL
with Auto	L	H	H	H	x	NOP	Nop, Enter precharge after tDPL
Precharge	L	H	H	L	x	BST	Nop, Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL [9,11]
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL [9,11]
	L	L	H	H	BA, RA	ACT	ILLEGAL [9,11]
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL [9,11]
	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Refresh	H	x	x	x	x	DESL	Nop, Enter idle after tRC
	L	H	H	x	x	NOP/BST	Nop, Enter idle after tRC
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Mode Register	H	x	x	x	x	DESL	Nop, Enter idle after 2 clocks
Accessing	L	H	H	H	x	NOP	Nop, Enter idle after 2 clocks
	L	H	H	L	x	BST	ILLEGAL
	L	H	L	x	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	x	x	BA, RA	ACT/PRE/PALL REF/MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA=Column Address, RA=Row Address, OC= Op-Code

CKE RELATED COMMAND TRUTH TABLE[1]

Current State	Operation	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Self-Refresh (S.R.)	INVALID, CLK (n - 1) would exit S.R.	H	X	X	X	X	X	X
	Self-Refresh Recovery[2]	L	H	H	X	X	X	X
	Self-Refresh Recovery[2]	L	H	L	H	H	X	X
	Illegal	L	H	L	H	L	X	X
	Illegal	L	H	L	L	X	X	X
	Maintain S.R.	L	L	X	X	X	X	X
Self-Refresh Recovery	Idle After t_{RC}	H	H	H	X	X	X	X
	Idle After t_{RC}	H	H	L	H	H	X	X
	Illegal	H	H	L	H	L	X	X
	Illegal	H	H	L	L	X	X	X
	Begin clock suspend next cycle[3]	H	L	H	X	X	X	X
	Begin clock suspend next cycle[3]	H	L	L	H	H	X	X
	Illegal	H	L	L	H	L	X	X
	Illegal	H	L	L	L	X	X	X
	Exit clock suspend next cycle[3]	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X
Power-Down (P.D.)	INVALID, CLK (n - 1) would exit P.D.	H	X	X	X	X	X	—
	EXIT P.D. -> Idle[3]	L	H	X	X	X	X	X
	Maintain power down mode	L	L	X	X	X	X	X
All Banks Idle	Refer to operations in Operative Command Table	H	H	H	X	X	X	—
	Refer to operations in Operative Command Table	H	H	L	H	X	X	—
	Refer to operations in Operative Command Table	H	H	L	L	H	X	—
	Auto-Refresh	H	H	L	L	L	H	X
	Refer to operations in Operative Command Table	H	H	L	L	L	L	Op - Code
	Refer to operations in Operative Command Table	H	L	H	X	X	X	—
	Refer to operations in Operative Command Table	H	L	L	H	X	X	—
	Refer to operations in Operative Command Table	H	L	L	L	H	X	—
	Self-Refresh[3]	H	L	L	L	L	H	X
	Refer to operations in Operative Command Table	H	L	L	L	L	L	Op - Code
	Power-Down[3]	L	X	X	X	X	X	X
Any state	Refer to operations in Operative Command Table	H	H	X	X	X	X	X
other than	Begin clock suspend next cycle[4]	H	L	X	X	X	X	X
listed above	Exit clock suspend next cycle	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X