Memory

Part 2 Update

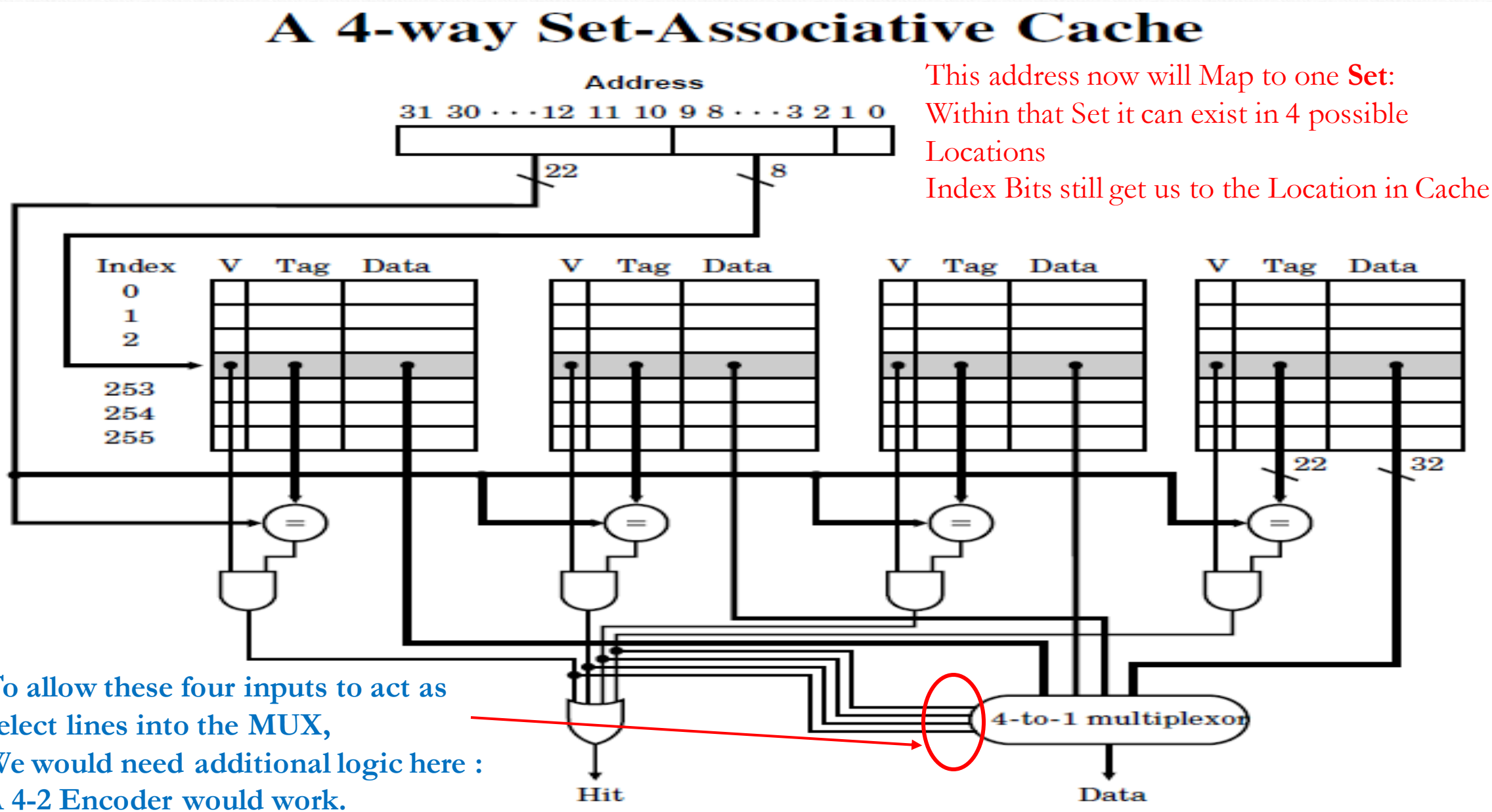
Course Evaluations

- Students Please take a few minutes to fill out the course evaluation for CS251:
- evaluate.uwaterloo.ca

Why is DRAM slower but cheaper than SRAM?

- A) DRAM writes are slower than reads due to capacitor refresh.. And it is cheaper because of the capacitors
- B) DRAM has much slower reads due to need to refresh the capacitors. Cheaper because it uses only one transistor
- C) SRAM is faster because it is using no capacitors and more expensive because it uses 2 transistors as opposed to one
- D) DRAM is slower because of address lookup uses large MUX
- E) SRAM faster because of two level decoding
- **ORIGINAL ANSWER IN CLASS (B) is incorrect. DRAM reads are equivalent to writes (both require a read and write to occur) Alternative Corrected Answer (B)**
- **B)** DRAM has much slower reads and writes than SRAM due to need to refresh the capacitors. Cheaper because it uses only one transistor

Alternative Placement Schemes



Final entries

2-way set associative cache

Memory Access

Dec	Binary	Hit/miss
20	10100	Miss
18	10010	Miss
20	10100	Hit
18	10010	Hit
22	10110	Miss
7	00111	Miss
22	10110	Hit
28	11100	Miss

Cache

Index	Tag0	Tag1
00	101	111
01		
10	100	101
11	001	

4-way set associative cache

Memory Access

Dec	Binary	Hit/miss
20	10100	Miss
18	10010	Miss
20	10100	Hit
18	10010	Hit
22	10110	Miss
7	00111	Miss
22	10110	Hit
28	11100	Miss

Cache

Index	Tag0	Tag1	Tag2	Tag3
0	1010	1001	1011	1110
1	0011			

Fully associative cache

Memory Access

Dec	Binary	Hit/miss
20	10100	Miss
18	10010	Miss
20	10100	Hit
18	10010	Hit
22	10110	Miss
7	00111	Miss
22	10110	Hit
28	11100	Miss

Cache

Tag0	Tag1	Tag2	Tag3	Tag4	Tag5	Tag6	Tag7
10100	10010	10110	00111	11100			

Fully associative cache

Memory Access

Dec	Binary	Hit/miss
20	10100	Miss
18	10010	Miss
20	10100	Hit
18	10010	Hit
22	10110	Miss
7	00111	Miss
22	10110	Hit
28	11100	Miss

Additional Requests:

30 11110 M

24 11000 M

04 00100 M

20 10100 H

08 01000 * where does this go

Cache

Tag0	Tag1	Tag2	Tag3	Tag4	Tag5	Tag6	Tag7
10100	10010	10110	00111	11100	11110	11000	00100

Fully associative cache

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Fully associative cache

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