

NORTH SOUTH UNIVERSITY

Department of Electrical & Computer Engineering (ECE)

CSE 332 Computer Organization & Architecture

Section: 02

Faculty: Tanjila Farah (TnF)

Lab Report: 2

Design of a 4-bit Binary Up-Down Synchronous counter

Submitted By: (Writer's name & ID)

Name: Nadim Mahmud	ID: 19218	77642
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Group Number: 0

Name	ID
Member 1 Sayef Uddin Ahmed Sadman	2212121042
Member 2 Musanna Ibn Amin	2233285042
Member 3 Hadim Mahmad Inliger Istal	192187764222196 1

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Date of Experiment: Date of Submission:

For Instructor's use only

SCORE:	REMARKS:		
100/100			
PENALTY:			

Objective;

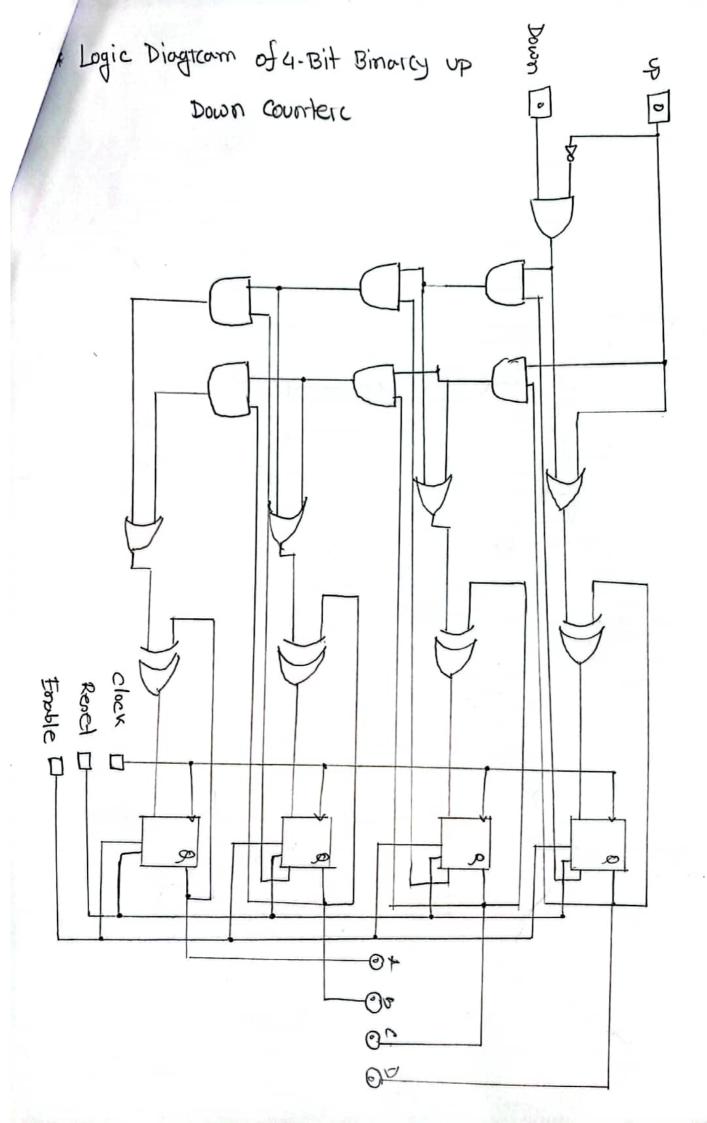
- * Design a 4-bit up-down counterc
- # using flip-slops to storce the 4-bit value.
- * use 4 D flip-flops to create a 4-bit tegister
- to use xor create and D Flip-Flop to create + flip-Flop.
- + How the countere Registere works with clock pulses.
- tow the value changes, by giving up counters and down counters.

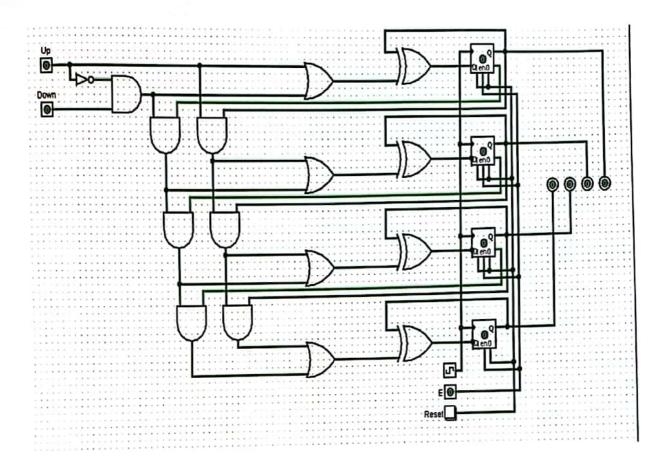
List of Equipments

- + Trainere Boated-
- * IC 7404, 2×7408, 7432, 7486, 2×7474
- * Witces for connection.
- + power Suppy.

A register that goer through a predetermined sequence of states upon the application of input pulses, is called a counter.

A 4-6it binarcy up/down counters goen from 0000 to 1111 and buck from 1111 to 0000. It was 4 + flip-flops, which toggle their output when the input is I, and stay the same When the input iso. All flp-flops share the same clock pulse. Fore counting up, the next flip-flop changer when the state goes from 0 to 1. Forc counting down, the next flip-flop changes when the state goes from 1 to 0.





Treuth Table:

clock pube	A	В	C	D
120	0	0	0	0
PI	0	٥	0	1
P2	0	0	1	0
P3	0	0	1	
P4	0	١	D	0
P5	0	1	0	
P6	0	ı	l	0
P 7	0	1	1	l
PS	1	0	0	0
P9	1	0	0	١
PID	1	0	1	0
PII	1	0	1	l
P12	1	1	0	0
P13	1	1	D	1
P14	1	1	1	0
PIS	1	1	1	1

In the lab we build a 4-bit Binutey up-Down counters. first we collect bund D flip-flop Ic (7474). we need 4 D flip-flop. 80, we collect 2 Ic. Thin we check the Icand there IC was ox. After that we take IC 7404, 2×-7408, 7432 and 7486. We placed the Ic on our trainere board. Then we dream the circuit diagram in loginein and stard with our horrdwere, connect all the winer with Ics. After that we connect power supply, After And we sow that the light of output P is not working. Then we chacked the values for 3 output. output for first 3 Its working perstectly. But we count complete ourc corunteta we time tune was some is ver with wine. That's why we own't get

any value fore output D. Then we checked for wires, but still couldn't fix it. Due to rearning out of time, we stoped. From two wext claim we will be more caraful with everything and try to complete our task.

CSE 332/ EEE 336/ ETE 336 <u>Truth Table:</u>

Computer Organization and Architecture

Clock pulse	Α .	В .	c	D ,
PO	0	0	0	0
P1	0,	0	0	1
P2	0	0	1	0
Р3	0	0	1	٠1
P4	0	1	0	0
P5	0	1	0	1
Р6	0	1	1	0
P7	0	1	1	1
Р8	1	0	0	0
Р9	1	0	0	2
P10	1	0	1	0
P11	1	0	1	1
P12	1	1	0	0
P13	1	1	0	1
P14	1	1	1	0
P15	1	1	1	1

dola sisse