
STM32
CubeMX

1. Description

1.1. Project

Project Name	stm32g473
Board Name	custom
Generated with:	STM32CubeMX 6.4.0
Date	12/31/2021

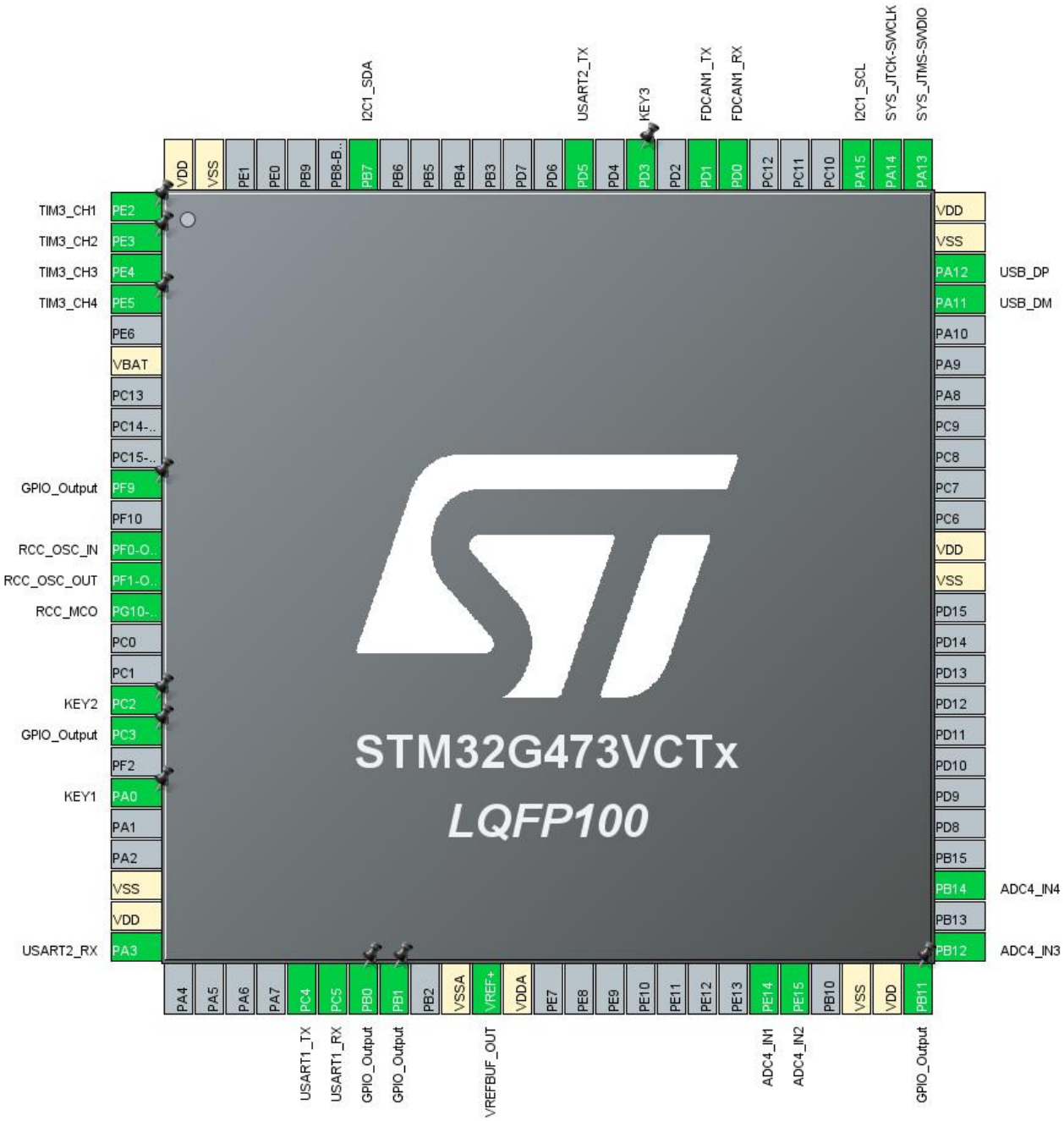
1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x3
MCU name	STM32G473VCTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration



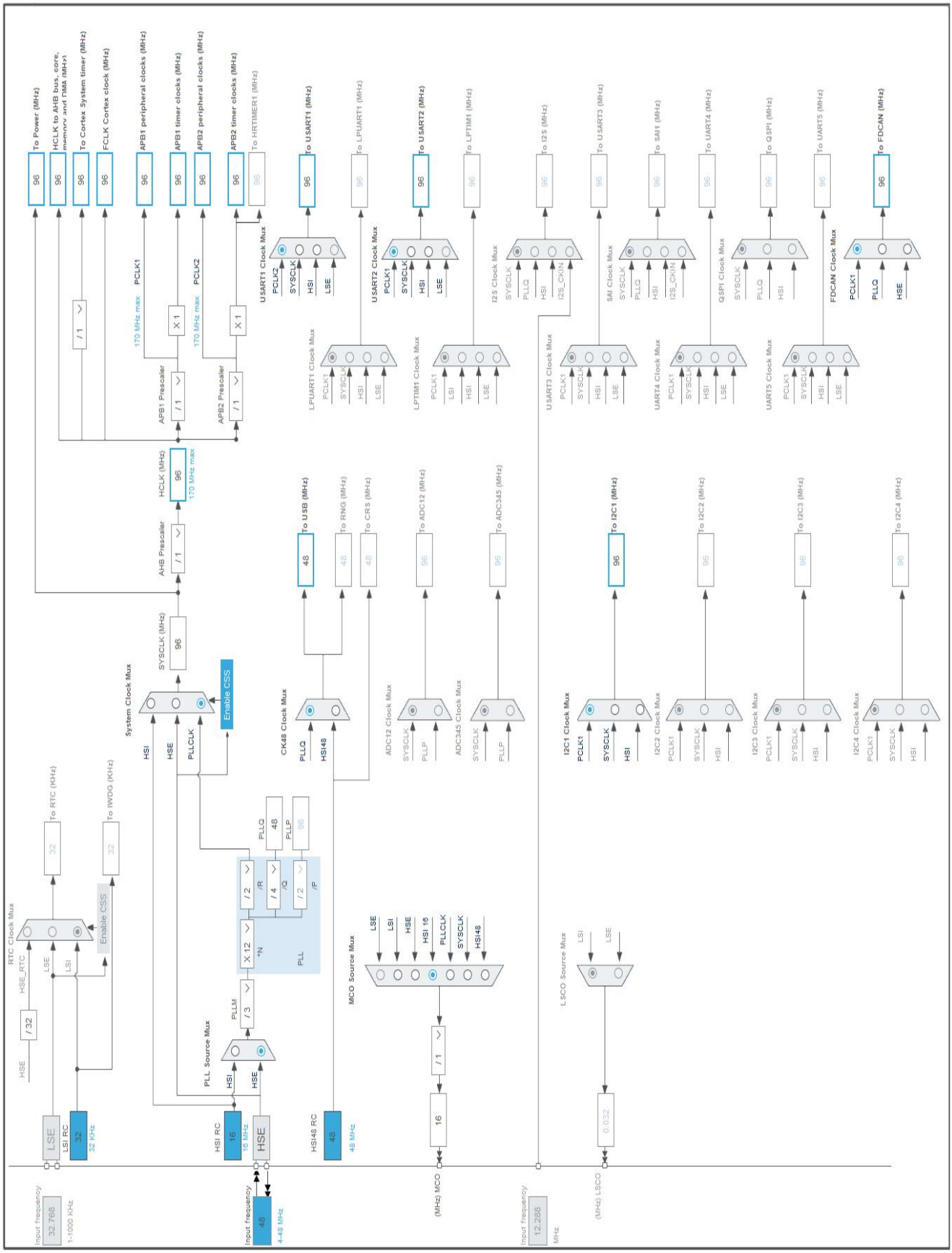
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	TIM3_CH1	
2	PE3	I/O	TIM3_CH2	
3	PE4	I/O	TIM3_CH3	
4	PE5	I/O	TIM3_CH4	
6	VBAT	Power		
10	PF9 *	I/O	GPIO_Output	
12	PF0-OSC_IN	I/O	RCC_OSC_IN	
13	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
14	PG10-NRST	I/O	RCC_MCO	
17	PC2 *	I/O	GPIO_Input	KEY2
18	PC3 *	I/O	GPIO_Output	
20	PA0 *	I/O	GPIO_Input	KEY1
23	VSS	Power		
24	VDD	Power		
25	PA3	I/O	USART2_RX	
30	PC4	I/O	USART1_TX	
31	PC5	I/O	USART1_RX	
32	PB0 *	I/O	GPIO_Output	
33	PB1 *	I/O	GPIO_Output	
35	VSSA	Power		
36	VREF+	MonoIO	VREFBUF_OUT	
37	VDDA	Power		
45	PE14	I/O	ADC4_IN1	
46	PE15	I/O	ADC4_IN2	
48	VSS	Power		
49	VDD	Power		
50	PB11 *	I/O	GPIO_Output	
51	PB12	I/O	ADC4_IN3	
53	PB14	I/O	ADC4_IN4	
63	VSS	Power		
64	VDD	Power		
72	PA11	I/O	USB_DM	
73	PA12	I/O	USB_DP	
74	VSS	Power		
75	VDD	Power		
76	PA13	I/O	SYS_JTMS-SWDIO	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
77	PA14	I/O	SYS_JTCK-SWCLK	
78	PA15	I/O	I2C1_SCL	
82	PD0	I/O	FDCAN1_RX	
83	PD1	I/O	FDCAN1_TX	
85	PD3 *	I/O	GPIO_Input	KEY3
87	PD5	I/O	USART2_TX	
94	PB7	I/O	I2C1_SDA	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm32g473
Project Folder	D:\GIT\Robot\stm32g473_demo\pcb
Toolchain / IDE	MDK-ARM V5.27
Firmware Package Name and Version	STM32Cube FW_G4 V1.5.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x2000
Minimum Stack Size	0x4000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	Yes

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_USART1_UART_Init	USART1
4	MX_TIM17_Init	TIM17
5	MX_TIM3_Init	TIM3
6	MX_USART2_UART_Init	USART2
7	MX_FDCAN1_Init	FDCAN1
8	MX_I2C1_Init	I2C1
9	MX_USB_Device_Init	USB_DEVICE
10	MX_ADC4_Init	ADC4

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x3
MCU	STM32G473VCTx
Datasheet	DS12712_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

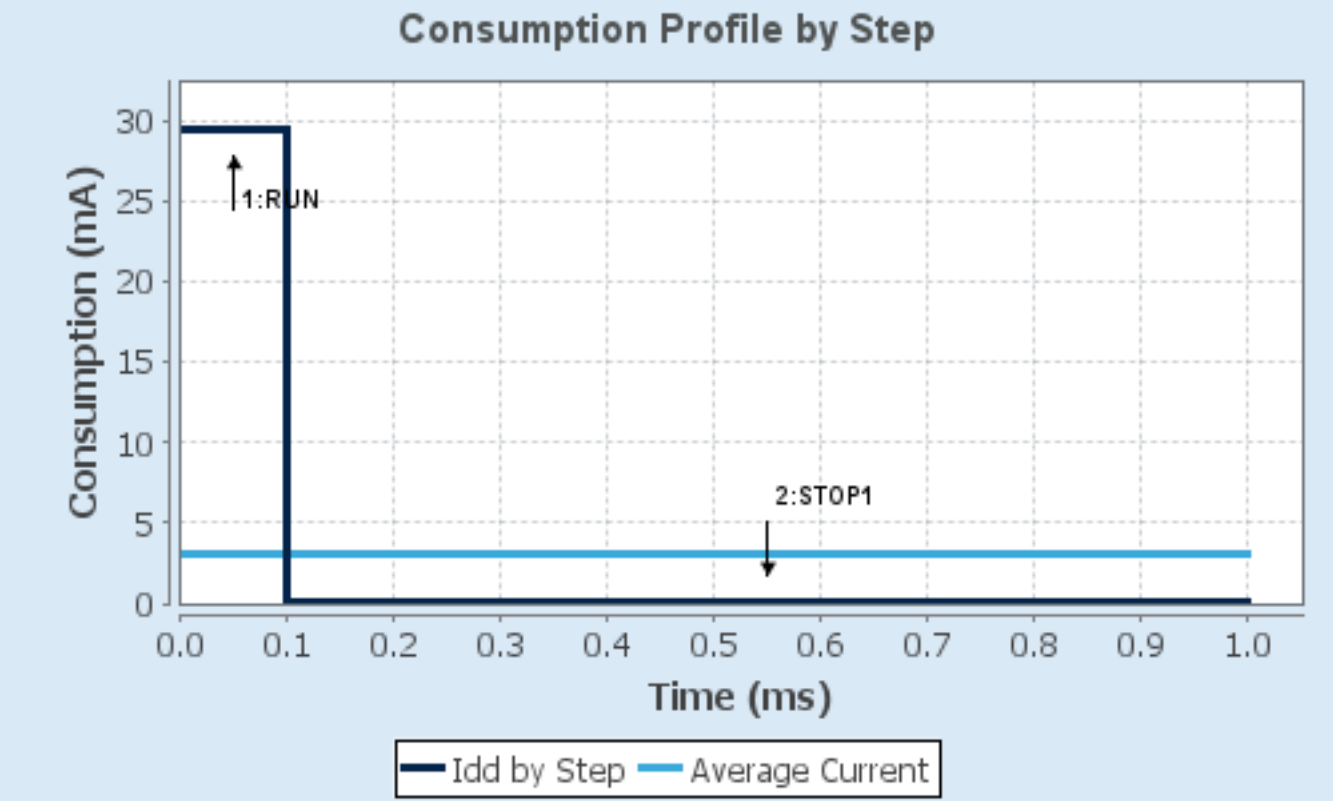
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/DualBank/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	29.5 mA	80.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	123.27	129.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	3.02 mA
Battery Life	1 month, 16 days, 9 hours	Average DMIPS	212.5 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC4

IN1: IN1 Differential

IN3: IN3 Differential

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 2
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. FDCAN1

mode: Activated

7.2.1. Parameter Settings:

Basic Parameters:

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Std Filters Nbr	0
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10B0DCFB ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

mode: Master Clock Output

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	**Power Regulator Voltage Scale 1 boost ***

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.5. SYS

Debug: Serial Wire

VREFBUF Mode: Internal voltage reference

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.5.1. Parameter Settings:

Voltage_Reference_Buffer_Settings:

Trimming Mode	Factory Trimming
Internal Voltage reference scale	SCALE 0: around 2.048 V

7.6. TIM3

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1700-1 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.7. TIM17

mode: Activated

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**17-1 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**10-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

7.8. USART1

Mode: Multiprocessor Communication

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	**460800 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Wake-Up Method	Idle Line
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable

TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.9. USART2

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.10. USB

mode: Device (FS)

7.10.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s

Physical interface	Internal Phy
Sof Enable	Disabled

Power Parameters:

Low Power	Disabled
Link Power Management	Disabled
Battery Charging	Disabled

7.11. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.11.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

7.11.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC4	PE14	ADC4_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PE15	ADC4_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PB12	ADC4_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PB14	ADC4_IN4	Analog mode	No pull-up and no pull-down	n/a	
FDCAN1	PD0	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PA15	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PG10-NRST	RCC_MCO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	VREF+	VREFBUF_OUT	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM3	PE2	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE3	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE4	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PC4	USART1_TX	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	
	PC5	USART1_RX	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	
USART2	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	
GPIO	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC2	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY2
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	
	PA0	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	
	PD3	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY3

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USB low priority interrupt remap	true	0	0
FDCAN1 interrupt 0	true	0	0
TIM1 trigger and commutation interrupts and TIM17 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USB high priority interrupt remap	unused		
FDCAN1 interrupt 1	unused		
I2C1 event interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C1 error interrupt	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		
ADC4 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USB low priority interrupt remap	false	true	true
FDCAN1 interrupt 0	false	true	true
TIM1 trigger and commutation interrupts and TIM17 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00528822.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00355726.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00500968.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00074240.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00083249.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00311483.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442716.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00605707.pdf
Application note	http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note	http://www.st.com/resource/en/application_note/DM00610467.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625282.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf