LeWiz Ethernet MAC Controller

Directory Description of Core 3 Code Release

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"The Wizard of Internet Communications"

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Change Log

Version	Significant Changes
1.00	Release version (pending review)
1.01 OSrc	Open source release
1.02	Modified for Core3

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NOTE: This document is intended for HW users using LeWiz MAC IP Core Test Bench.

1 Directory Map:

LMAC3_INFO
- ASYNCH_FIFO – containing technology independent behavioral FIFO model
- AXIS_BRIDGE – AXI4 Stream (AXIS) bus bridge model
- AXIS_LMAC_TB – AXIS LeWiz MAC testbench
- AXIS_LMAC_TOP – top level of LMAC with AXIS interface
- AXIS_MASTER – AXIS bus master behavioral model
- LMAC_CORE_TOP – main LMAC core model with FIFO interface
- PHY_EMULATOR – behavioral model of PHY emulator to test various PHY speeds
- TESTS – contain TX/RX tests and results
- waveforms – examples of waveforms for Modelsim
- work – Modelsim specific database

2 Abbreviations:

AXIS = AXI4 stream
LMAC = LeWiz MAC
PHY = Physical layer
TB = TestBench
TX = Transmit
RX = Receive

3 Description of each directory

3.1 LMAC3_INFO:

This is the top directory that contains all the subfolders described below including the verification results and all other relevant information.

3.2 ASYNCH_FIFO: (behavioral code)

This directory only contains the behavioral model of the FIFO to be used as a base FIFO module throughout the entire project. All other FIFOs used in this project are created by designing a wrapper on top of this base FIFO. This model is ASIC/FPGA technology independent.

3.3 AXIS_BRIDGE:

This directory contains the behavioral code for the AXI4 stream interface bridge. It includes a top-level module named AXIS_BRIDGE_TOP which instantiated 4 FIFOs and 4 control logic modules for transmitting and receiving data and control information between the AXIS_MASTER module and LMAC_CORE_TOP module.

3.4 AXIS_LMAC_TB: (behavioral code)

This directory contains a top level testbench named AXIS_LMAC_TB for system level testing of the LMAC_CORE_TOP module.

3.5 AXIS_LMAC_TOP:

This directory contains a top-level module that instantiates the AXIS_BRIDGE_TOP module and LMAC_CORE_TOP module.

3.6 AXIS_MASTER: (behavioral code)

This directory contains the code of the AXI_STREAM_MASTER module. AXI_STREAM_MASTER is mainly used for generating the desired number of the packet to the AXIS_BRIDGE_TOP. It also contains the memory write and read modules to store the data and control information for the simulation purpose.

3.7 LMAC_CORE_TOP: (synthesizable code)

This directory contains the code of the main LMAC IP Core (Core3) design. The top module is named LMAC_CORE_TOP. It contains the core logic for both Tx and Rx sides. It supports all five speed modes 100G, 50G, 40G, 25G, and 10G bit per second.

3.8 PHY_EMULATOR: (behavioral code)

This directory contains the behavioral code to emulate the 256-bit CGMII PHY interface. It supports loopback testing or allows the user to generate stored packets into the LMAC Core using the rx_pkt_gen_100G module inside the PHY Emulator. For loopback mode, it causes the packets transmitted by LMAC core looping back into the RX side of the LMAC core. In network generated mode, it enables user to generate packets into the Rx side of the LMAC core.

3.9 TESTS: (script code)

Contains all the test examples, test scripts, test files, test results.

3.10 waveforms: (Modelsim info)

Contains example waveform configuration files. These files can be opened in Modelsim's wave window.

3.11 work: (Modelsim info)

Contains Modelsim specific data files.