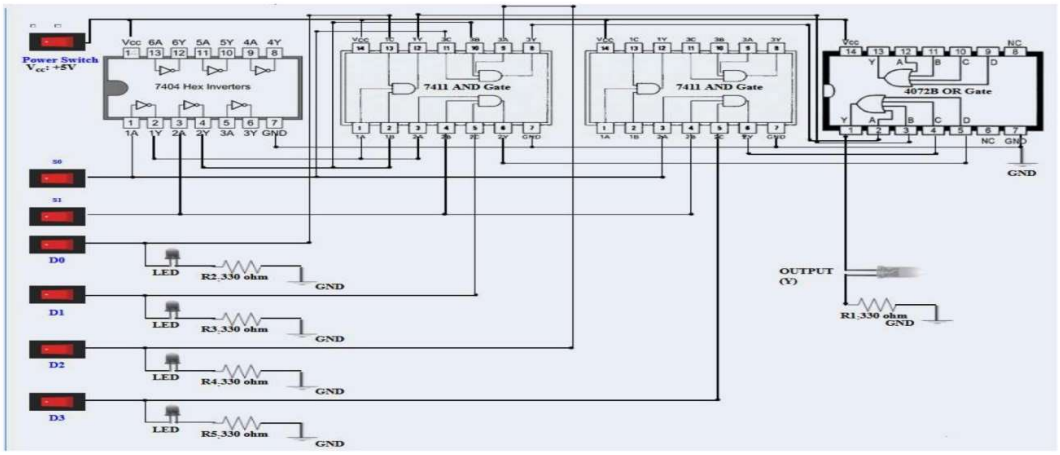


Figure. 8.3: Virtual Lab connections of 4:1 Multiplexer

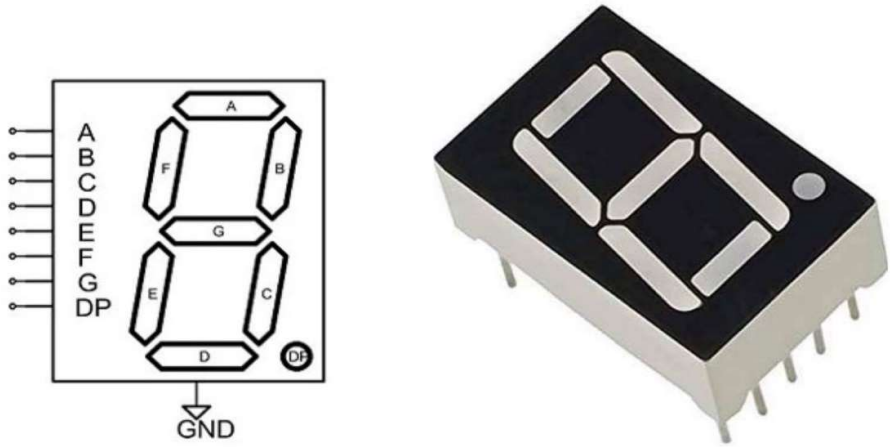


Figure 7.1: Seven segment display

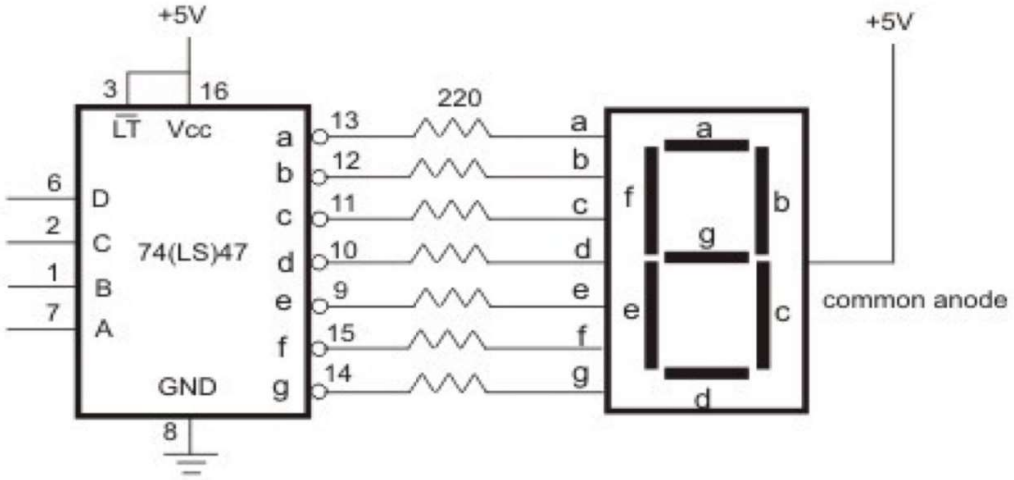


Figure 7.2: BCD to 7-segment display

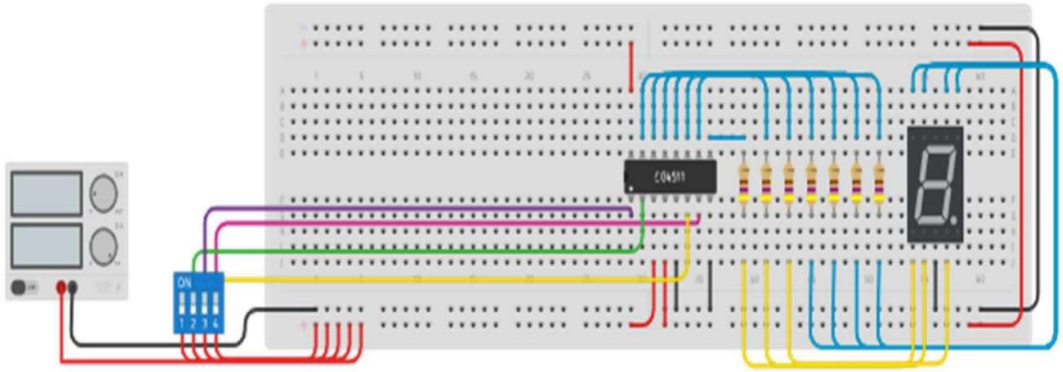


Figure 7.3: Breadboard connections

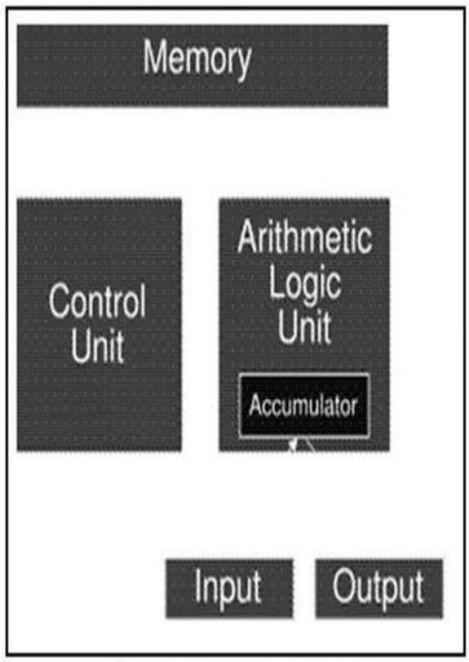


Figure 10.1: Central Processing Unit

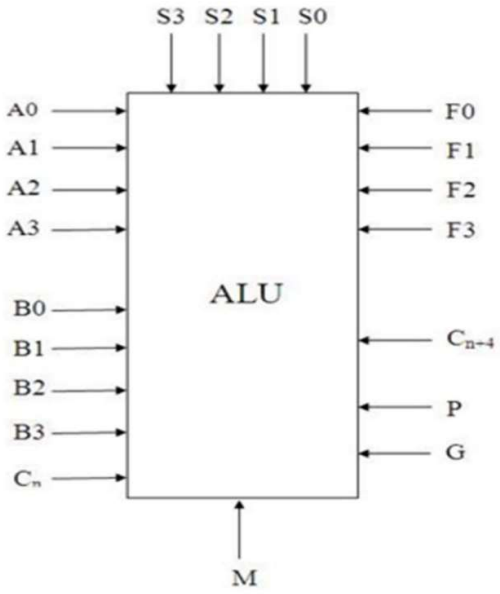


Figure 10.2: Functional representation of ALU

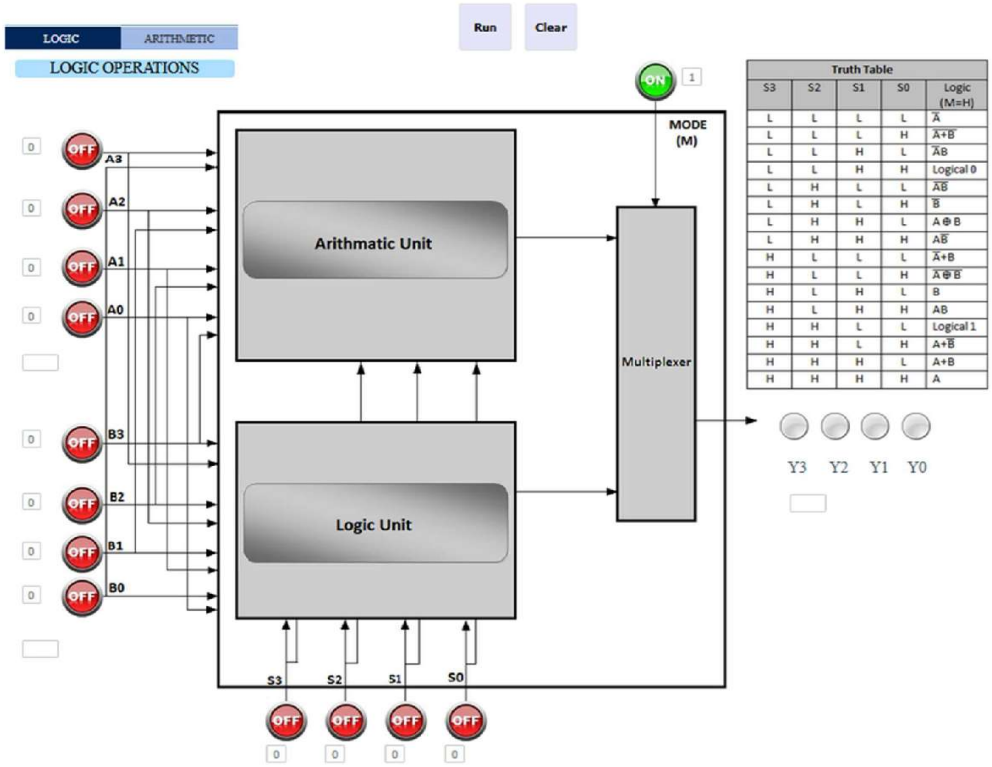
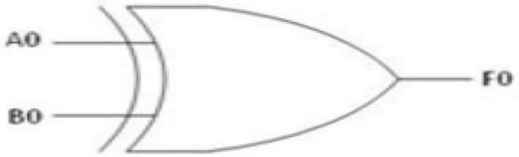


Figure 10.3: Simulation model for Logic Operations



Inputs		Output
A0	B0	F0
0	0	0
0	1	1
1	0	1
1	1	0

Figure 10.4: Ex-OR Logic

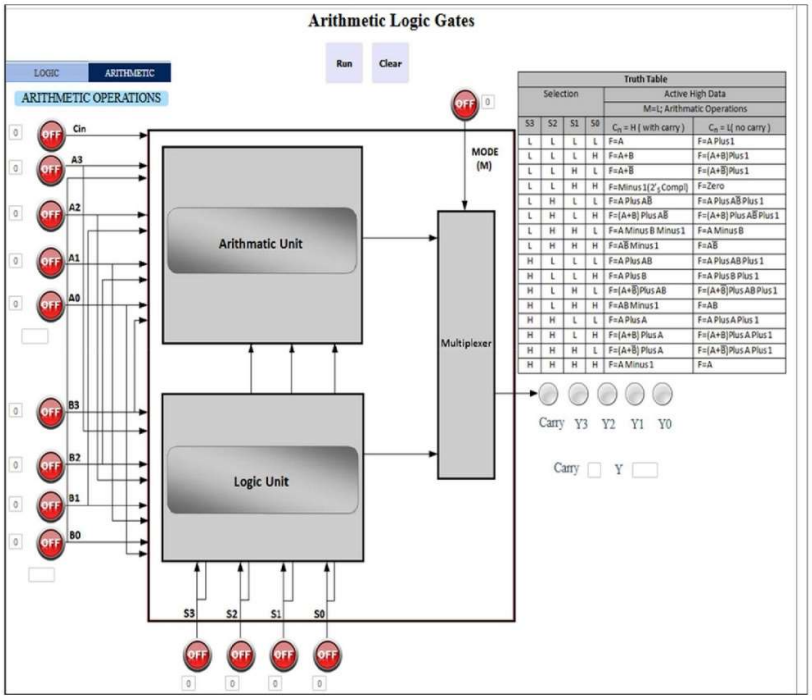


Figure 10.5: Simulation model for Arithmetic and Logic Operations

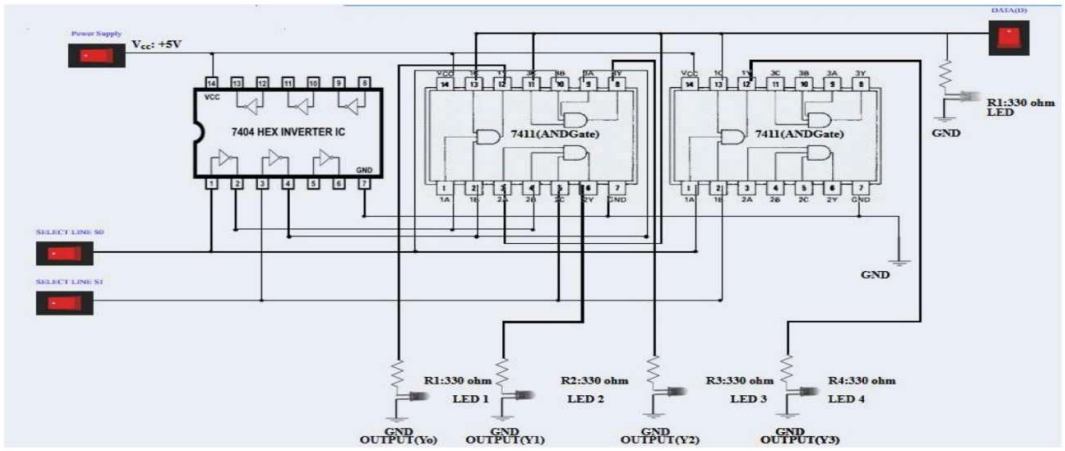


Figure. 8.4: Virtual Lab connections of 1:4 Demultiplexer

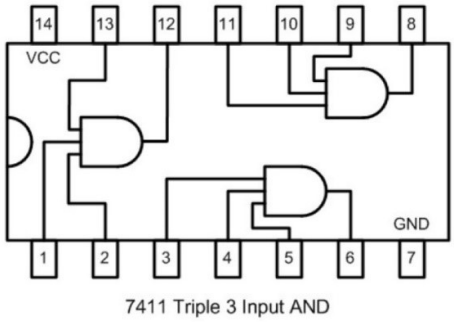


Figure. 8.5 Pin diagrams of IC 7411(3 input AND gate)

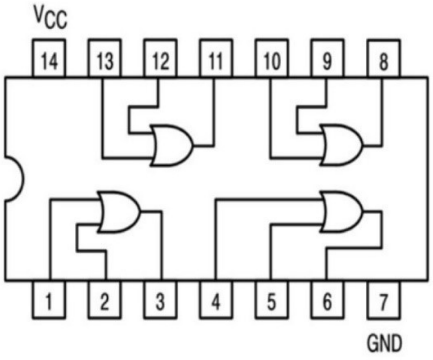


Figure. 8.6 Pin diagrams of IC 7432 (3 input OR gate)

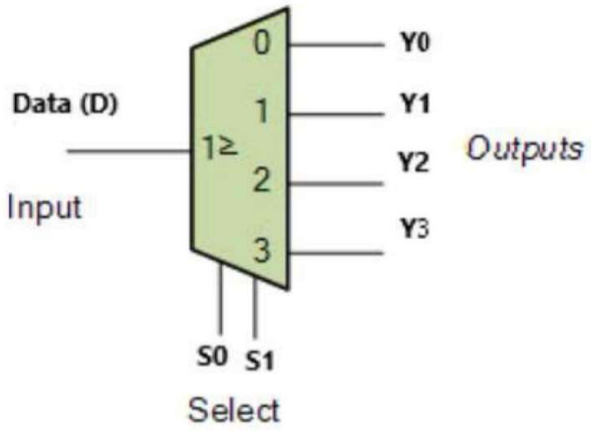


Figure. 8.2 Block diagram for 1:4 demultiplexer

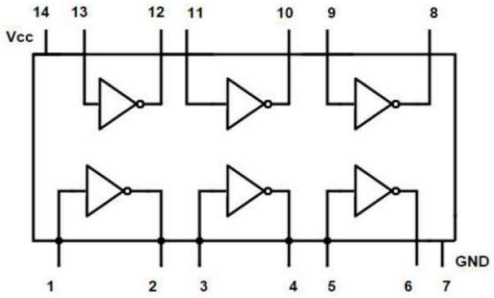


Figure. 8.7 Pin diagrams of IC 7400 (3 input NOT gate)

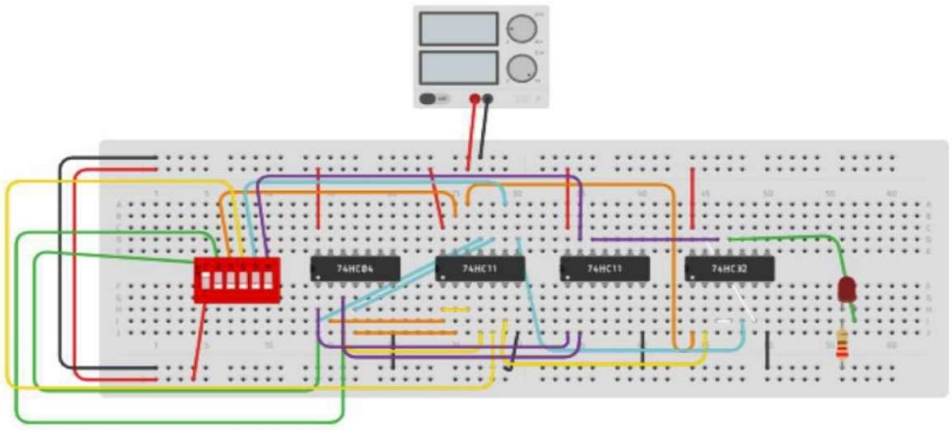


Figure 8.8: Breadboard connections of 4:1 Multiplexer

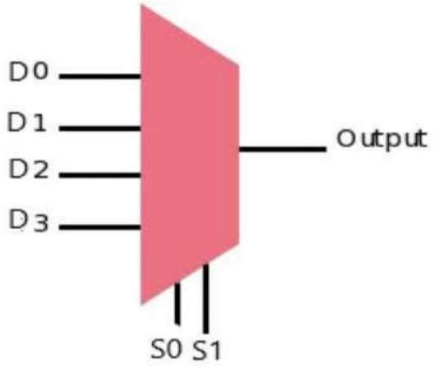


Figure. 8.1 Block diagram for 4:1 multiplexer

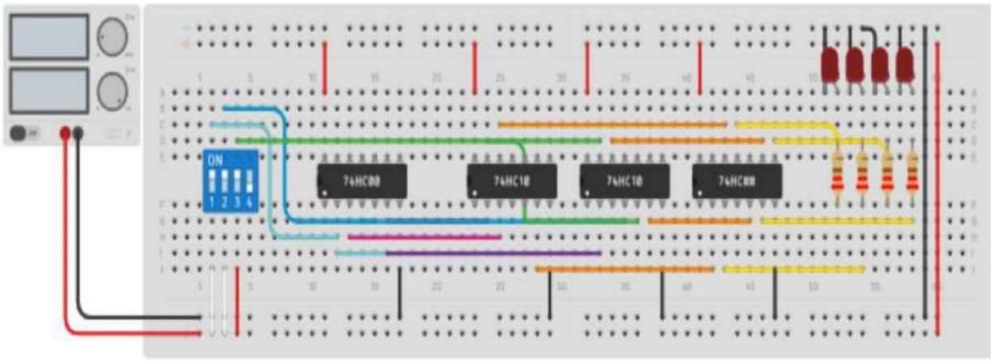


Figure 8.9: Breadboard connections of 1:4 Demultiplexer