数字逻辑与处理器基础实验

Quartus II使用说明

提 纲

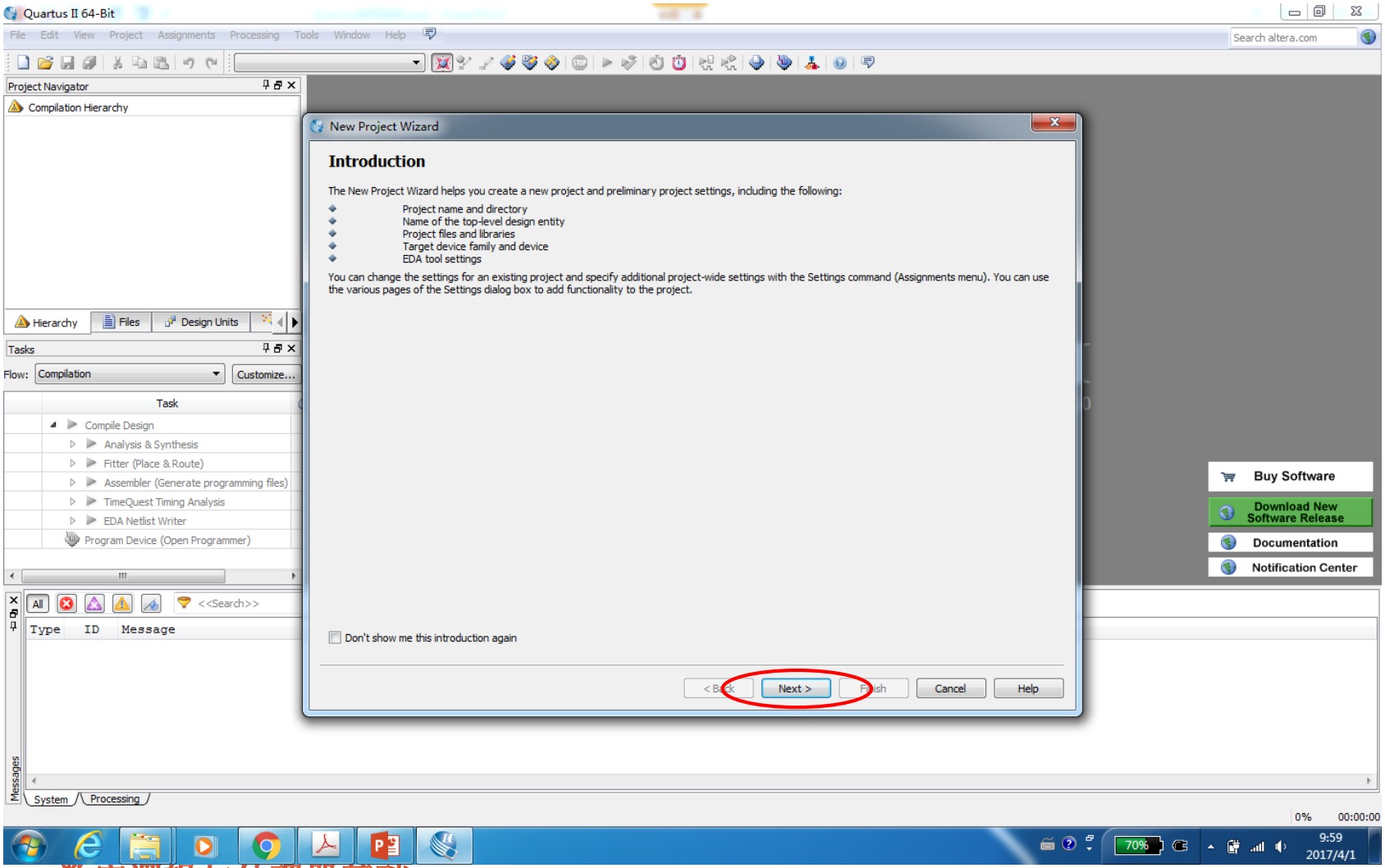
- *新建工程*
- 设置Unused Pin类型
- 编译、绑定管脚
- 程序下载
- TimeQuest时序约束

启动Quartus软件

新建工程

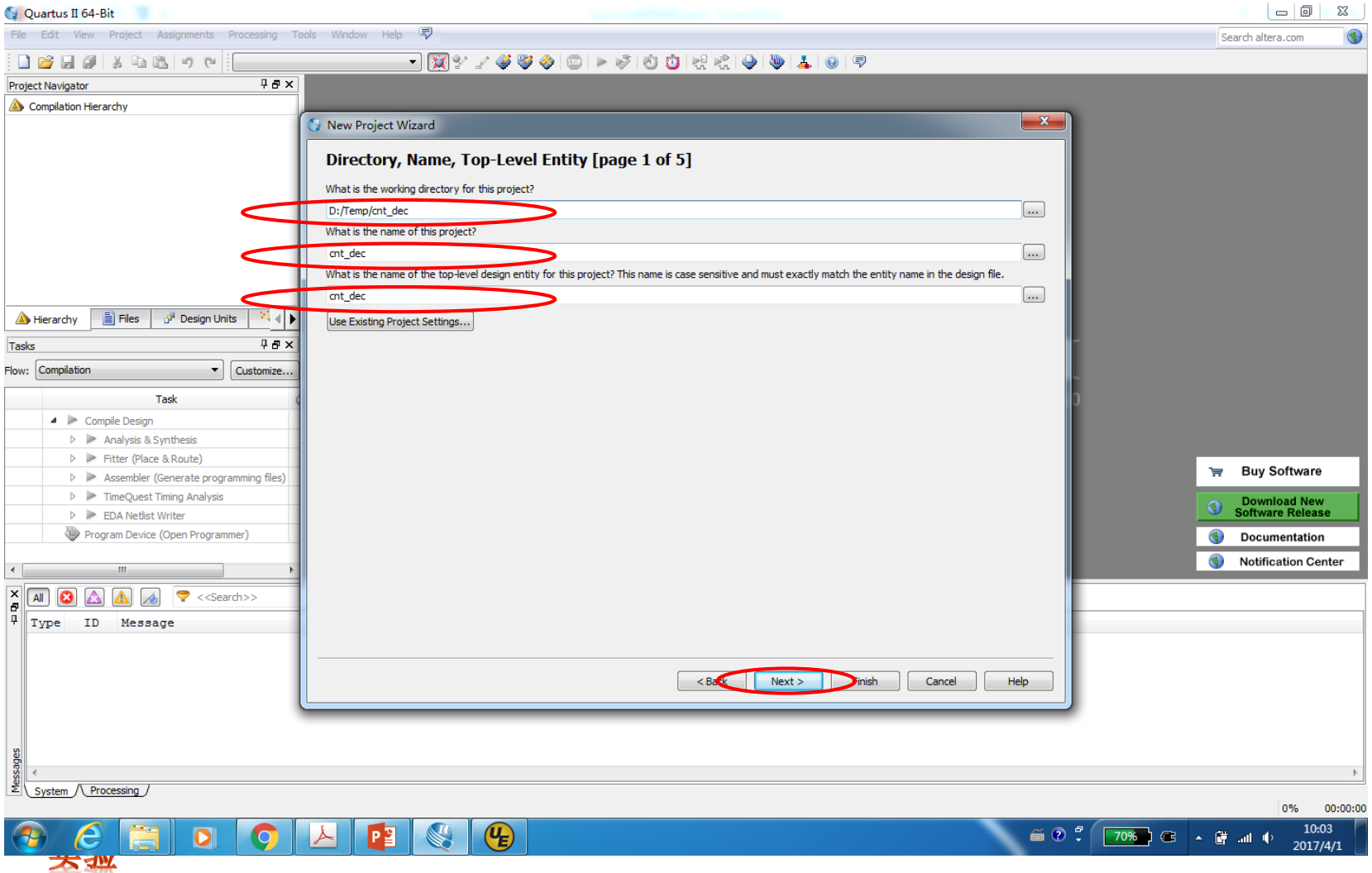

Quartus II 64-Bit
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
ALTERA
QUARTUS® II
Version 13.0
Buy Software
Download New Software Release
Documentation
Notification Center
<<Search>>
Type ID Message
Messages
System Processing
Starts the New Project Wizard
0% 00:00:00
70%
9:57
2017/4/1

新建工程


Quartus II 64-Bit
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator
Compilation Hierarchy
Hierarchy Files Design Units
Tasks
Flow: Compilation Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
New Project Wizard
Introduction
The New Project Wizard helps you create a new project and preliminary project settings, including the following:
Project name and directory
Name of the top-level design entity
Project files and libraries
Target device family and device
EDA tool settings
You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.
Don't show me this introduction again
< Back
Next >
Finish
Cancel
Help
Buy Software
Download New Software Release
Documentation
Notification Center
Type ID Message
Messages
System Processing
0% 00:00:00
70%
9:59
2017/4/1

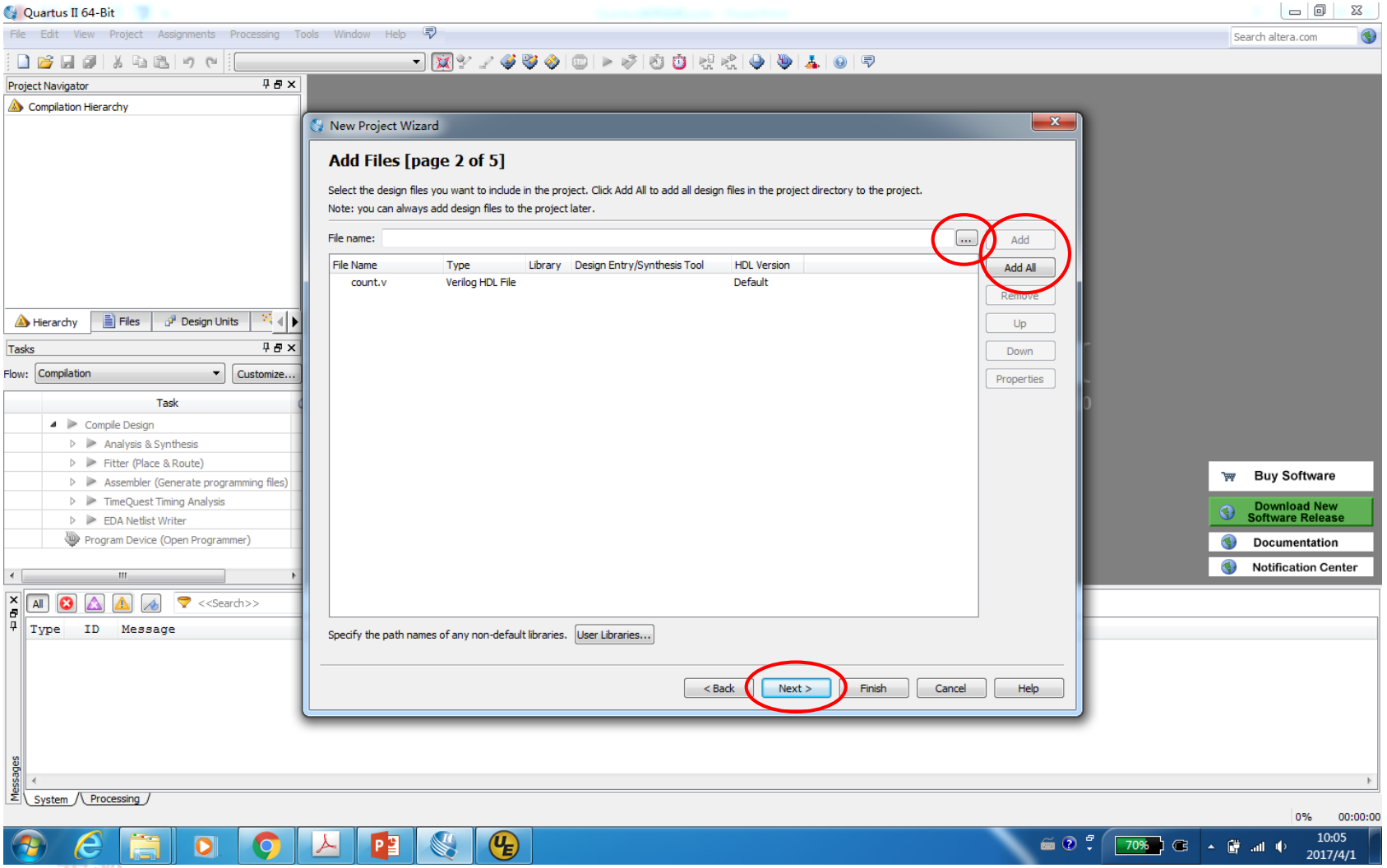
新建工程

设置工程路径、工程名称和顶层设计模块名，之后单击next



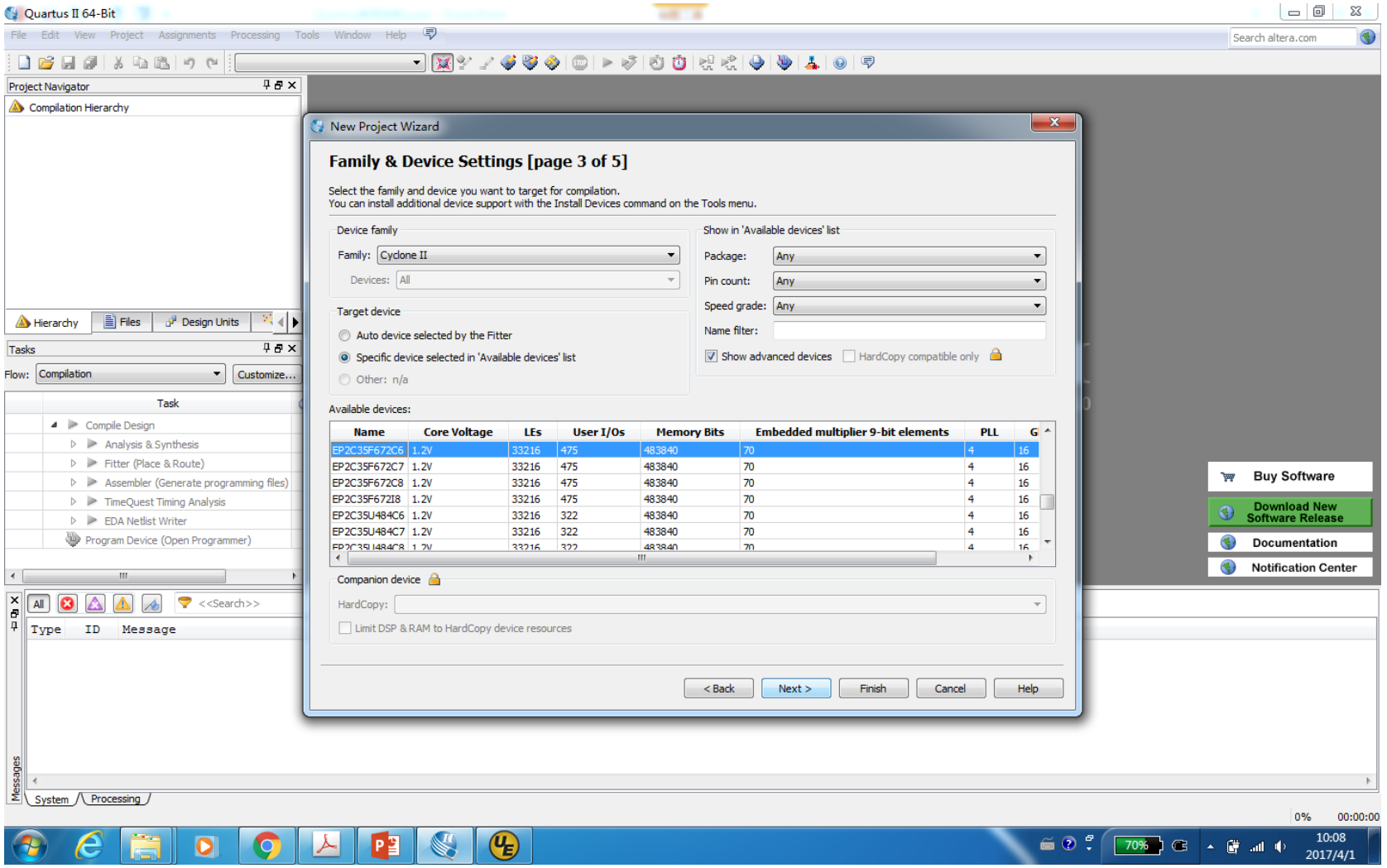
新建工程

添加verilog文件，之后next



新建工程

设置FPGA型号：EP2C35F672C6，之后next，直到finish



提 纲

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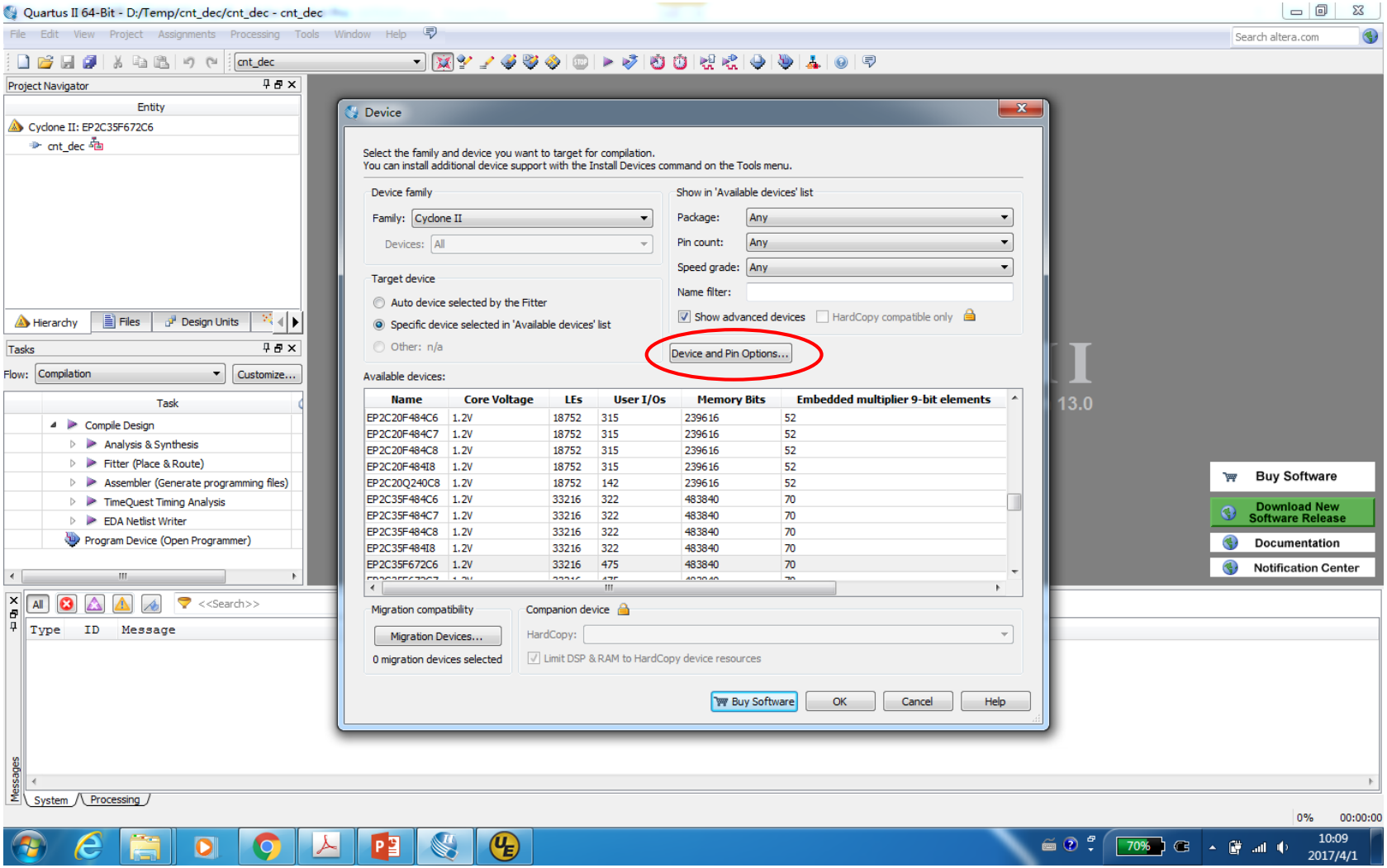
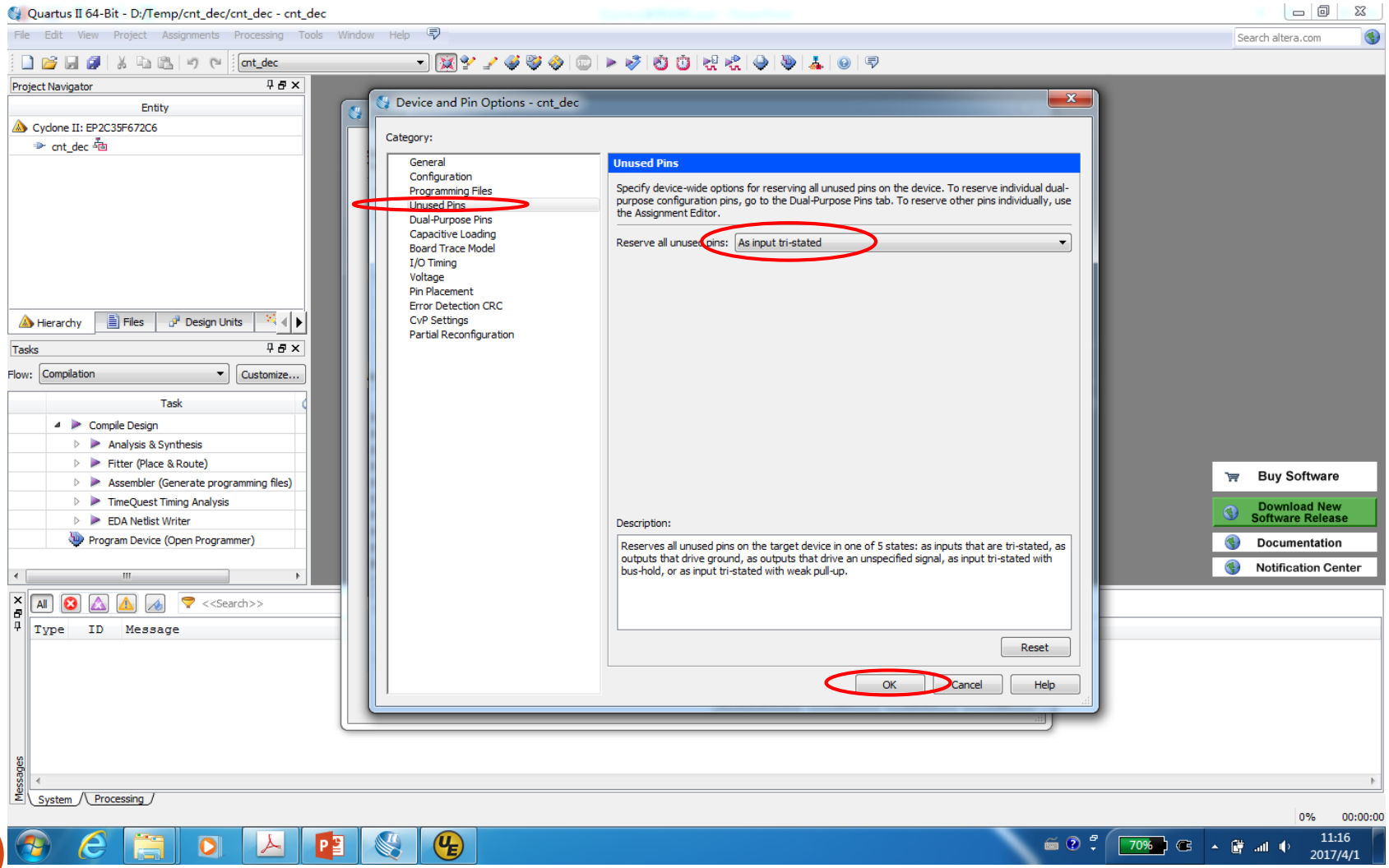
设置Unused Pin类型

Assignment->Device，打开窗口，单击Device and Pin Options



设置Unused Pin类型

在Unused Pins标签下设置未用引脚为“As input tri-stated”，之后确定



提 纲

- 新建工程
- 设置Unused Pin类型
- ***编译、绑定管脚***
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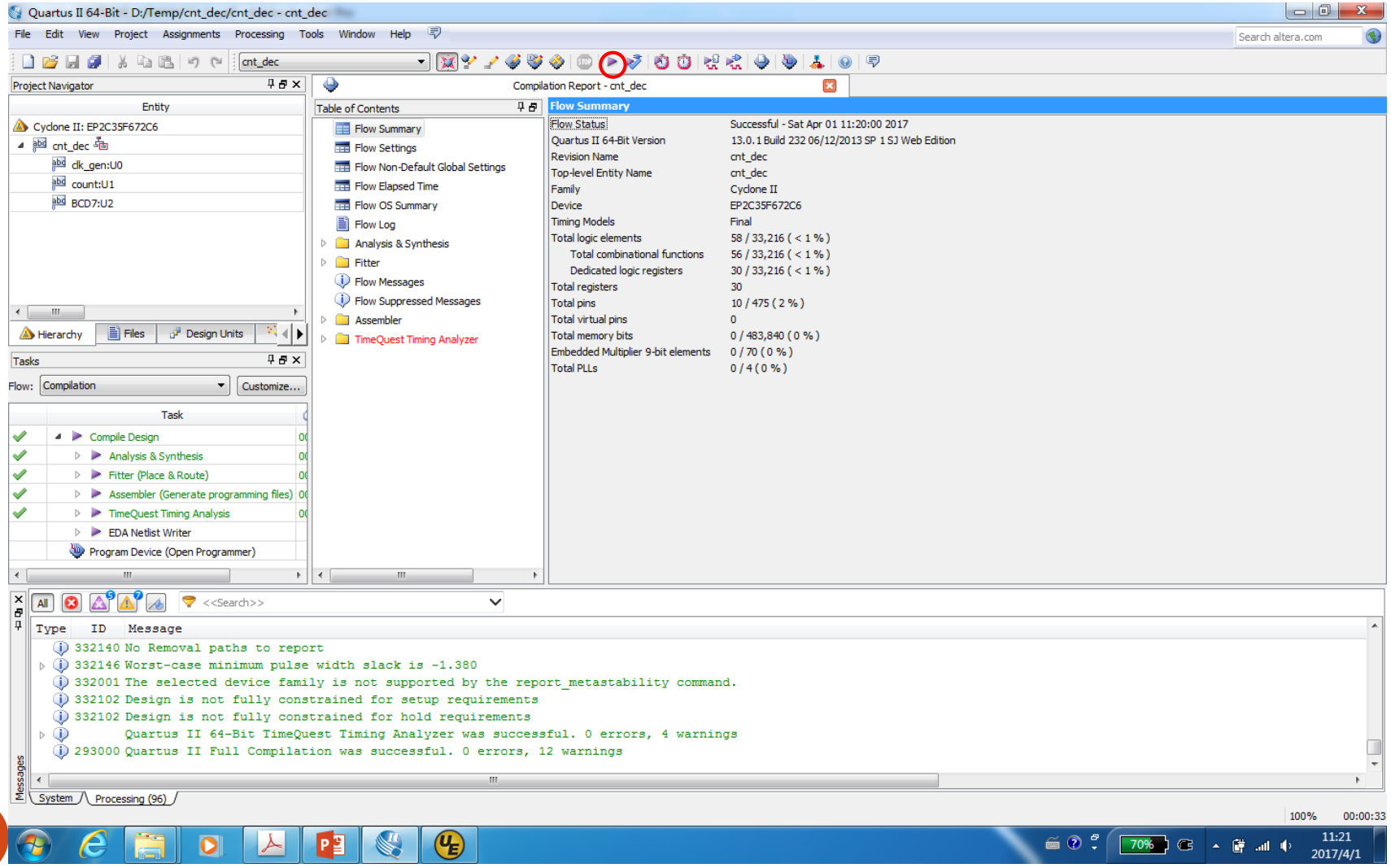
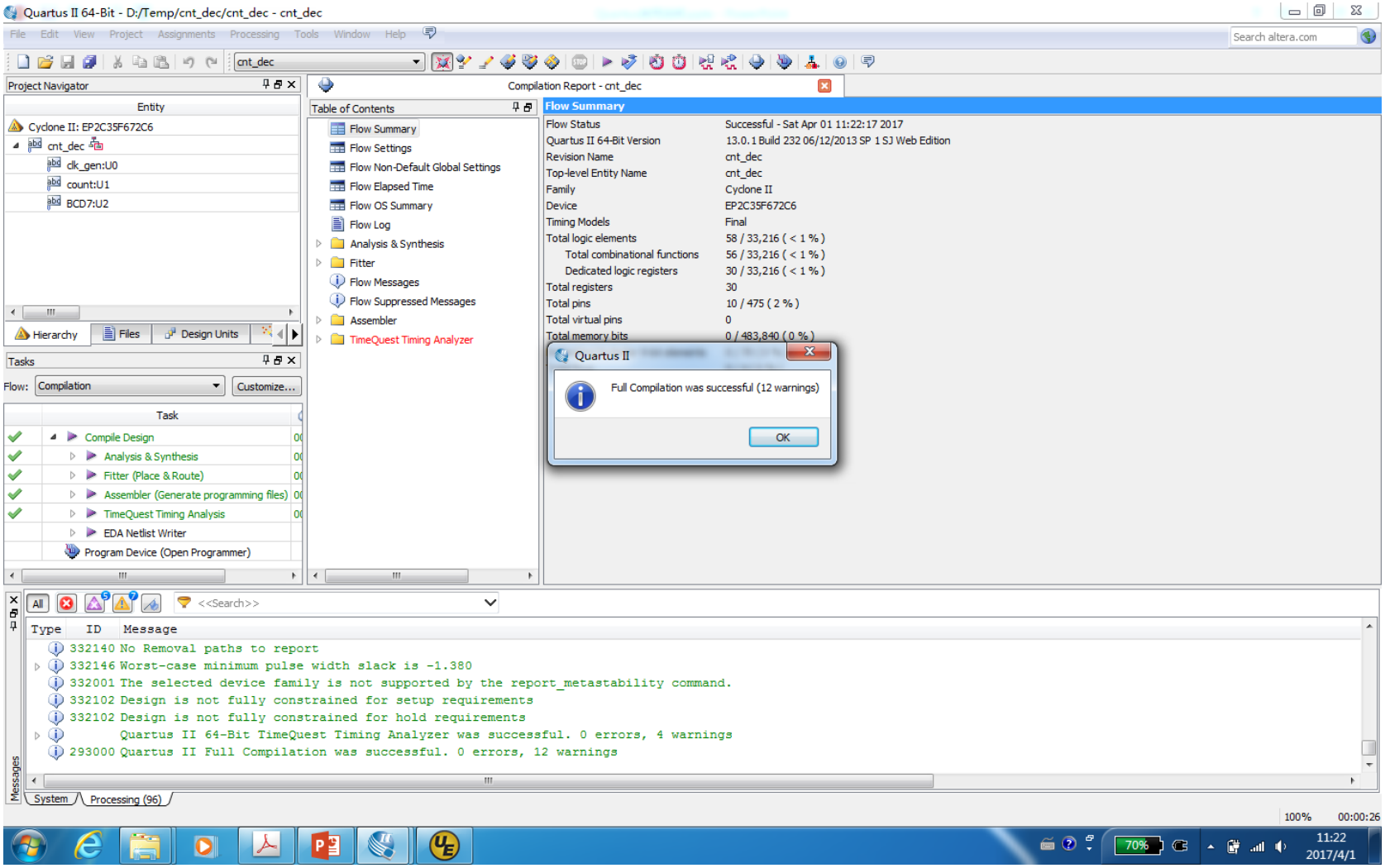
编译

单击Start Compilation按钮开始编译



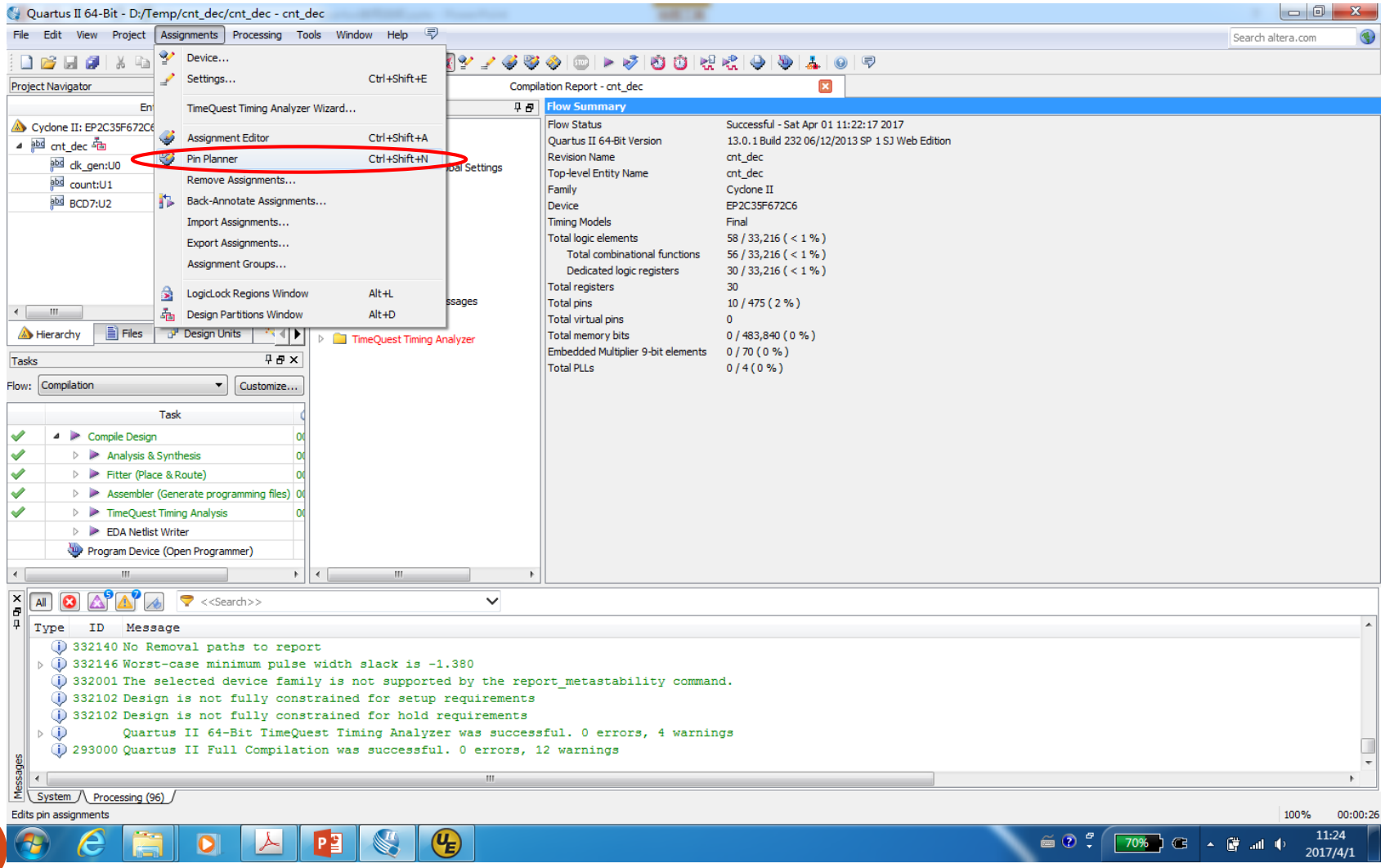
编译

编译完成显示如下


Quartus II 64-Bit - D:/Temp/cnt_dec/cnt_dec - cnt_dec
Project Navigator
Entity
Cyclone II: EP2C35F672C6
cnt_dec
clk_gen:U0
count:U1
BCD7:U2
Compilation Report - cnt_dec
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Flow Messages
Flow Suppressed Messages
Assembler
TimeQuest Timing Analyzer
Flow Summary
Flow Status Successful - Sat Apr 01 11:22:17 2017
Quartus II 64-Bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name cnt_dec
Top-level Entity Name cnt_dec
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 58 / 33,216 (< 1 %)
Total combinational functions 56 / 33,216 (< 1 %)
Dedicated logic registers 30 / 33,216 (< 1 %)
Total registers 30
Total pins 10 / 475 (2 %)
Total virtual pins 0
Total memory bits 0 / 483,840 (0 %)
Quartus II
Full Compilation was successful (12 warnings)
OK
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Type ID Message
332140 No Removal paths to report
332146 Worst-case minimum pulse width slack is -1.380
332001 The selected device family is not supported by the report_metastability command.
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
System
Processing (96)
100%
00:00:26
11:22
2017/4/1

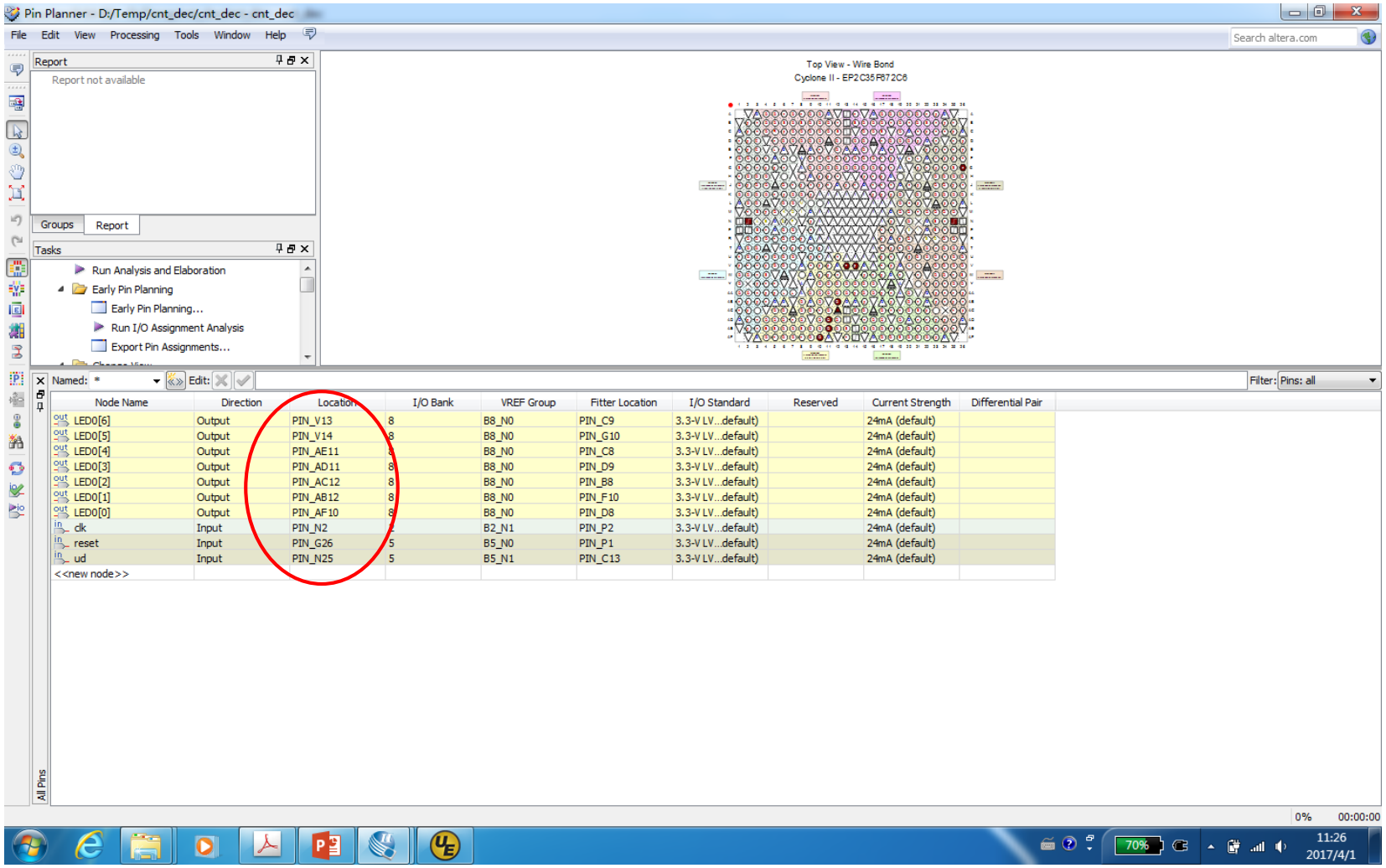
引脚绑定-方法1

编译完成后，点击Assignment->Pin Planner



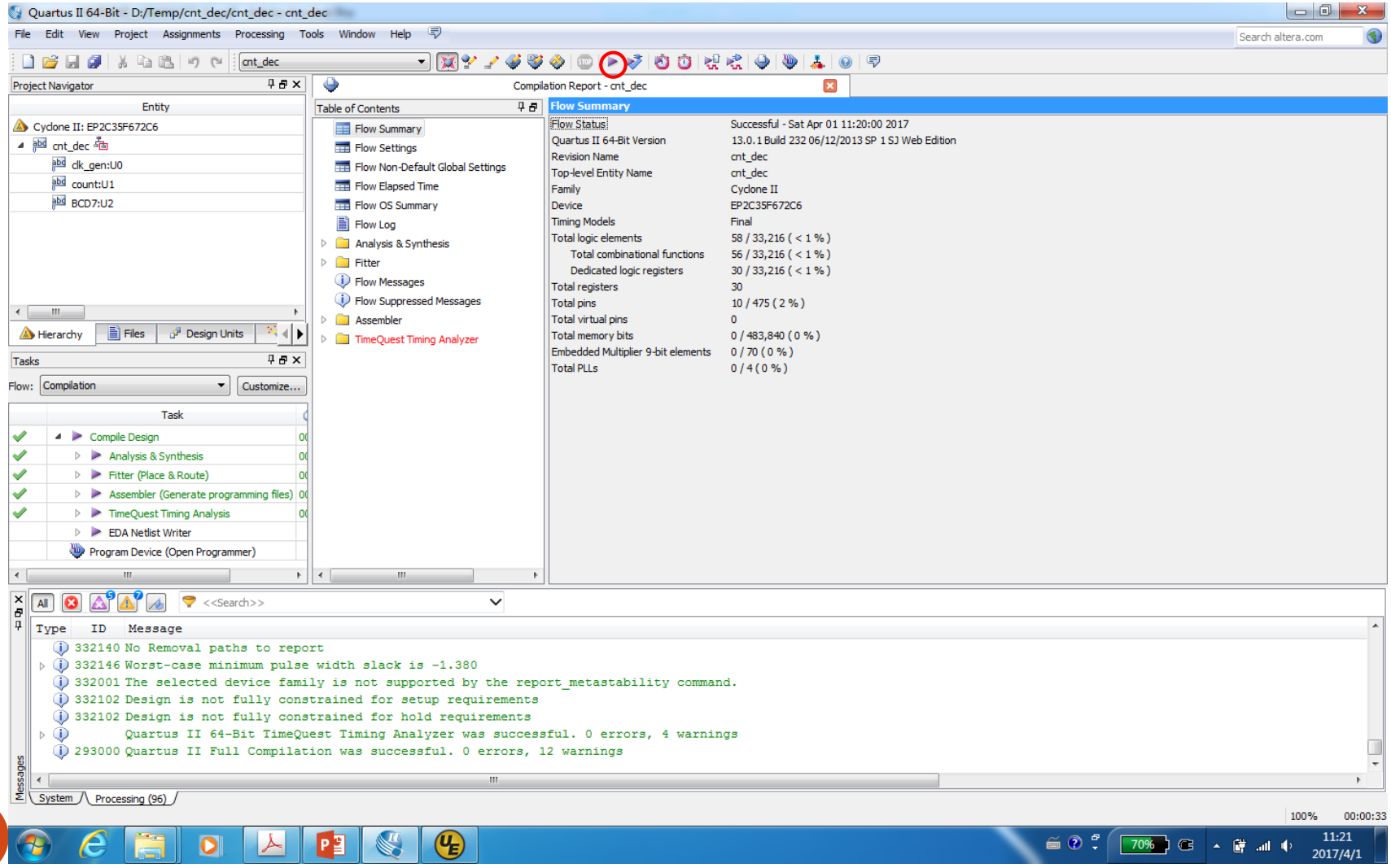
引脚绑定-方法1

在Pin Planner窗口，每一个引脚对应的Location位置输入引脚号，“PIN_”不用输入，会自动补上



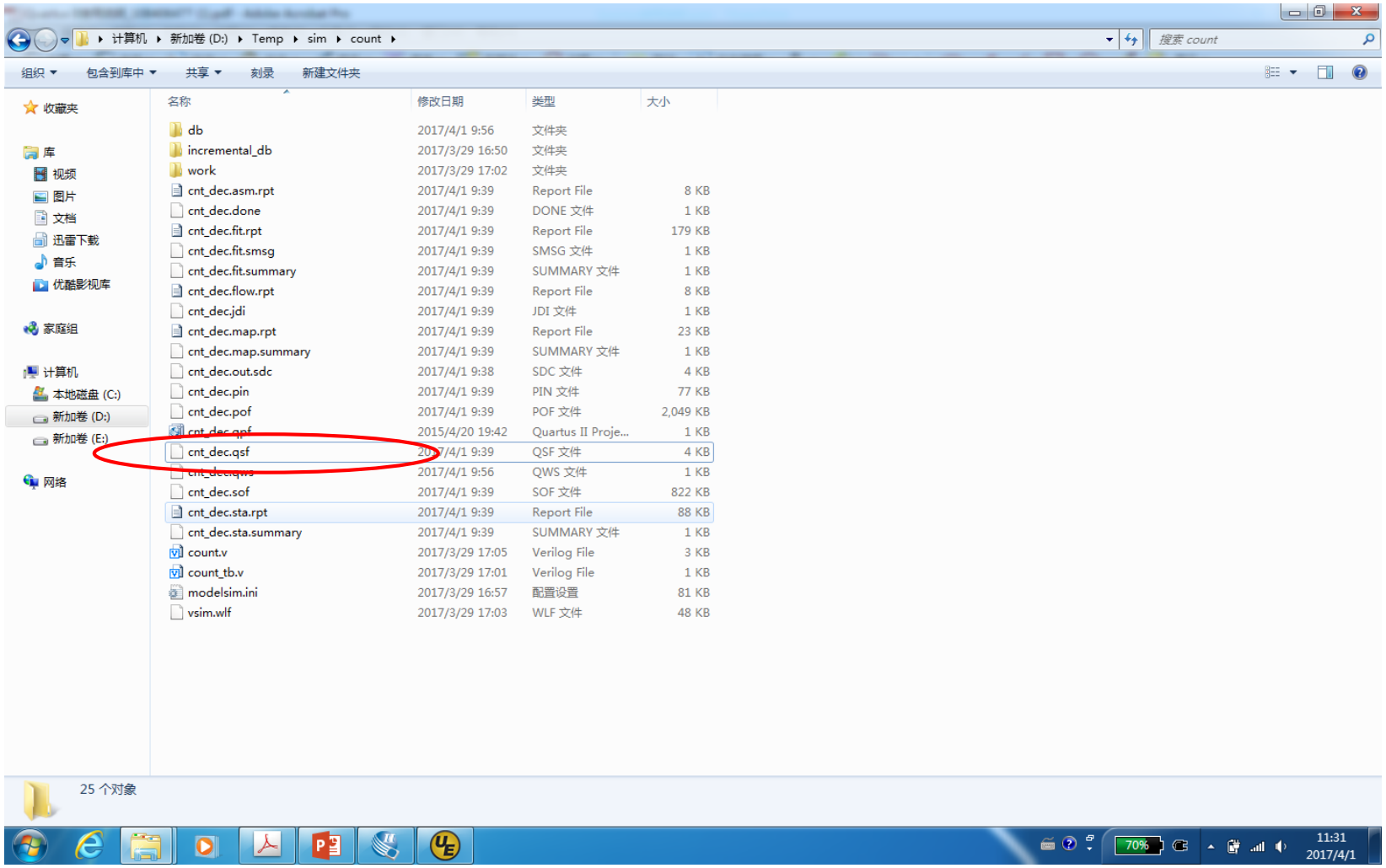
引脚绑定-方法1

引脚制定完成后，**必须重新编译工程**



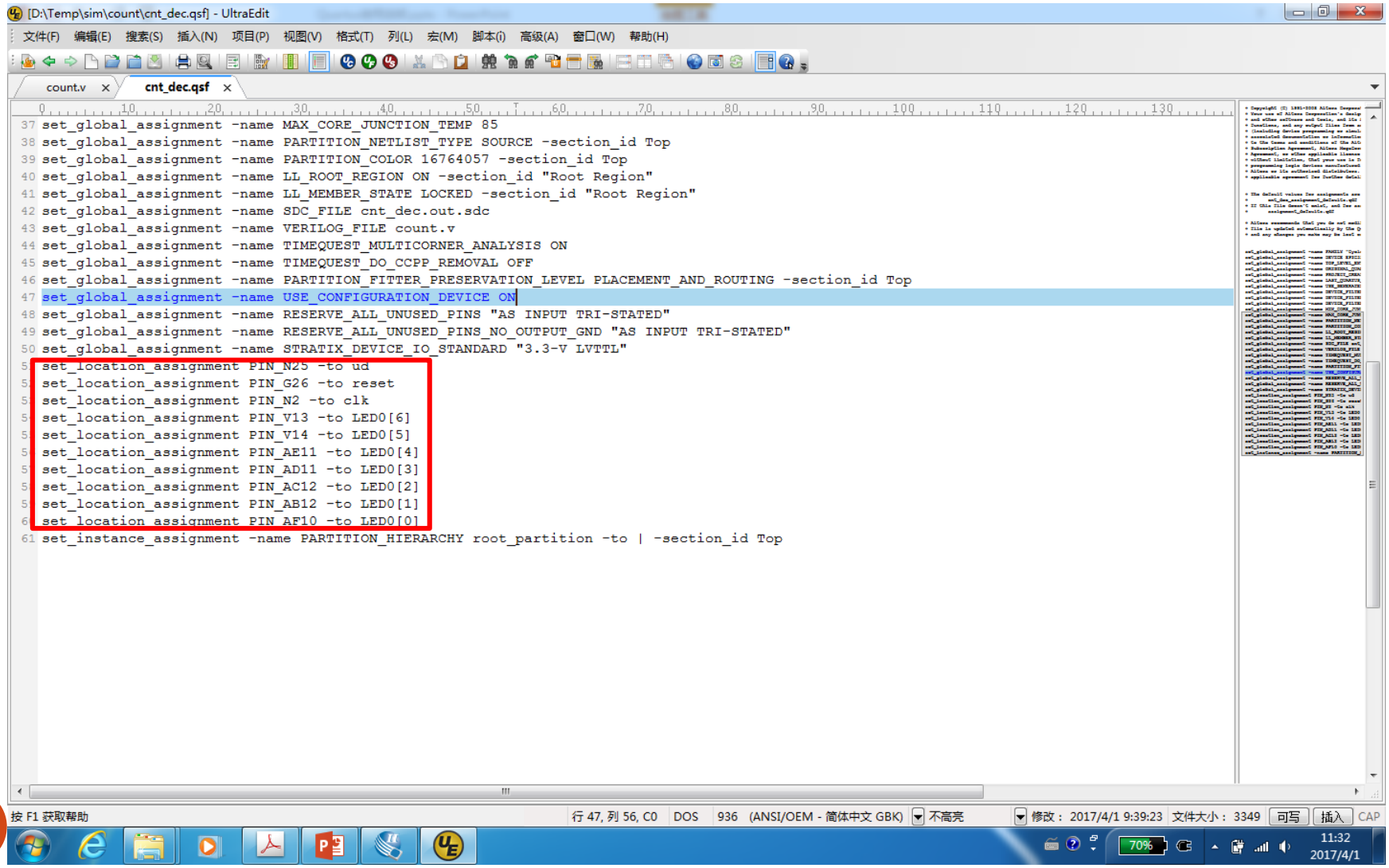
引脚绑定-方法2

在QuartusII工程所在目录下，找到扩展名为.qsf的文件，其文件名和工程名相同



引脚绑定-方法2

使用文本编辑器打开.qsf文件，可按如下格式指定引脚



引脚绑定-方法2

- 使用.qsf文件指定引脚的方法，可在新建工程完成之后直接进行，不需要先编译再修改qsf文件
- 通过qsf文件指定完引脚后，**必须重新编译工程，才能使引脚指定生效**

提 纲

- 新建工程
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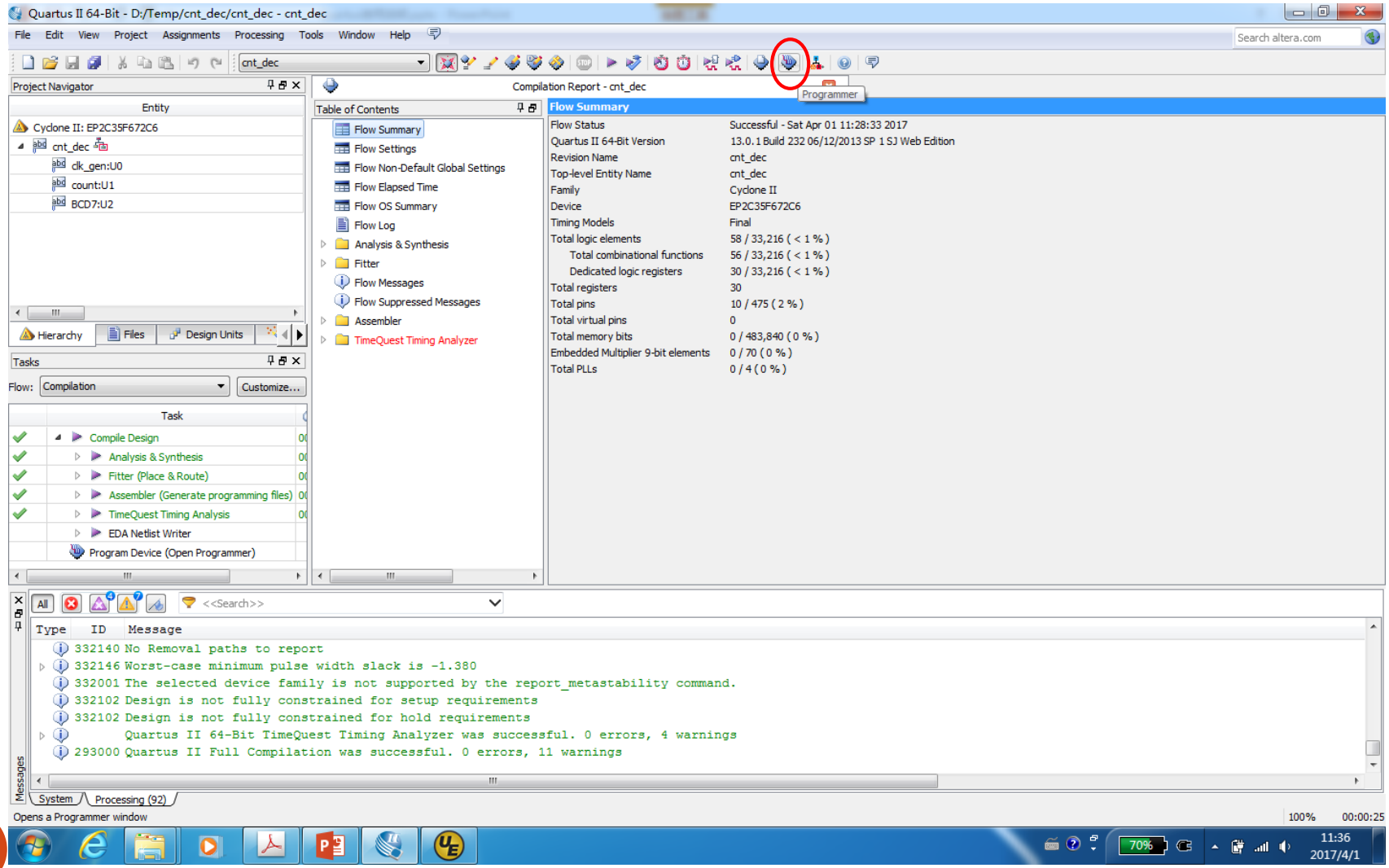
- *程序下载*
- TimeQuest时序约束

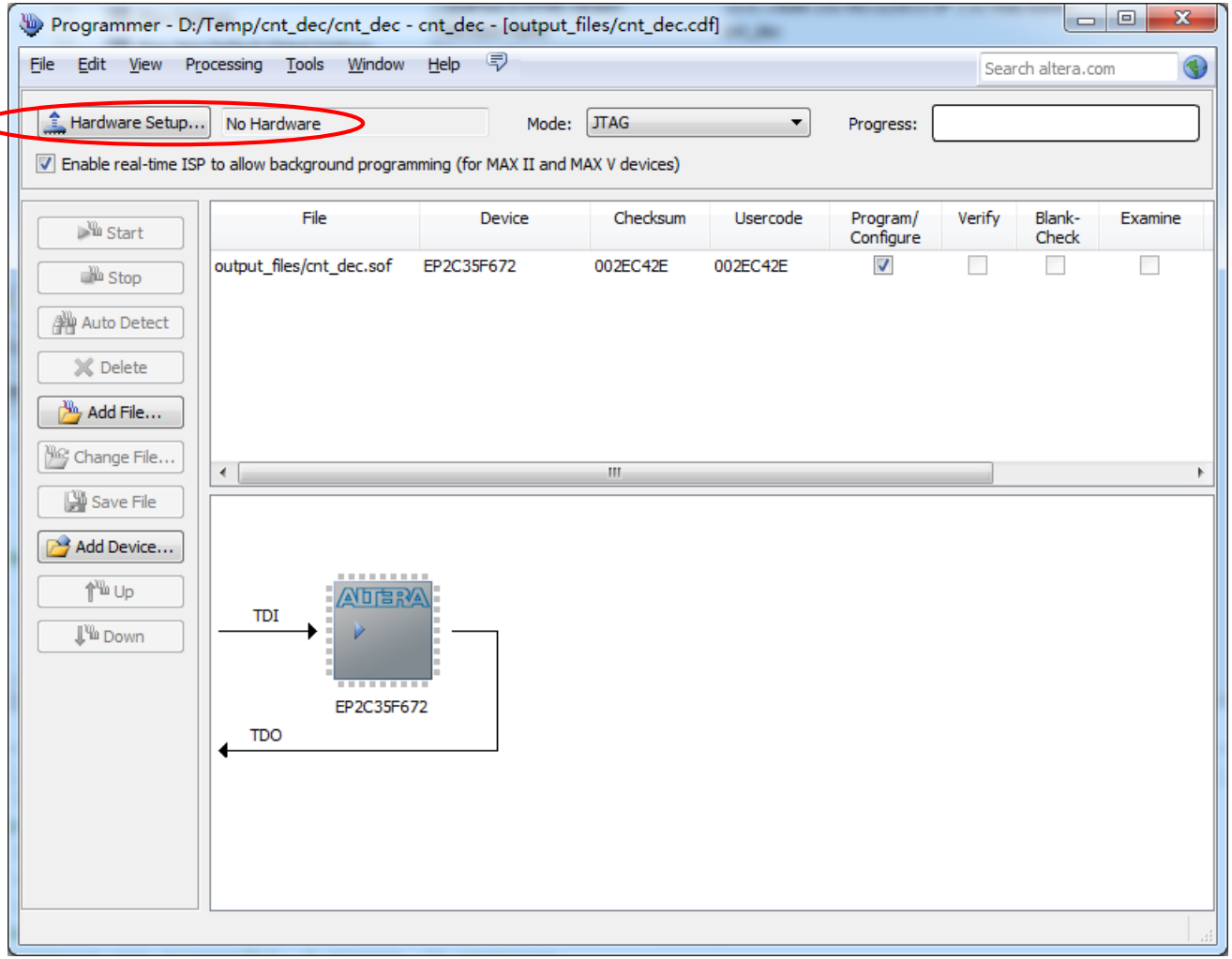
程序下载

单击programmer按钮



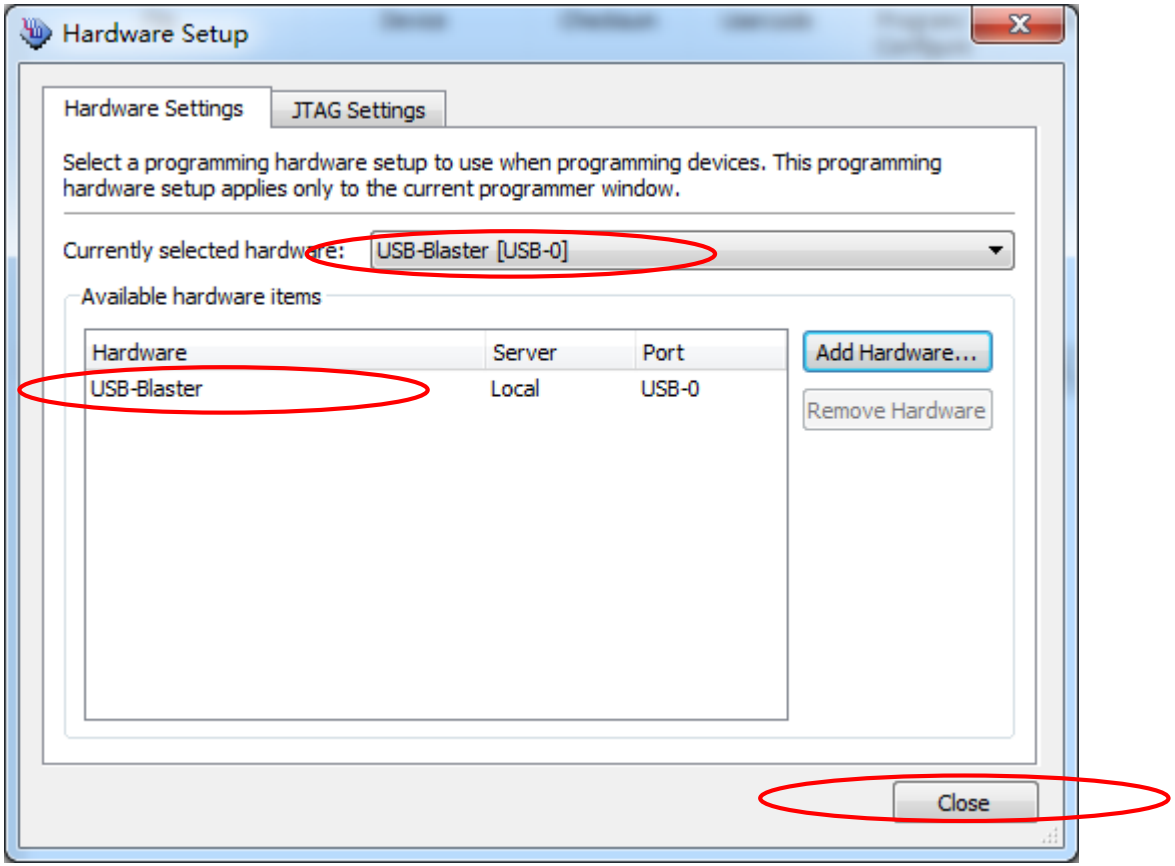
程序下载

单击Hardware Setup按钮，设置下载线



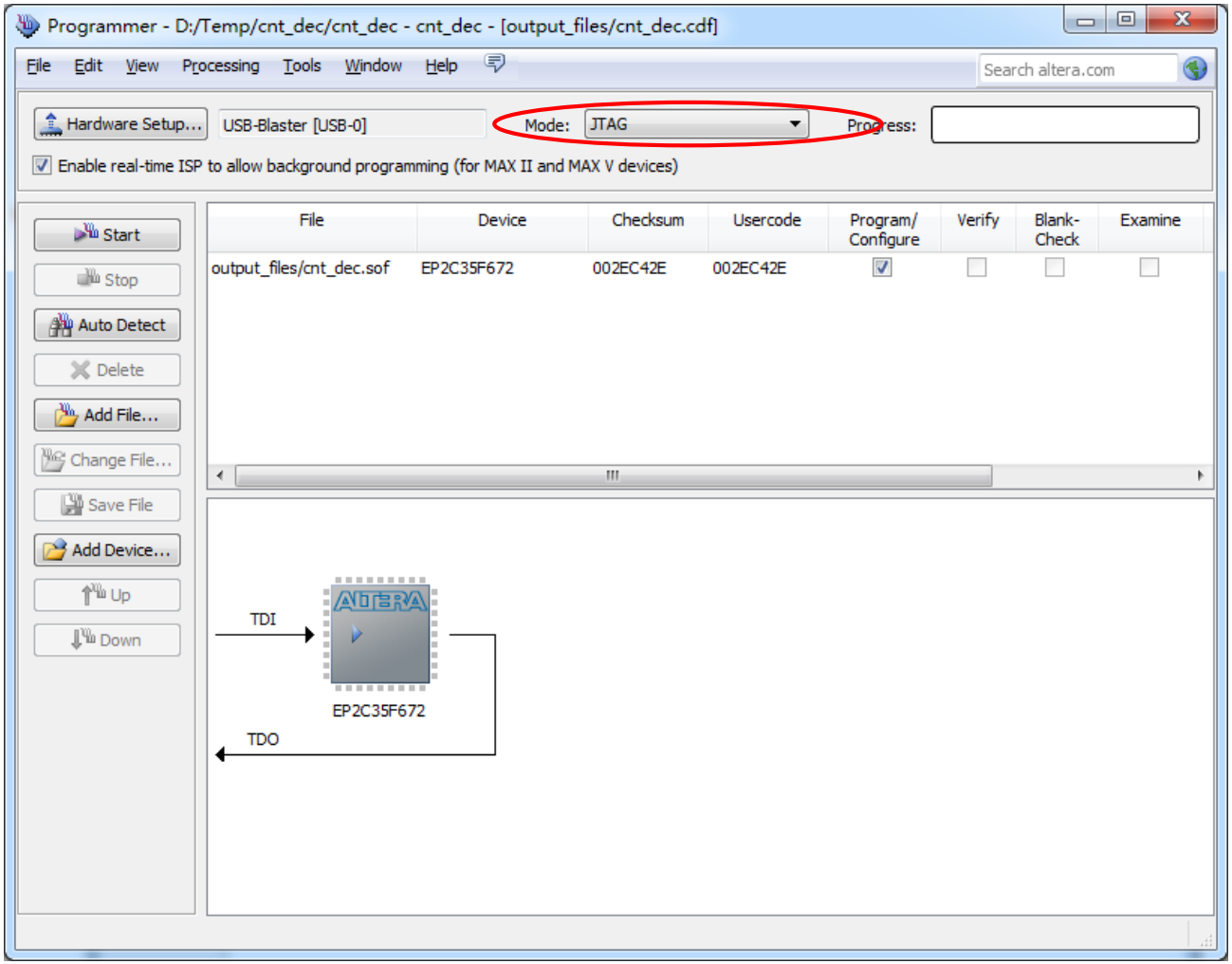
程序下载

在Hardware Setup窗口，设置selected hardware为USB-Blaster，之后close



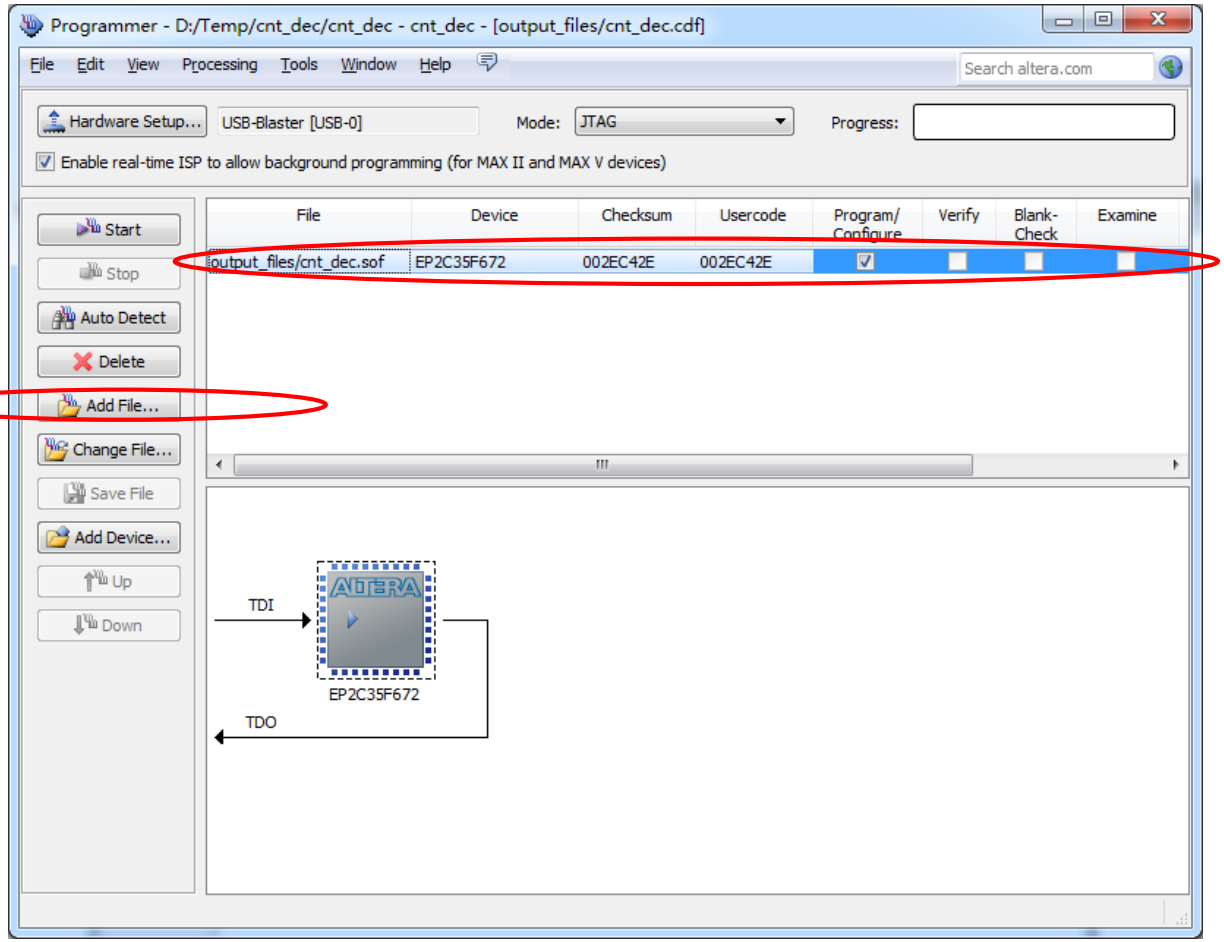
程序下载

选择下载模式为JTAG



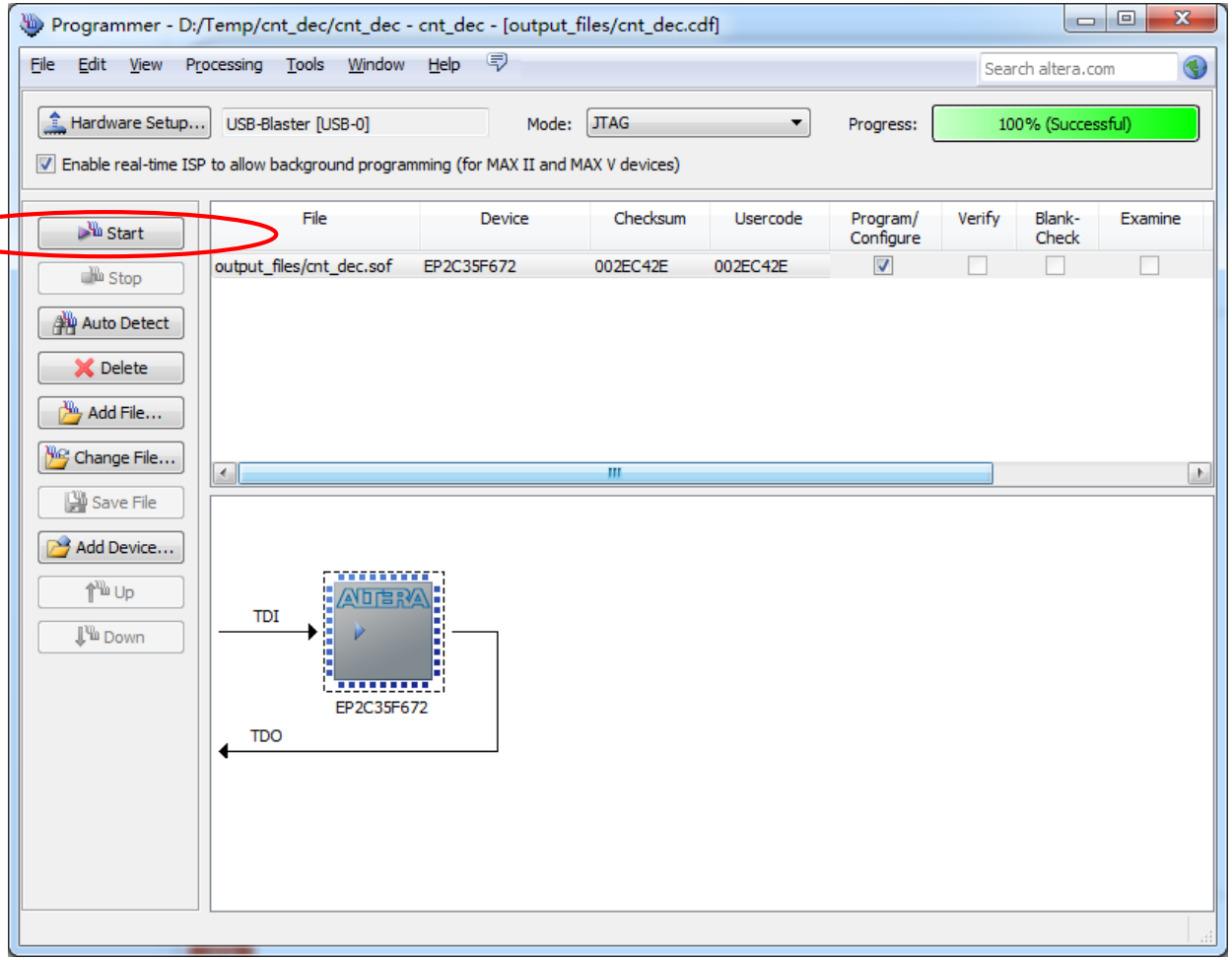
程序下载

添加*.sof下载文件，programmer窗口缺省会添加当前工程的sof文件，也可手动添加文件



程序下载

单击Start按钮开始下载



提 纲

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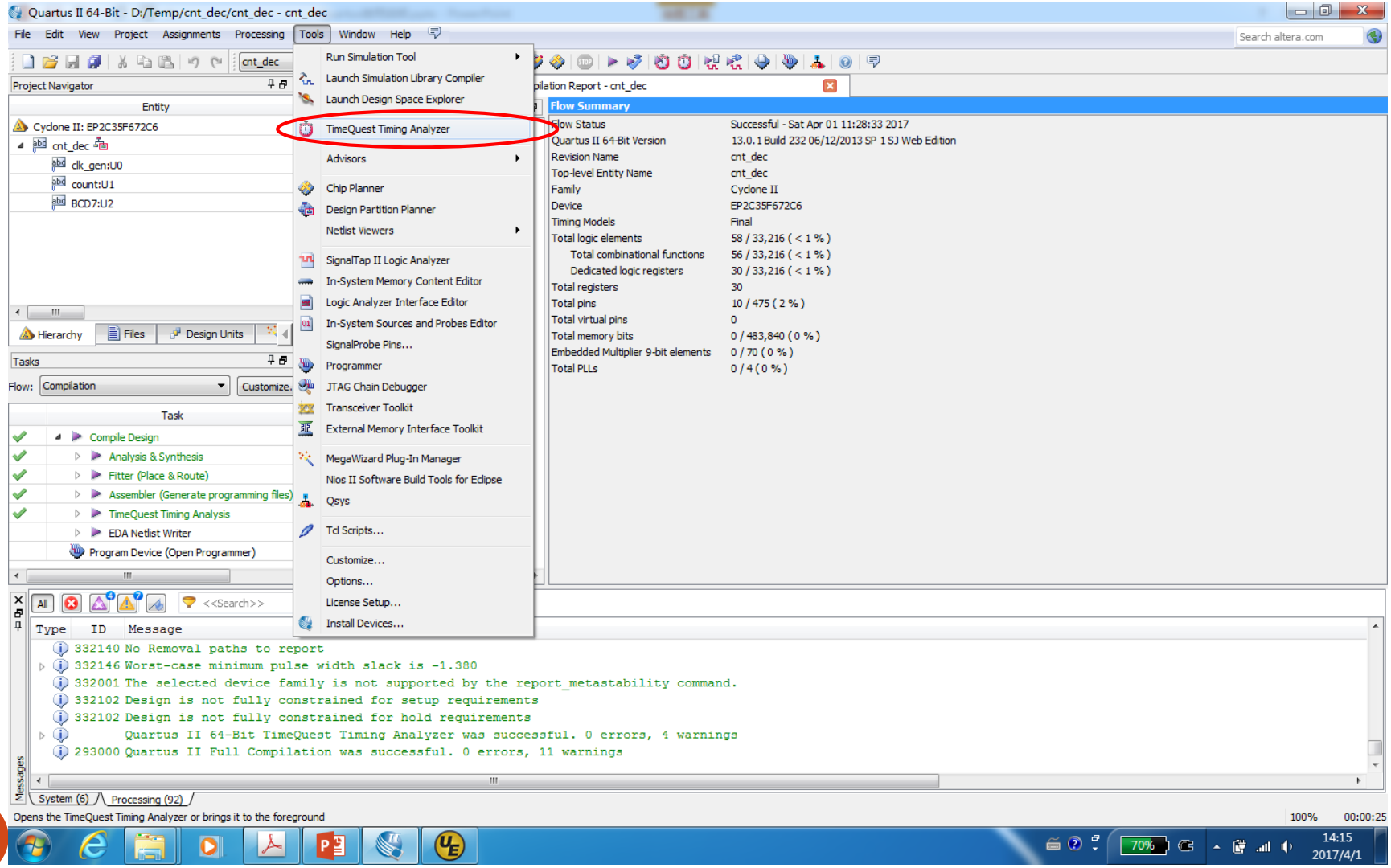
- *TimeQuest时序约束*

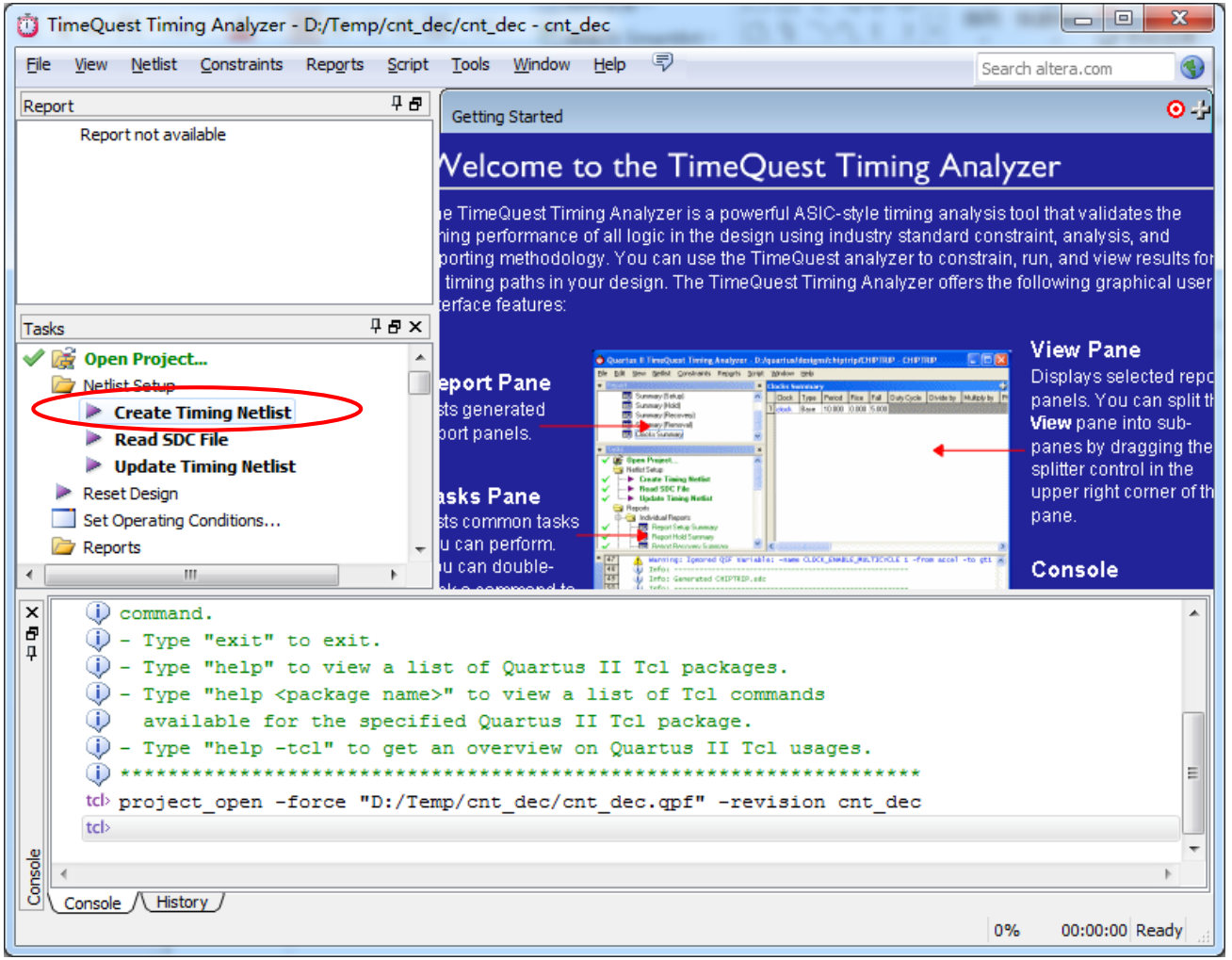
TimeQuest时序约束

单击Tools->TimeQuest Timing Analyzer，启动TimeQuest



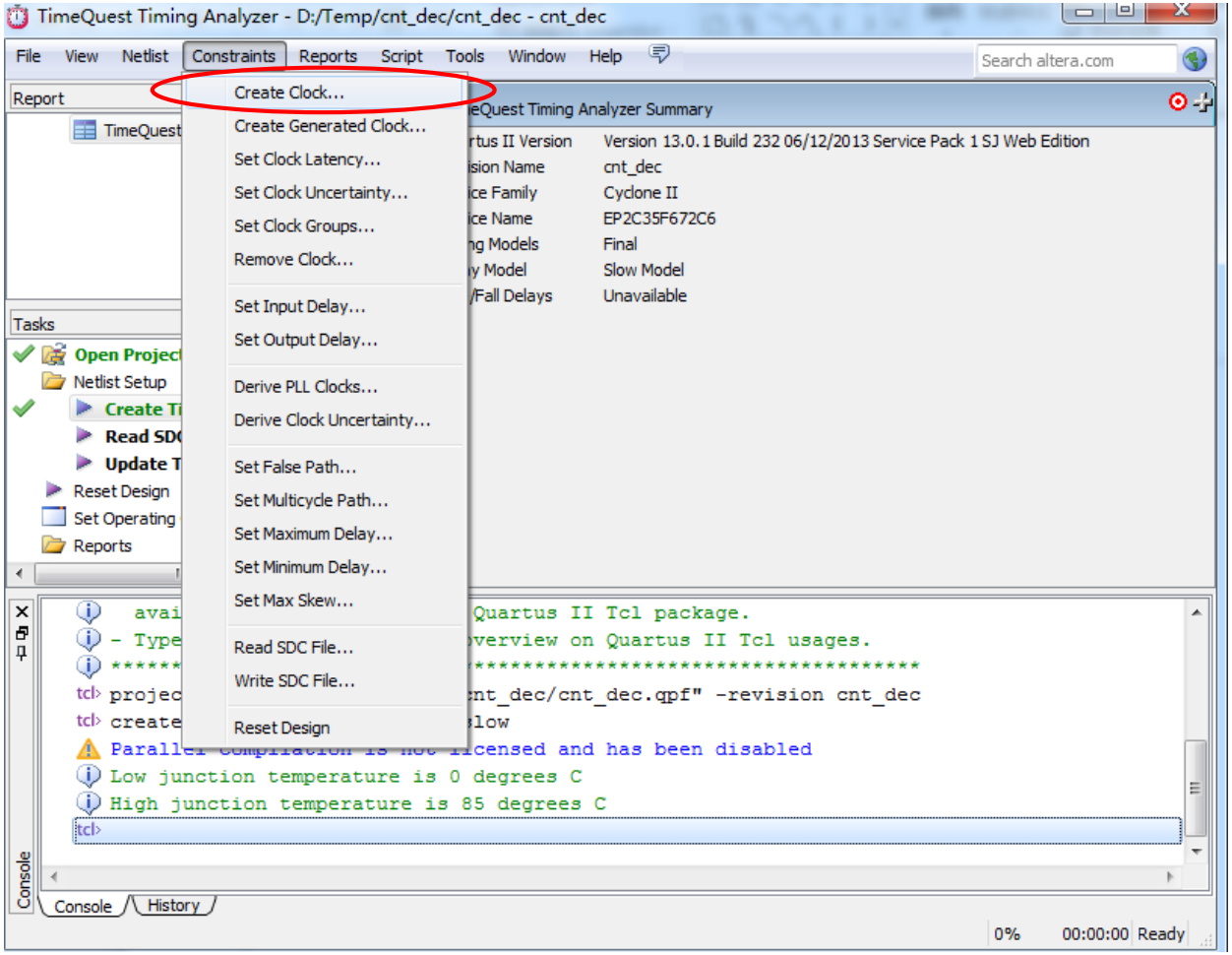
TimeQuest时序约束

双击Tasks->Create Timing Netlist



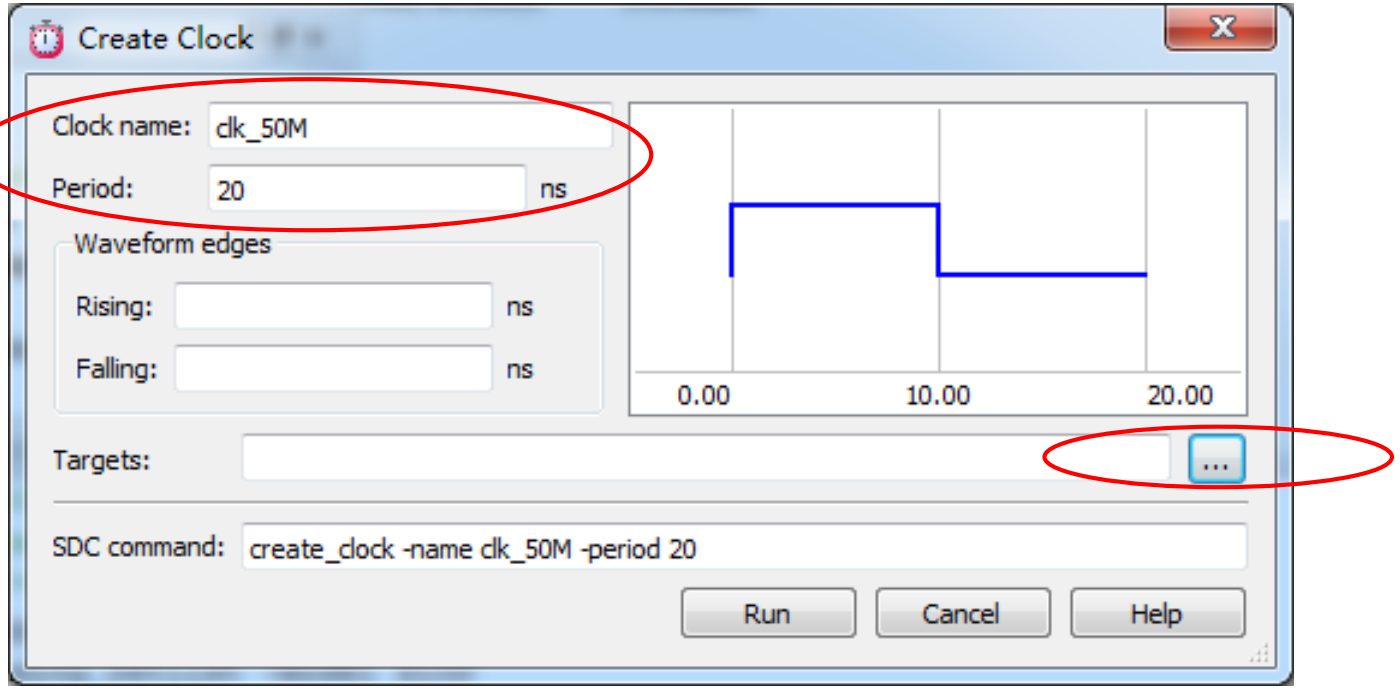
TimeQuest时序约束

点击Constraints->Create Clock



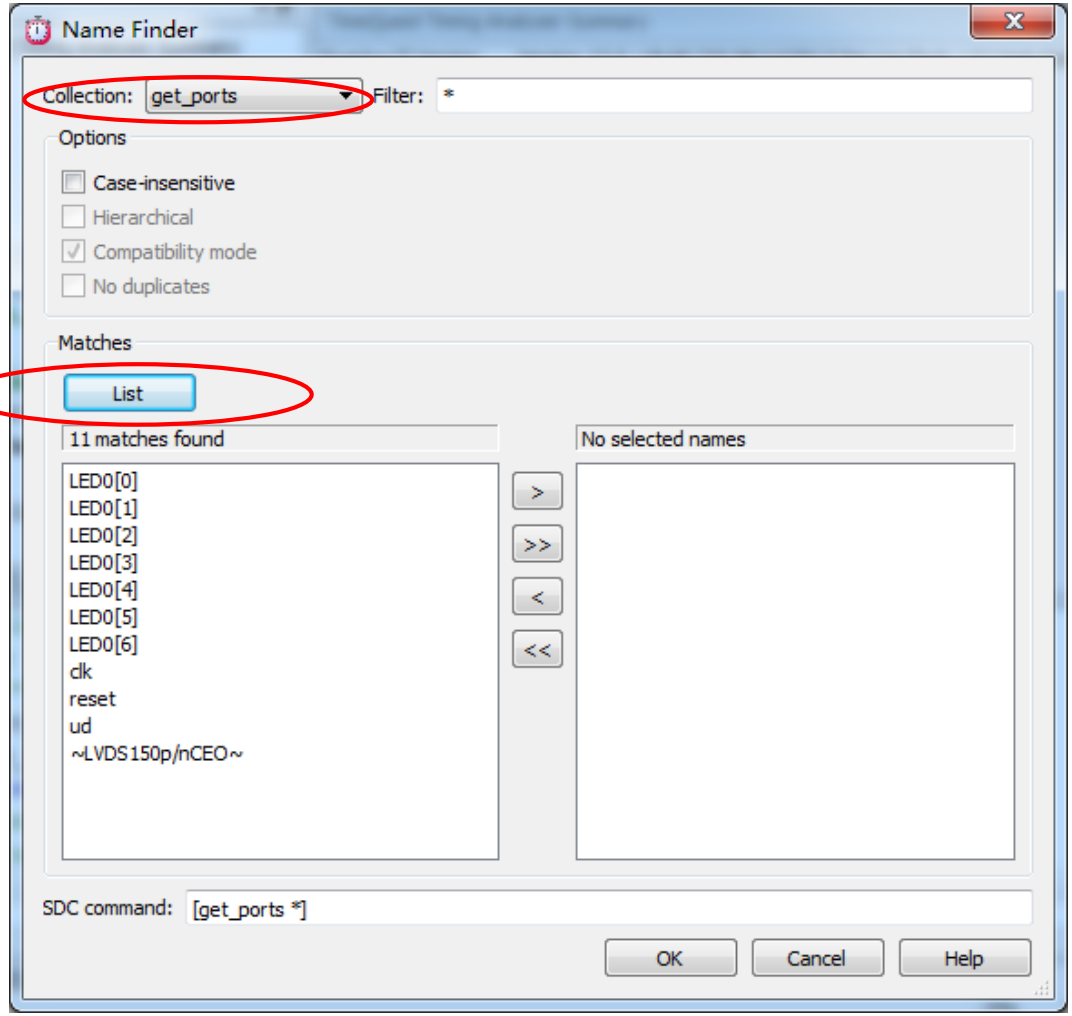
TimeQuest时序约束

设置时钟约束名，时钟周期



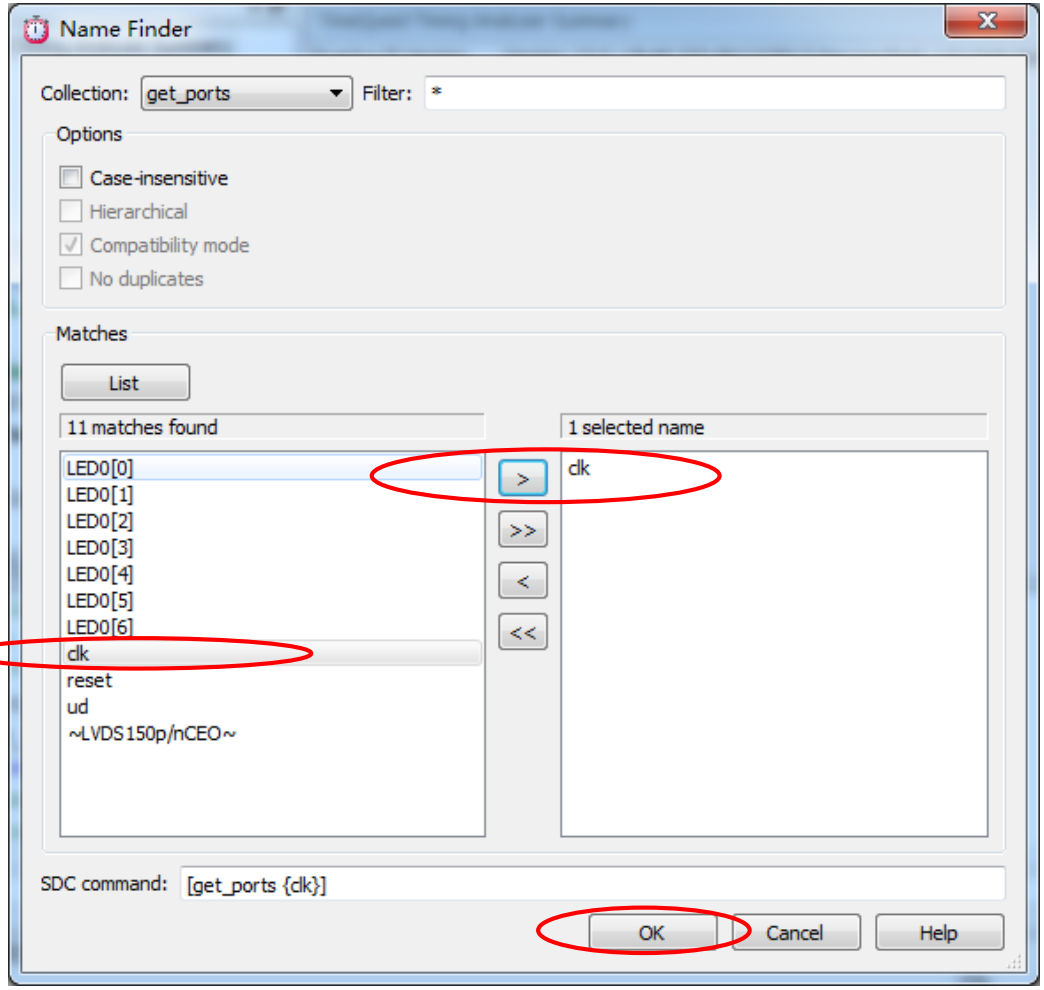
TimeQuest时序约束

设置目标信号：单击Target右侧的浏览按钮，打开Name Finder，Collection选择缺省的get_ports，之后单击List按钮



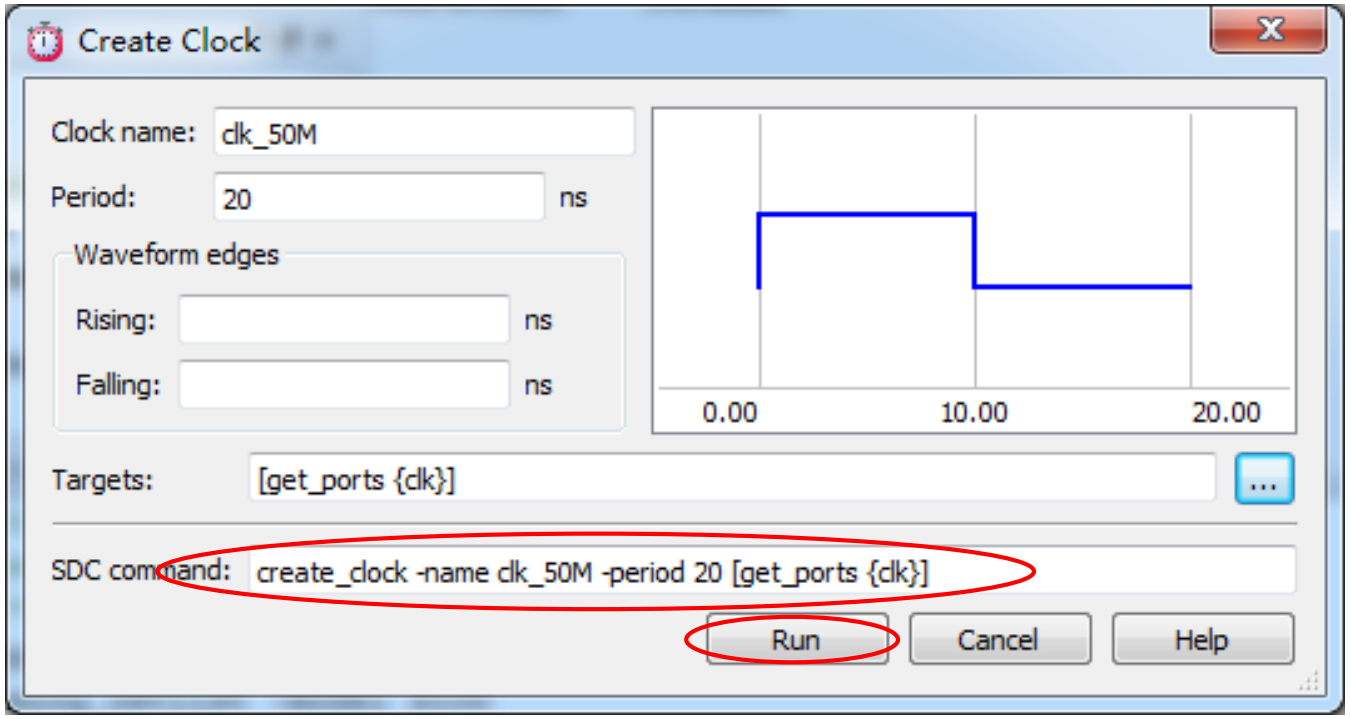
TimeQuest时序约束

选择clk信号，单击>按钮，将clock添加到右侧列表，之后单击OK



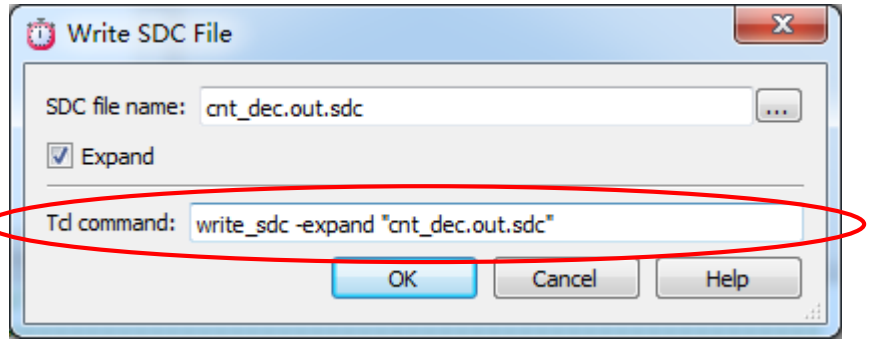
TimeQuest时序约束

返回之后，在SDC command文本框中出现SDC命令，之后单击Run



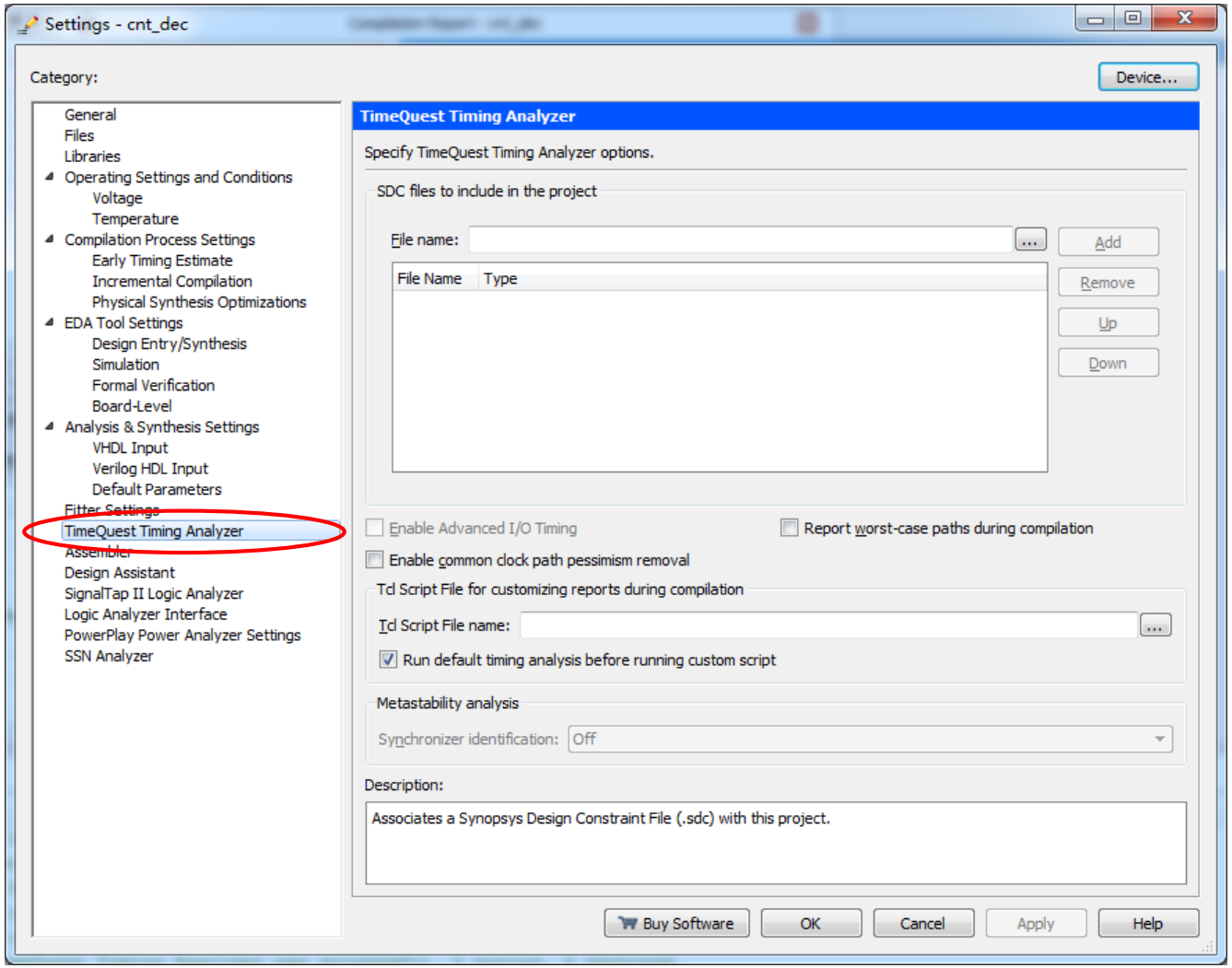
TimeQuest时序约束

- 回到TimeQuest界面之后，单击Constraints->Write SDC file，用缺省设置，单击OK关闭窗口。写出的SDC文件名通常为“工程名.out.sdc”。
- 之后关闭TimeQuest。



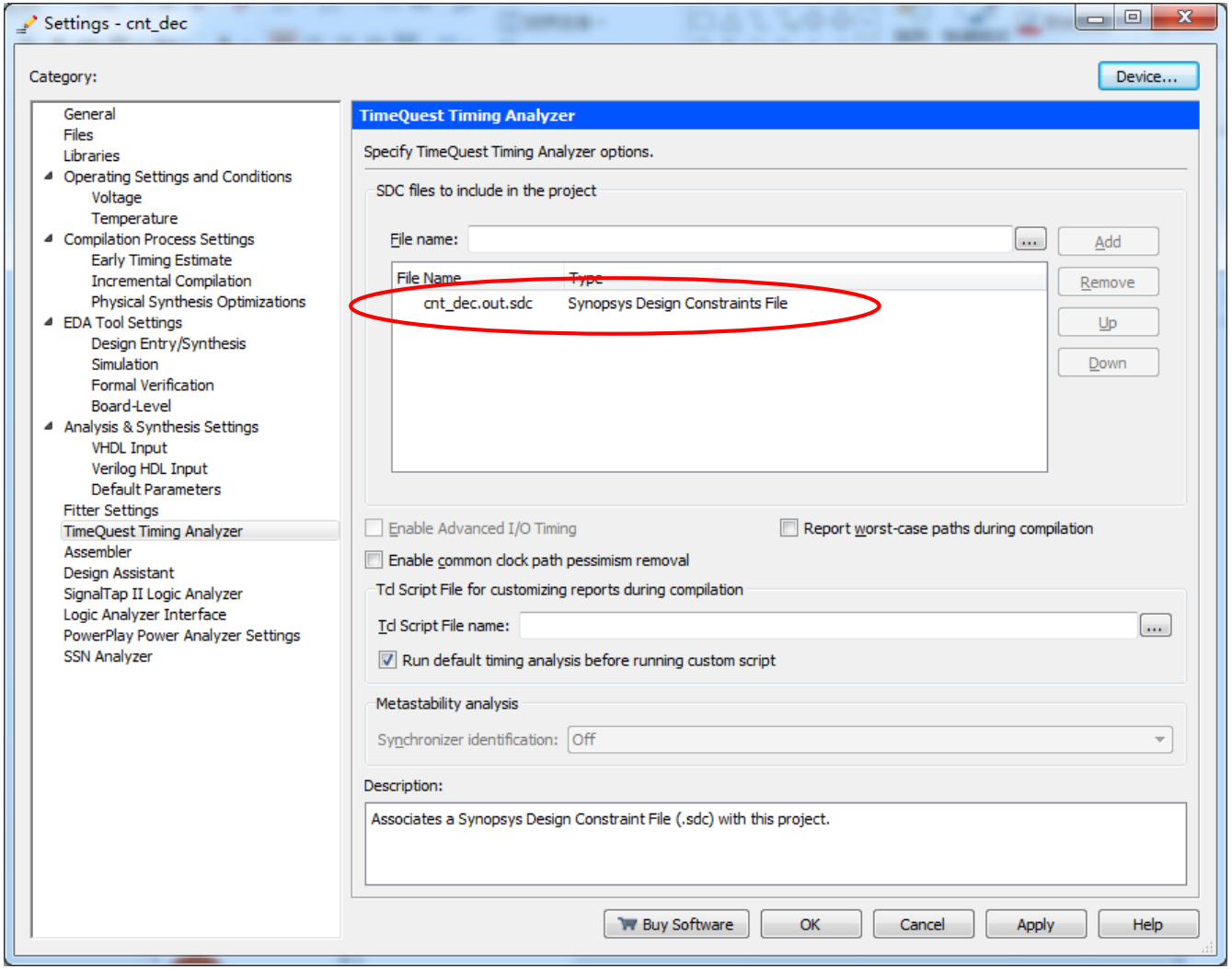
TimeQuest时序约束

回到QuartusII，单击Assignment->Settings，选择TimeQuest Timing Analyzer



TimeQuest时序约束

在右侧将生成的SDC文件添加到SDC file列表



TimeQuest时序约束

重新编译工程，编译完成之后，可以在TimeQuest分析结果中查看时序报告