

# 数字逻辑与处理器基础实验

Quartus II使用说明



# 提 纲

- **新建工程**
- 设置Unused Pin类型
- 编译、绑定管脚
- 程序下载
- TimeQuest时序约束

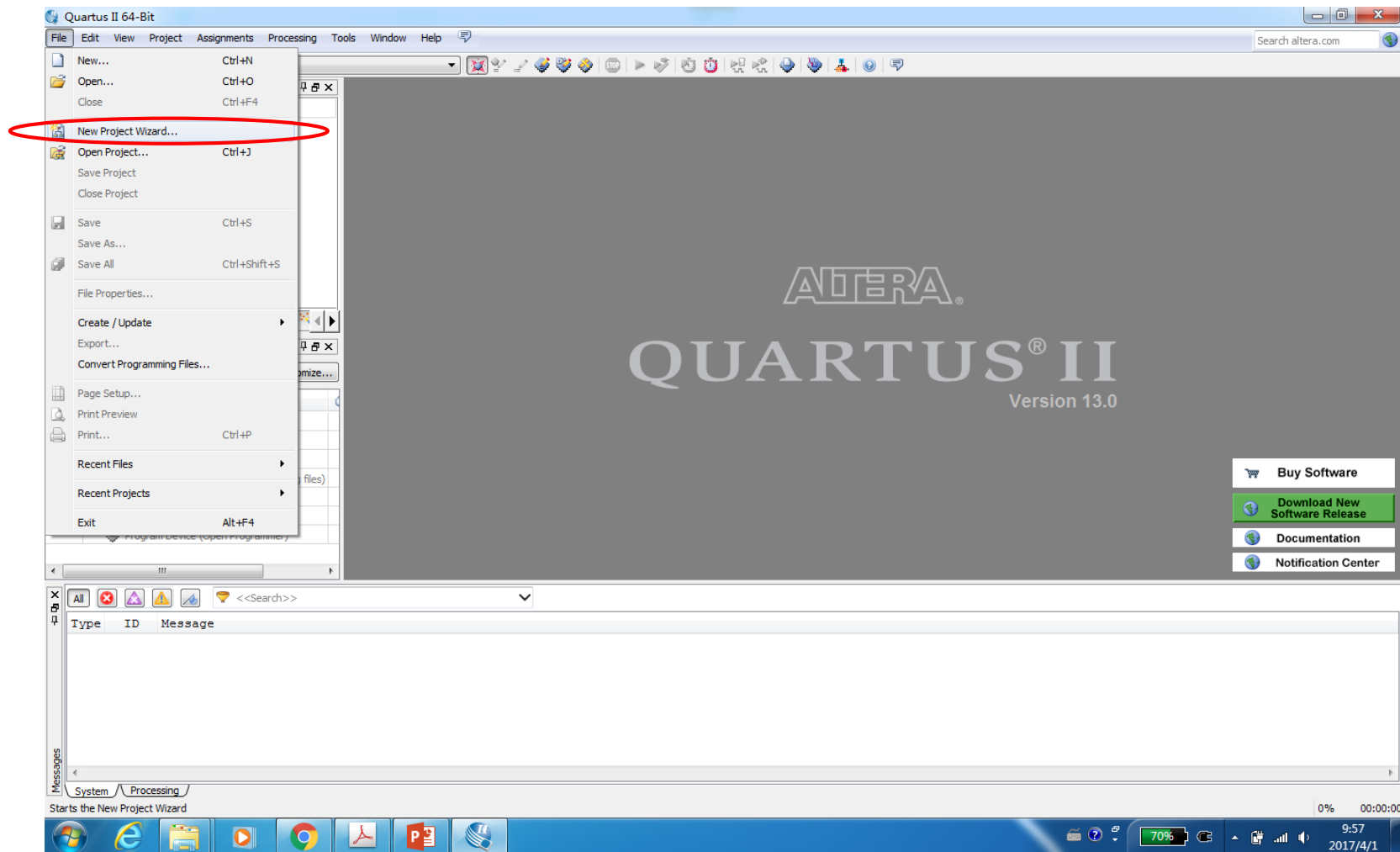


# 启动Quartus软件



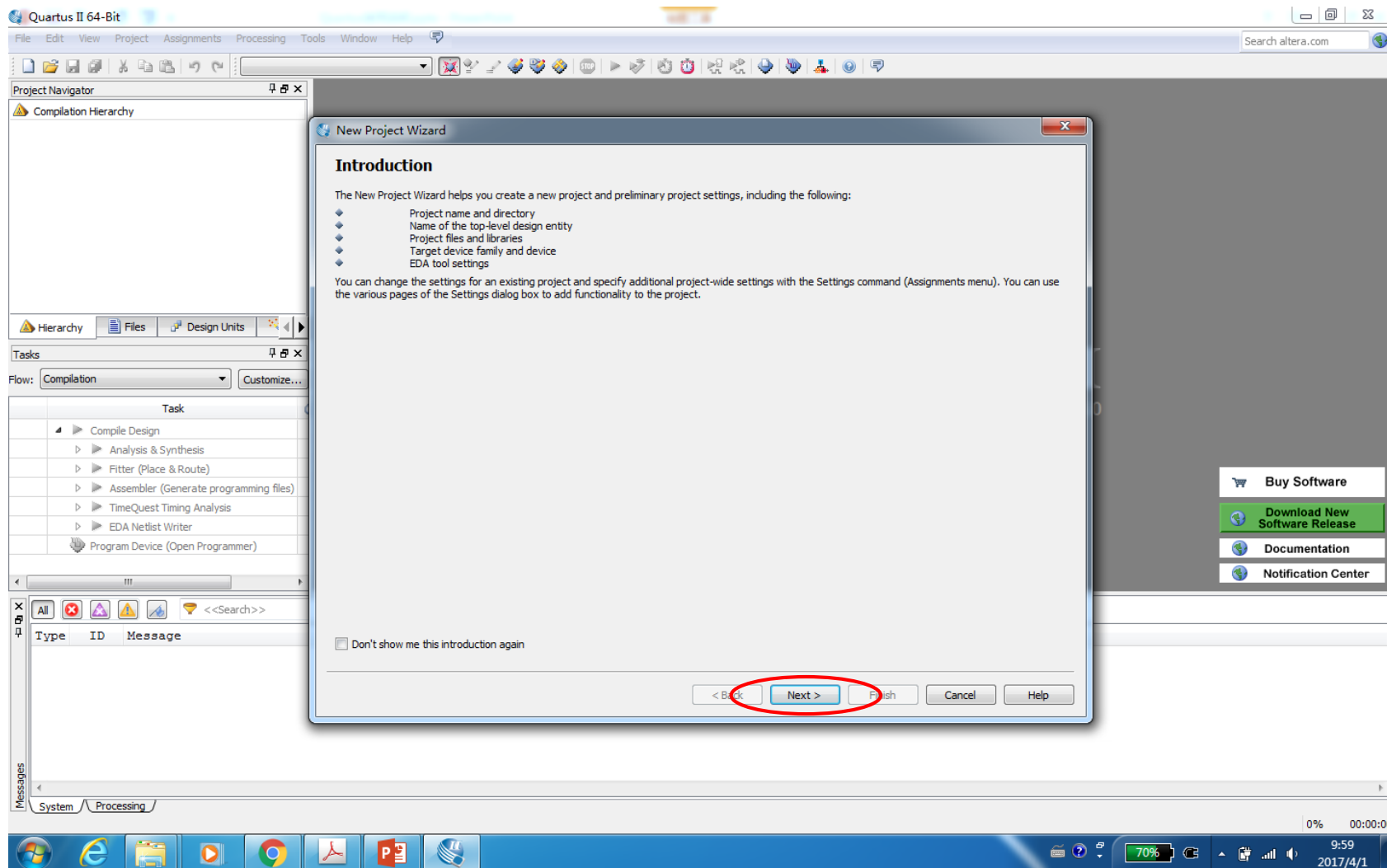


# 新建工程





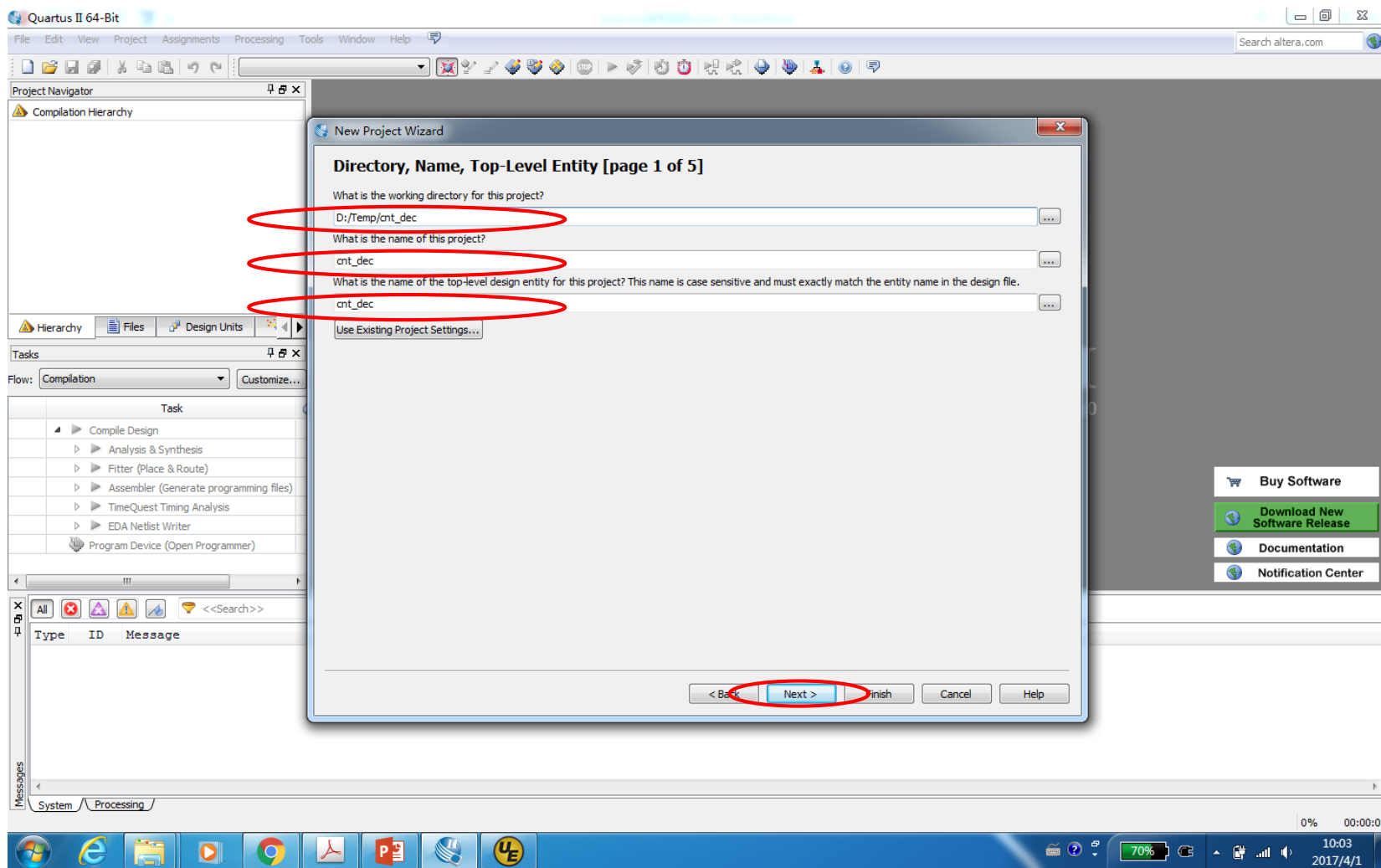
# 新建工程





# 新建工程

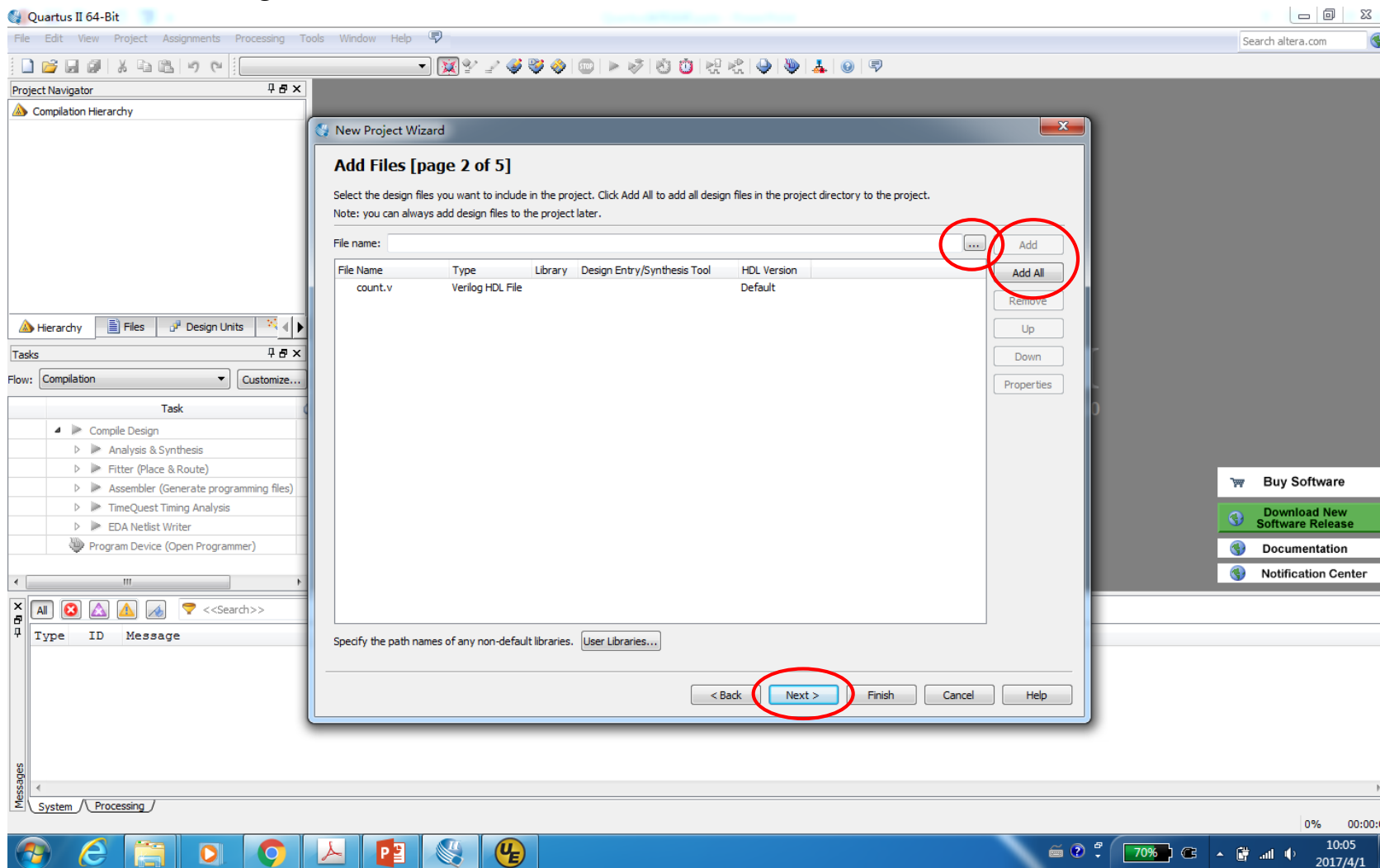
设置工程路径、工程名称和顶层设计模块名，之后单击next





# 新建工程

添加verilog文件，之后next





# 新建工程

设置FPGA型号：EP2C35F672C6，之后next，直到finish

Quartus II 64-Bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming files)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Program Device (Open Programmer)

Messages

System Processing

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

Device family

Family: Cyclone II

Devices: All

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter:

☒ Show advanced devices ☐ HardCopy compatible only

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	G
EP2C35F672C6	1.2V	33216	475	483840	70	4	16
EP2C35F672C7	1.2V	33216	475	483840	70	4	16
EP2C35F672C8	1.2V	33216	475	483840	70	4	16
EP2C35F672I8	1.2V	33216	475	483840	70	4	16
EP2C35U484C6	1.2V	33216	322	483840	70	4	16
EP2C35U484C7	1.2V	33216	322	483840	70	4	16
EP2C35U484C8	1.2V	33216	322	483840	70	4	16

Companion device

HardCopy:

☐ Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

Buy Software

Download New Software Release

Documentation

Notification Center

0% 00:00:00

10:08 2017/4/1





# 提 纲

- 新建工程
- *设置Unused Pin类型*
- 编译、绑定管脚
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# 设置Unused Pin类型

Assignment->Device, 打开窗口, 单击Device and Pin Options

Quartus II 64-Bit - D:/Temp/cnt\_dec/cnt\_dec - cnt\_dec

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

- Cyclone II: EP2C35F672C6
  - cnt\_dec

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming files)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Program Device (Open Programmer)

Device

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

Device family

Family: Cyclone II

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter:

☒ Show advanced devices ☐ HardCopy compatible only

Device and Pin Options...

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements
EP2C20F484C6	1.2V	18752	315	239616	52
EP2C20F484C7	1.2V	18752	315	239616	52
EP2C20F484C8	1.2V	18752	315	239616	52
EP2C20F484I8	1.2V	18752	315	239616	52
EP2C20Q240C8	1.2V	18752	142	239616	52
EP2C35F484C6	1.2V	33216	322	483840	70
EP2C35F484C7	1.2V	33216	322	483840	70
EP2C35F484C8	1.2V	33216	322	483840	70
EP2C35F484I8	1.2V	33216	322	483840	70
EP2C35F672C6	1.2V	33216	475	483840	70

Migration compatibility

Migration Devices...

0 migration devices selected

Companion device

HardCopy:

☒ Limit DSP & RAM to HardCopy device resources

Buy Software OK Cancel Help

13.0

Buy Software

Download New Software Release

Documentation

Notification Center

System Processing

0% 00:00:00

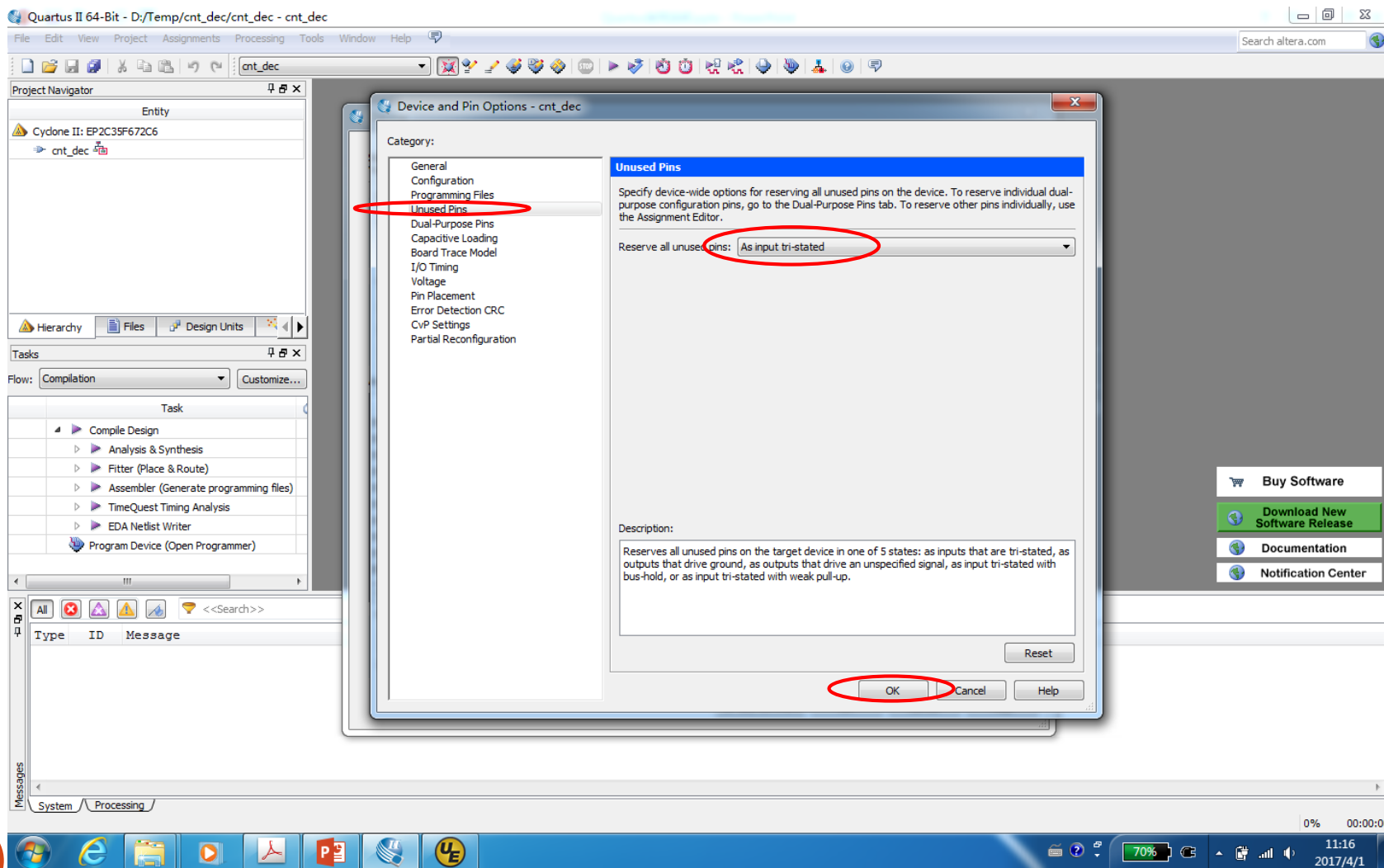
10:09 2017/4/1

70%



# 设置Unused Pin类型

在Unused Pins标签下设置未用引脚为“As input tri-stated”，之后确定





# 提 纲

- 新建工程
- 设置Unused Pin类型
- **编译、绑定管脚**
- 程序下载
- TimeQuest时序约束



# 编译

单击Start Compilation按钮开始编译

Quartus II 64-Bit - D:/Temp/cnt\_dec/cnt\_dec - cnt\_dec

File Edit View Project Assignments Processing Tools Window Help

cnt\_dec

Project Navigator

Entity

- Cyclone II: EP2C35F672C6
  - cnt\_dec
    - clk\_gen:U0
    - count:U1
    - BCD7:U2

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- TimeQuest Timing Analyzer

Flow Summary

Flow Status: Successful - Sat Apr 01 11:20:00 2017

Quartus II 64-Bit Version: 13.0.1 Build 232 06/12/2013 SP 1 S3 Web Edition

Revision Name: cnt\_dec

Top-level Entity Name: cnt\_dec

Family: Cyclone II

Device: EP2C35F672C6

Timing Models: Final

Total logic elements: 58 / 33,216 (< 1 %)

Total combinational functions: 56 / 33,216 (< 1 %)

Dedicated logic registers: 30 / 33,216 (< 1 %)

Total registers: 30

Total pins: 10 / 475 (2 %)

Total virtual pins: 0

Total memory bits: 0 / 483,840 (0 %)

Embedded Multiplier 9-bit elements: 0 / 70 (0 %)

Total PLLs: 0 / 4 (0 %)

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

Messages

Type ID Message

- 332140 No Removal paths to report
- 332146 Worst-case minimum pulse width slack is -1.380
- 332001 The selected device family is not supported by the report\_metastability command.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
- 293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings

System Processing (96)

100% 00:00:33

11:21 2017/4/1



# 编译

编译完成显示如下

Quartus II 64-Bit - D:/Temp/cnt\_dec/cnt\_dec - cnt\_dec

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

- Cyclone II: EP2C35F672C6
  - cnt\_dec
    - clk\_gen:U0
    - count:U1
    - BCD7:U2

Tasks

Flow: Compilation Customize...

Task	Progress
Compile Design	00%
Analysis & Synthesis	00%
Fitter (Place & Route)	00%
Assembler (Generate programming files)	00%
TimeQuest Timing Analysis	00%
EDA Netlist Writer	00%
Program Device (Open Programmer)	00%

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- TimeQuest Timing Analyzer

Flow Summary

Flow Status: Successful - Sat Apr 01 11:22:17 2017

Quartus II 64-Bit Version: 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition

Revision Name: cnt\_dec

Top-level Entity Name: cnt\_dec

Family: Cyclone II

Device: EP2C35F672C6

Timing Models: Final

Total logic elements: 58 / 33,216 (< 1 %)

Total combinational functions: 56 / 33,216 (< 1 %)

Dedicated logic registers: 30 / 33,216 (< 1 %)

Total registers: 30

Total pins: 10 / 475 (2 %)

Total virtual pins: 0

Total memory bits: 0 / 483,840 (0 %)

Quartus II

Full Compilation was successful (12 warnings)

OK

Messages

Type	ID	Message
Info	332140	No Removal paths to report
Info	332146	Worst-case minimum pulse width slack is -1.380
Info	332001	The selected device family is not supported by the report_metastability command.
Info	332102	Design is not fully constrained for setup requirements
Info	332102	Design is not fully constrained for hold requirements
Info	293000	Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Info	293000	Quartus II Full Compilation was successful. 0 errors, 12 warnings

System Processing (96%)

100% 00:00:26

70%

11:22 2017/4/1



# 引脚绑定-方法1

编译完成后，点击Assignment->Pin Planner

The screenshot shows the Quartus II 64-Bit IDE interface. The 'Assignments' menu is open, and the 'Pin Planner' option is highlighted with a red circle. The 'Flow Summary' window is open, displaying the compilation status and resource usage. The 'Messages' window at the bottom shows the compilation results, indicating that the compilation was successful with 0 errors and 12 warnings.

**Flow Summary**

Flow Status	Successful - Sat Apr 01 11:22:17 2017
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	cnt_dec
Top-level Entity Name	cnt_dec
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	58 / 33,216 (< 1 %)
Total combinational functions	56 / 33,216 (< 1 %)
Dedicated logic registers	30 / 33,216 (< 1 %)
Total registers	30
Total pins	10 / 475 (2 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

**Messages**

Type	ID	Message
Information	332140	No Removal paths to report
Warning	332146	Worst-case minimum pulse width slack is -1.380
Warning	332001	The selected device family is not supported by the report_metastability command.
Warning	332102	Design is not fully constrained for setup requirements
Warning	332102	Design is not fully constrained for hold requirements
Information		Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Information	293000	Quartus II Full Compilation was successful. 0 errors, 12 warnings



# 引脚绑定-方法1

在Pin Planner窗口，每一个引脚对应的Location位置输入引脚号，“PIN\_”不用输入，会自动补上

Top View - Wire Bond  
Cyclone II - EP2C35F872C6

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Differential Pair
LED0[6]	Output	PIN_V13	8	B8_N0	PIN_C9	3.3-V LV...default		24mA (default)	
LED0[5]	Output	PIN_V14	8	B8_N0	PIN_G10	3.3-V LV...default		24mA (default)	
LED0[4]	Output	PIN_AE11	8	B8_N0	PIN_C8	3.3-V LV...default		24mA (default)	
LED0[3]	Output	PIN_AD11	8	B8_N0	PIN_D9	3.3-V LV...default		24mA (default)	
LED0[2]	Output	PIN_AC12	8	B8_N0	PIN_B8	3.3-V LV...default		24mA (default)	
LED0[1]	Output	PIN_AB12	8	B8_N0	PIN_F10	3.3-V LV...default		24mA (default)	
LED0[0]	Output	PIN_AF10	8	B8_N0	PIN_D8	3.3-V LV...default		24mA (default)	
clk	Input	PIN_N2		B2_N1	PIN_P2	3.3-V LV...default		24mA (default)	
reset	Input	PIN_G26	5	B5_N0	PIN_P1	3.3-V LV...default		24mA (default)	
ud	Input	PIN_N25	5	B5_N1	PIN_C13	3.3-V LV...default		24mA (default)	
<<new node>>									





# 引脚绑定-方法1

引脚制定完成后，**必须重新编译工程**

The screenshot displays the Quartus II 64-Bit IDE interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The toolbar contains various icons, with the 'Compile' icon (a circular arrow) circled in red. The Project Navigator on the left shows the project hierarchy for 'cnt\_dec' under 'Cyclone II: EP2C35F672C6'. The central pane shows the 'Compilation Report - cnt\_dec' with a 'Flow Summary' table. The bottom pane shows the 'Messages' window with a list of warnings and a successful compilation status.

**Flow Summary**

Flow Status	Successful - Sat Apr 01 11:20:00 2017
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 S3 Web Edition
Revision Name	cnt_dec
Top-level Entity Name	cnt_dec
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	58 / 33,216 (< 1 %)
Total combinational functions	56 / 33,216 (< 1 %)
Dedicated logic registers	30 / 33,216 (< 1 %)
Total registers	30
Total pins	10 / 475 (2 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

**Messages**

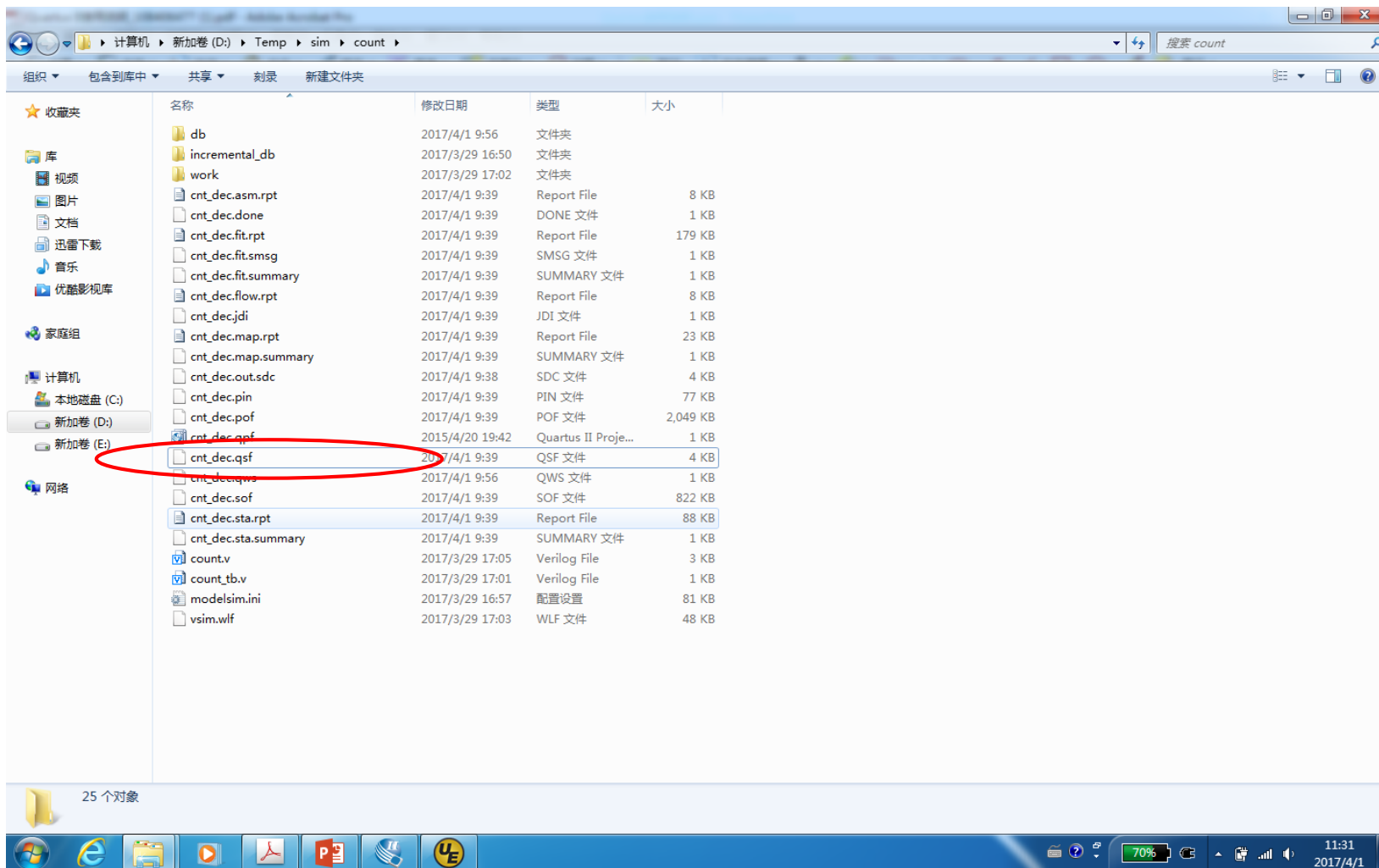
Type	ID	Message
Warning	332140	No Removal paths to report
Warning	332146	Worst-case minimum pulse width slack is -1.380
Warning	332001	The selected device family is not supported by the report_metastability command.
Warning	332102	Design is not fully constrained for setup requirements
Warning	332102	Design is not fully constrained for hold requirements
Information		Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Information		Quartus II Full Compilation was successful. 0 errors, 12 warnings

System Processing (96%) 100% 00:00:33



# 引脚绑定-方法2

在QuartusII工程所在目录下，找到扩展名为.qsf的文件，其文件名和工程名相同





使用文本编辑器打开.qsf文件，可按如下格式指定引脚

The screenshot displays the UltraEdit text editor with a Verilog file named `cnt_dec.qsf`. The file contains several sections of code defining global and location assignments for a Stratix device. A red rectangular box highlights a specific block of code between lines 50 and 60, which consists of ten `set_location_assignment` statements mapping various pins to LED outputs.

```

50 set_global_assignment -name STRATIX_DEVICE_IO STANDARD "3.3-V LVTTL"
51
52 set_location_assignment PIN_N25 -to ud
53 set_location_assignment PIN_G26 -to reset
54
55 set_location_assignment PIN_N2 -to clk
56
57 set_location_assignment PIN_V13 -to LED0[6]
58 set_location_assignment PIN_V14 -to LED0[5]
59
60 set_location_assignment PIN_AE11 -to LED0[4]
61 set_location_assignment PIN_AD11 -to LED0[3]
62 set_location_assignment PIN_AC12 -to LED0[2]
63 set_location_assignment PIN_AB12 -to LED0[1]
64 set_location_assignment PIN_AF10 -to LED0[0]
65
66 set_instance_assignment -name PARTITION_HIERARCHY root_partition -to | -section_id Top

```

The status bar at the bottom indicates the current position is at row 47, column 56, in DOS encoding (ANSI/OEM - 简体中文 GBK), with a non-visual mode selected. The system tray shows the date and time as 2017/4/1 19:39:23.



# 引脚绑定-方法2

- 使用.qsf文件指定引脚的方法，可在新建工程完成之后直接进行，不需要先编译再修改qsf文件
- 通过qsf文件指定完引脚后，**必须重新编译工程，才能使引脚指定生效**



# 提 纲

- 新建工程
- 设置Unused Pin类型
- 编译、绑定管脚
- **程序下载**
- TimeQuest时序约束



# 程序下载

单击programmer按钮

The screenshot shows the Quartus II 64-Bit software interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The toolbar contains various icons, with the 'Programmer' button (represented by a blue chip icon) circled in red. Below the toolbar, the 'Project Navigator' pane on the left shows a project hierarchy for 'cnt\_dec' under 'Cyclone II: EP2C35F672C6'. The 'Table of Contents' pane in the center lists various reports, with 'Flow Summary' selected. The 'Flow Summary' pane on the right displays the compilation status: 'Successful - Sat Apr 01 11:28:33 2017'. It lists details such as Quartus II 64-Bit Version (13.0.1), Revision Name (cnt\_dec), Top-level Entity Name (cnt\_dec), Family (Cyclone II), Device (EP2C35F672C6), and various resource usage statistics. The 'Messages' pane at the bottom shows a list of messages, including warnings about removal paths, pulse width slack, and device family support, as well as success messages for the TimeQuest Timing Analyzer and the full compilation.

Quartus II 64-Bit - D:/Temp/cnt\_dec/cnt\_dec - cnt\_dec

File Edit View Project Assignments Processing Tools Window Help

cnt\_dec

Project Navigator

Entity

- Cyclone II: EP2C35F672C6
  - cnt\_dec
    - clk\_gen:U0
    - count:U1
    - BCD7:U2

Table of Contents

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- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- TimeQuest Timing Analyzer

Flow Summary

Flow Status: Successful - Sat Apr 01 11:28:33 2017

Quartus II 64-Bit Version: 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition

Revision Name: cnt\_dec

Top-level Entity Name: cnt\_dec

Family: Cyclone II

Device: EP2C35F672C6

Timing Models: Final

Total logic elements: 58 / 33,216 (< 1 %)

Total combinational functions: 56 / 33,216 (< 1 %)

Dedicated logic registers: 30 / 33,216 (< 1 %)

Total registers: 30

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Total memory bits: 0 / 483,840 (0 %)

Embedded Multiplier 9-bit elements: 0 / 70 (0 %)

Total PLLs: 0 / 4 (0 %)

Messages

Type ID Message

- 332140 No Removal paths to report
- 332146 Worst-case minimum pulse width slack is -1.380
- 332001 The selected device family is not supported by the report\_metastability command.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
- 293000 Quartus II Full Compilation was successful. 0 errors, 11 warnings

System Processing (92)

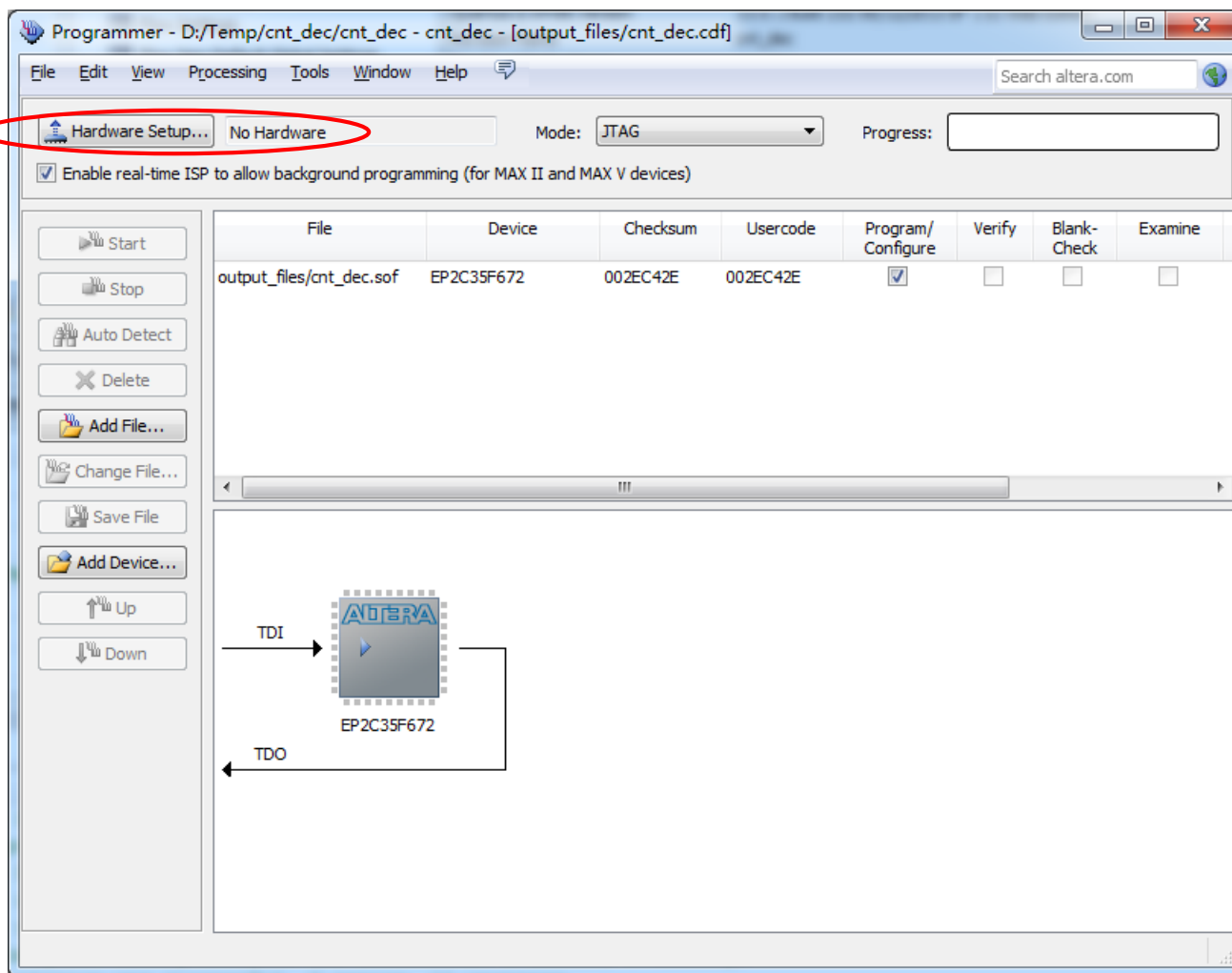
Opens a Programmer window

100% 00:00:25

11:36 2017/4/1

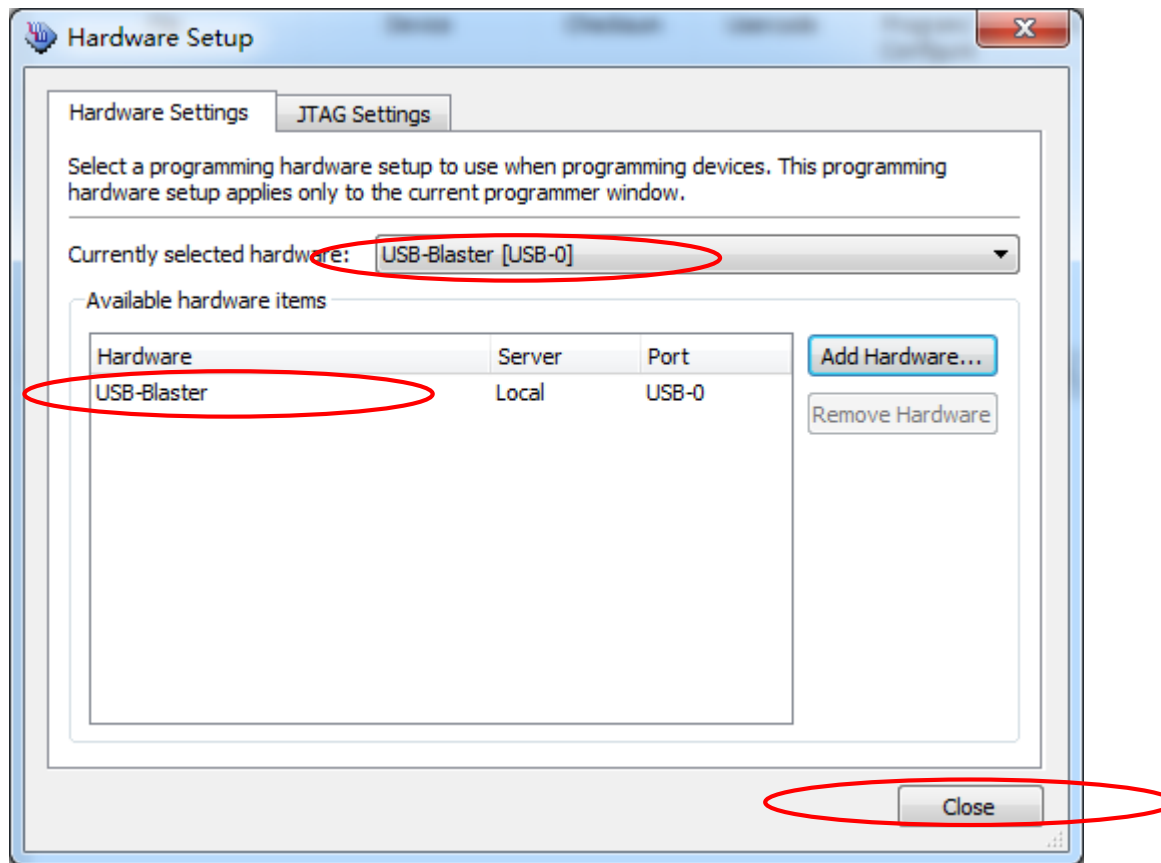
# 程序下载

单击Hardware Setup按钮，设置下载线



# 程序下载

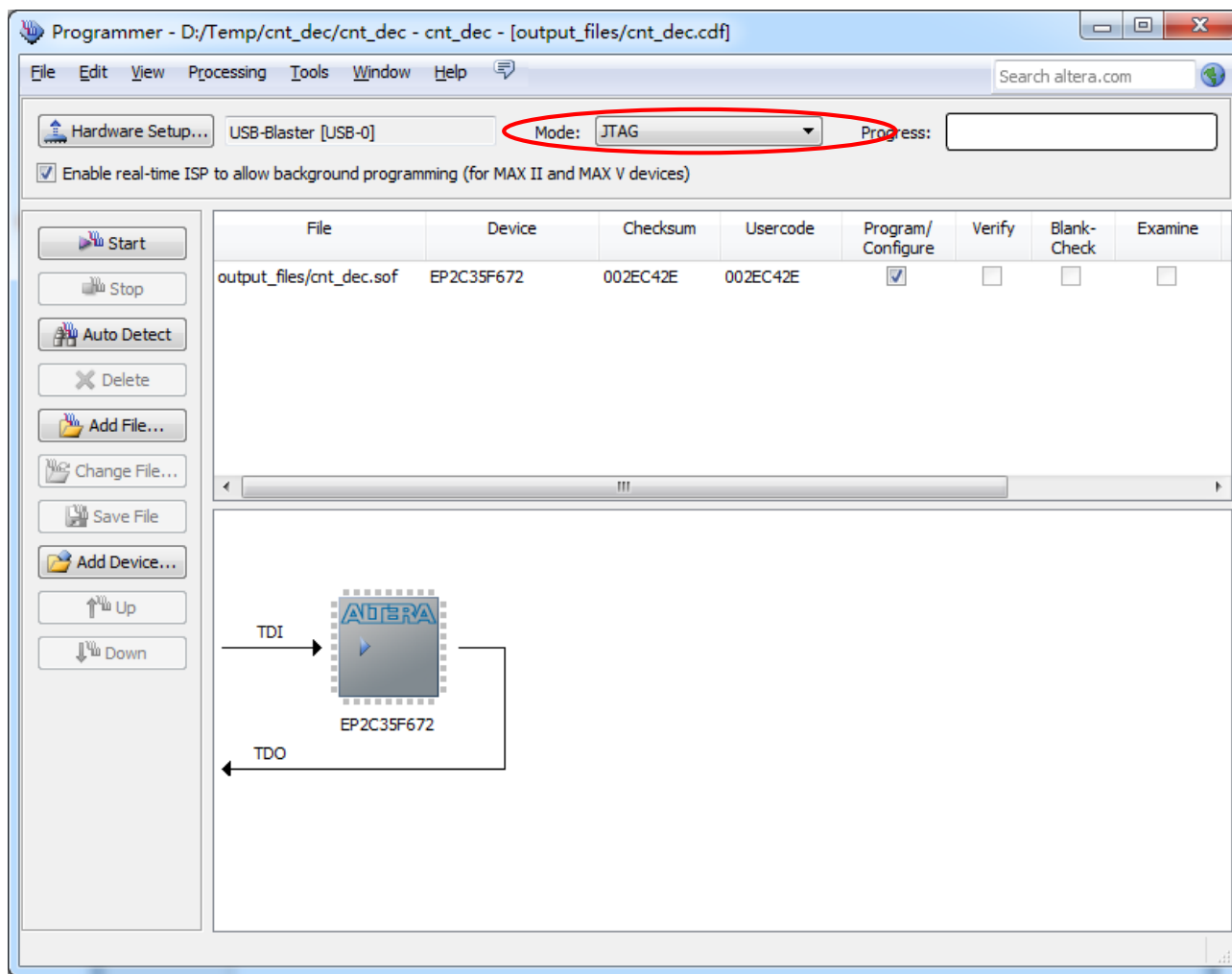
在Hardware Setup窗口，设置selected hardware为USB-Blaster，之后close





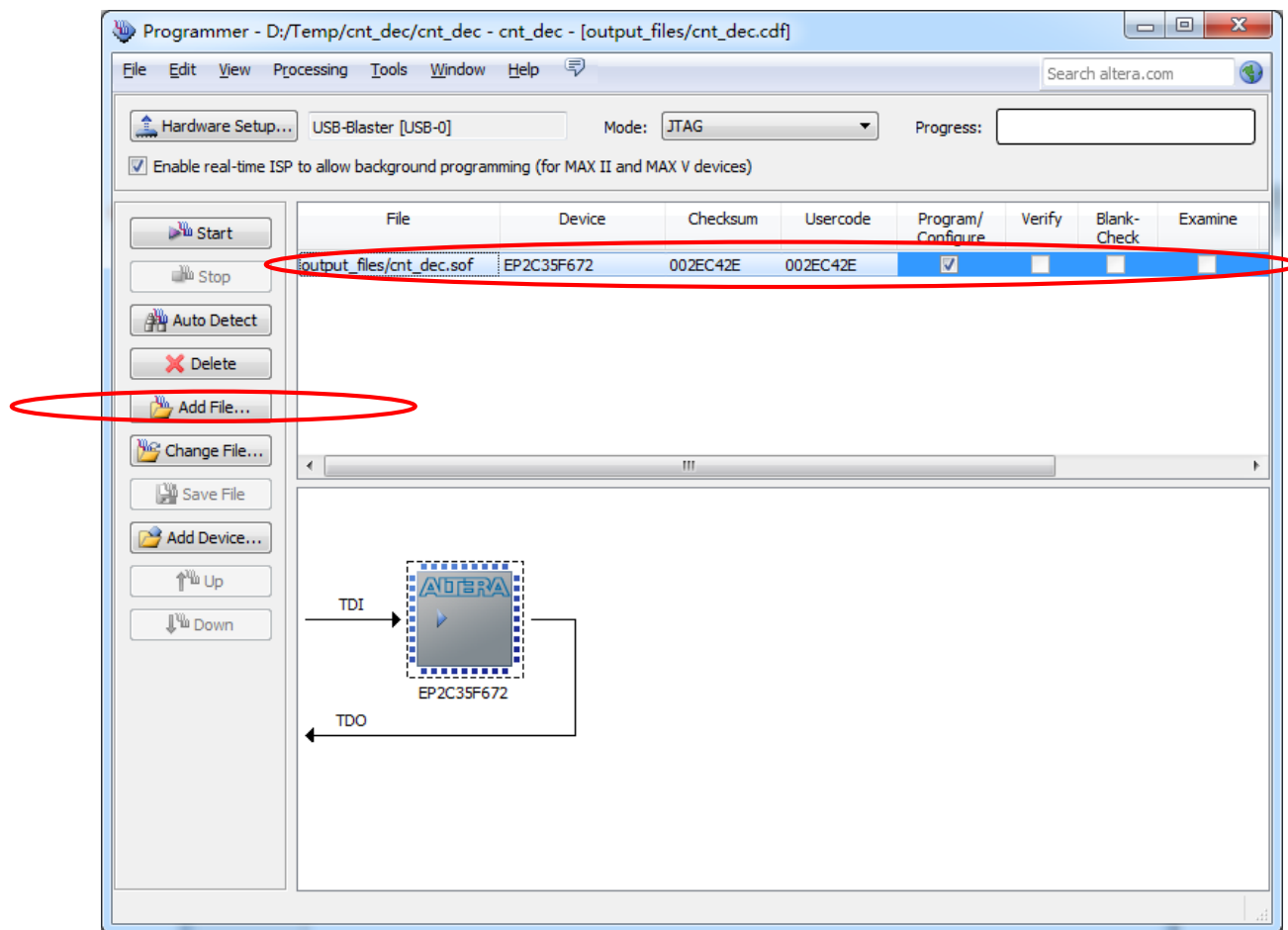
# 程序下载

选择下载模式为JTAG



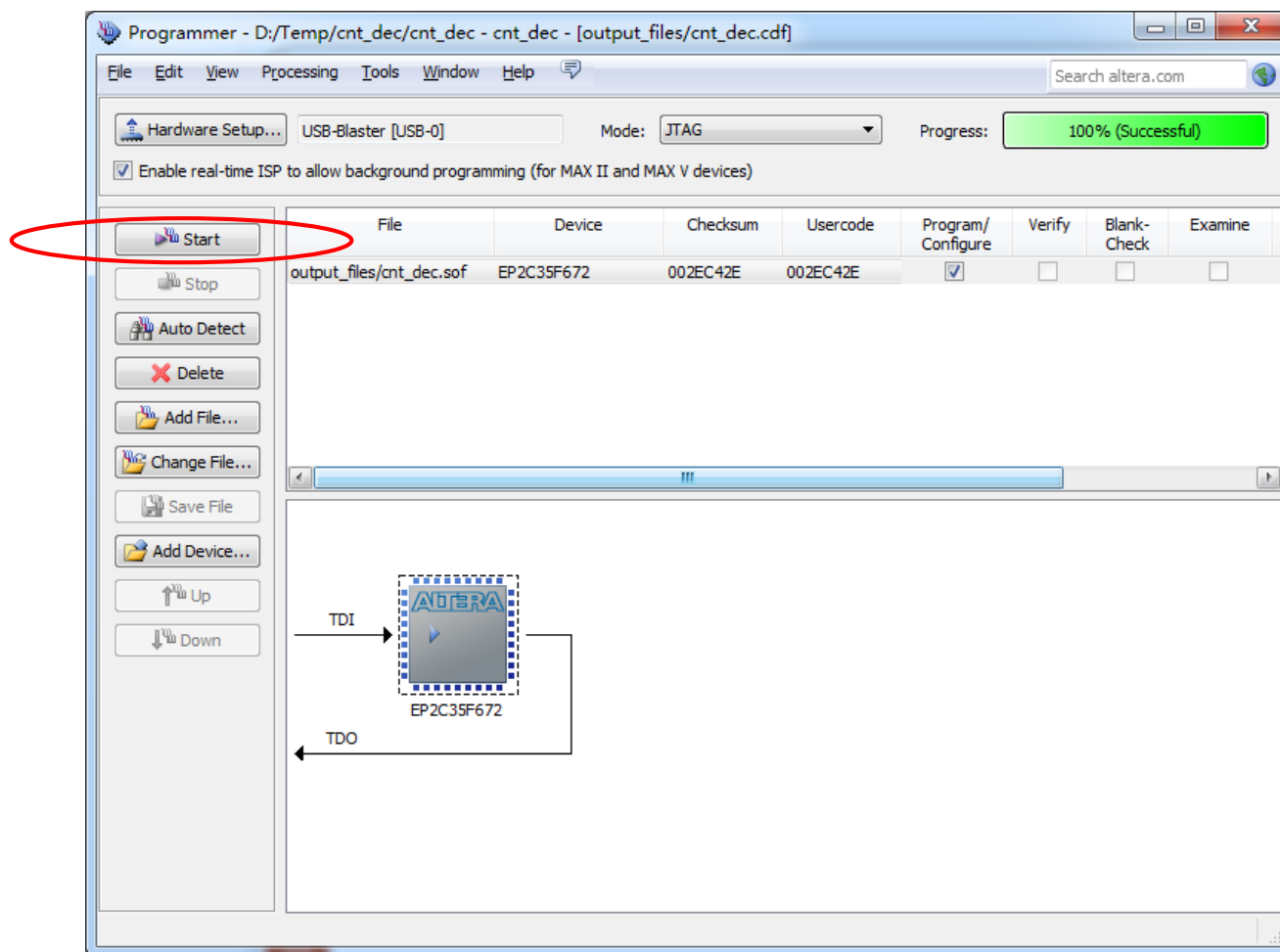
# 程序下载

添加\*.sof下载文件，programmer窗口缺省会添加当前工程的sof文件，也可手动添加文件



# 程序下载

单击Start按钮开始下载





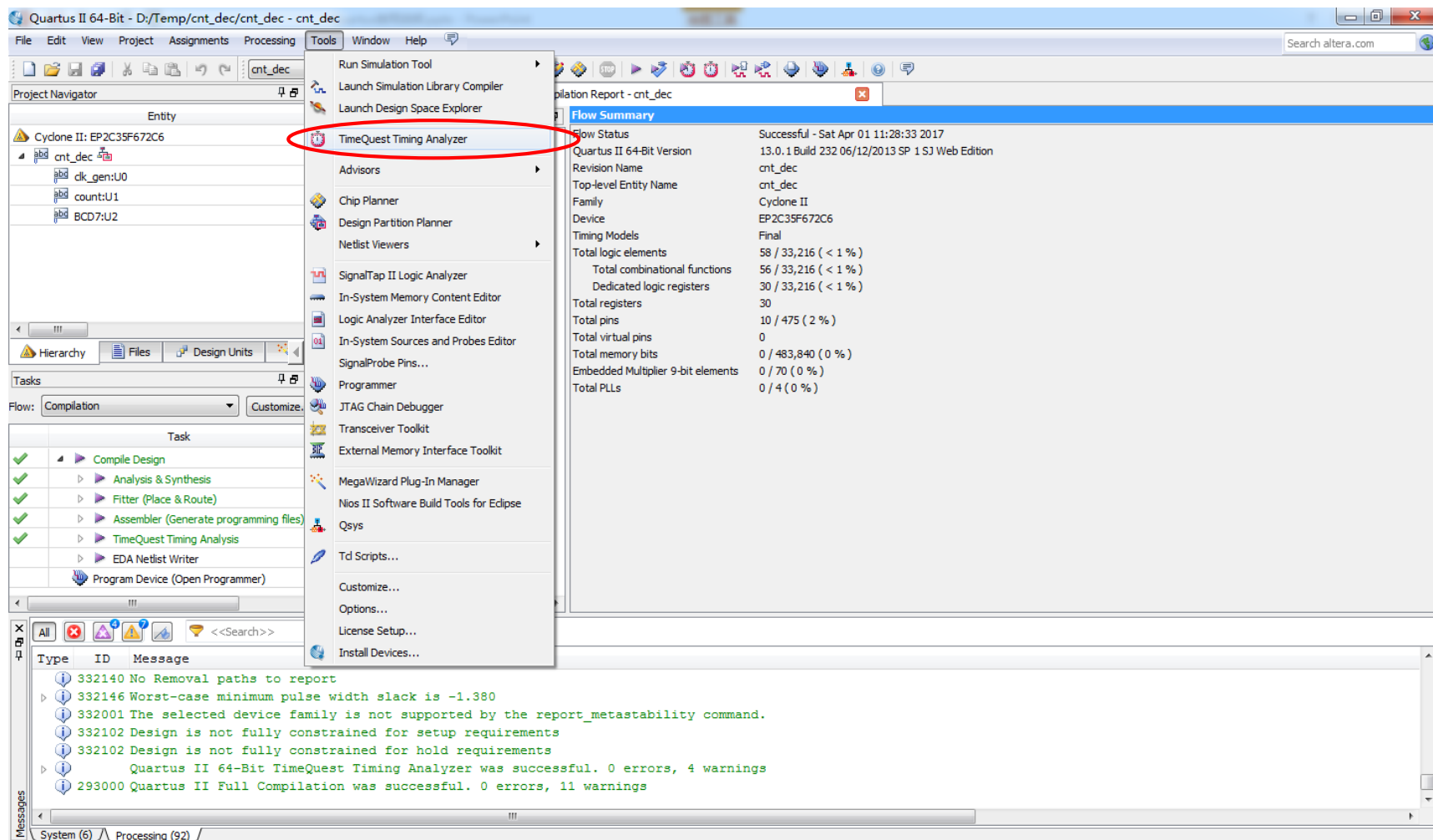
# 提 纲

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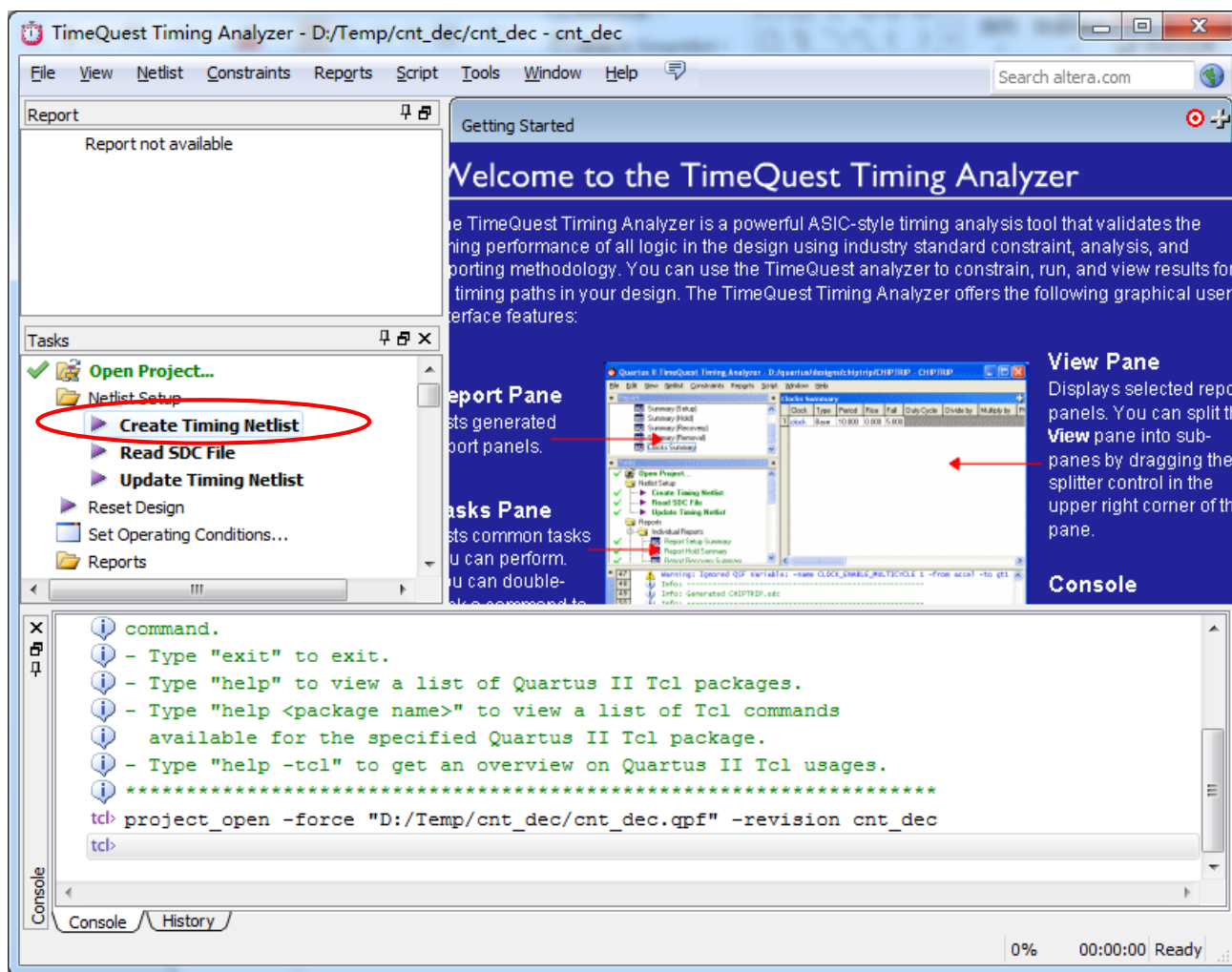
# TimeQuest时序约束

单击Tools->TimeQuest Timing Analyzer, 启动TimeQuest



# TimeQuest时序约束

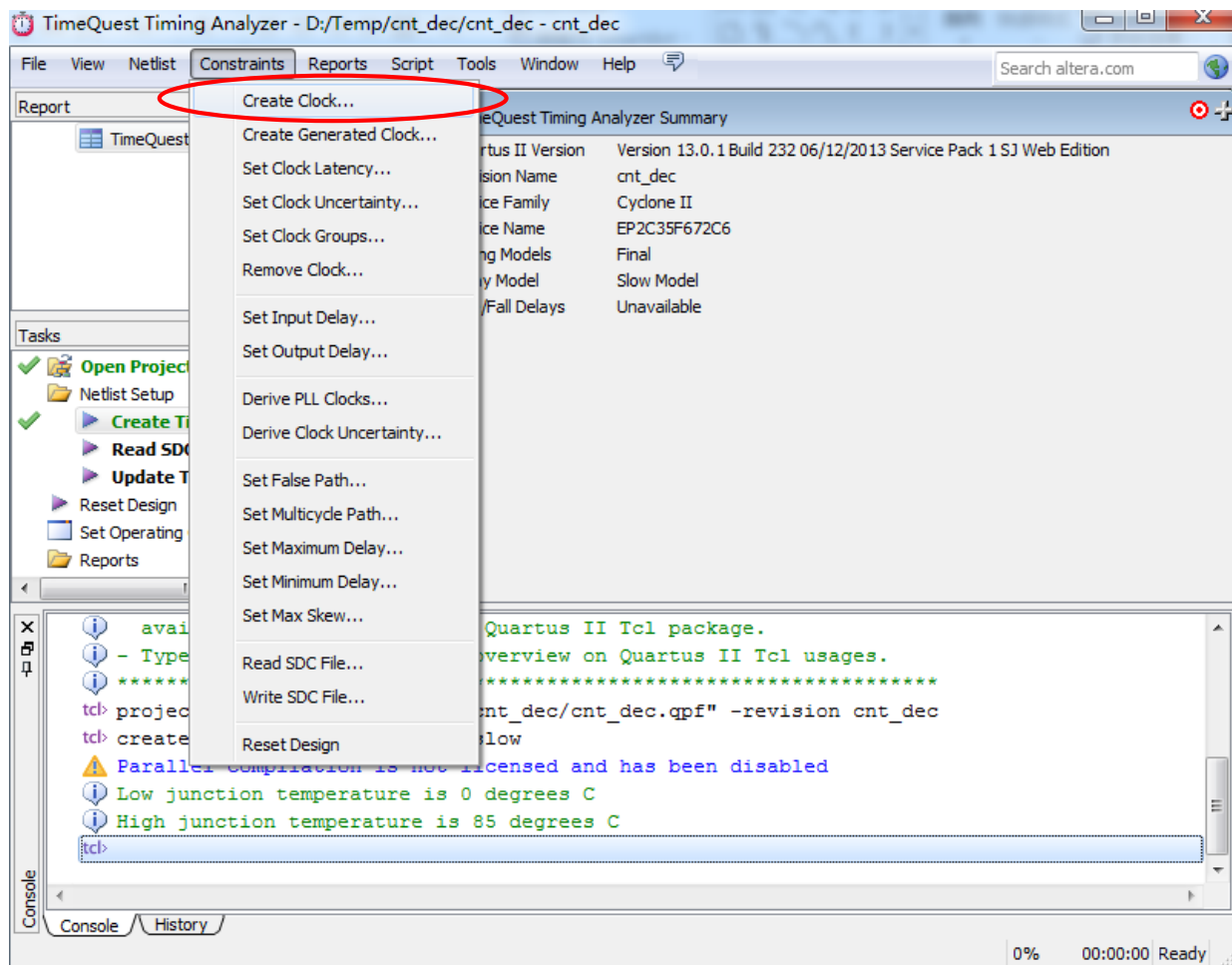
双击Tasks->Create Timing Netlist





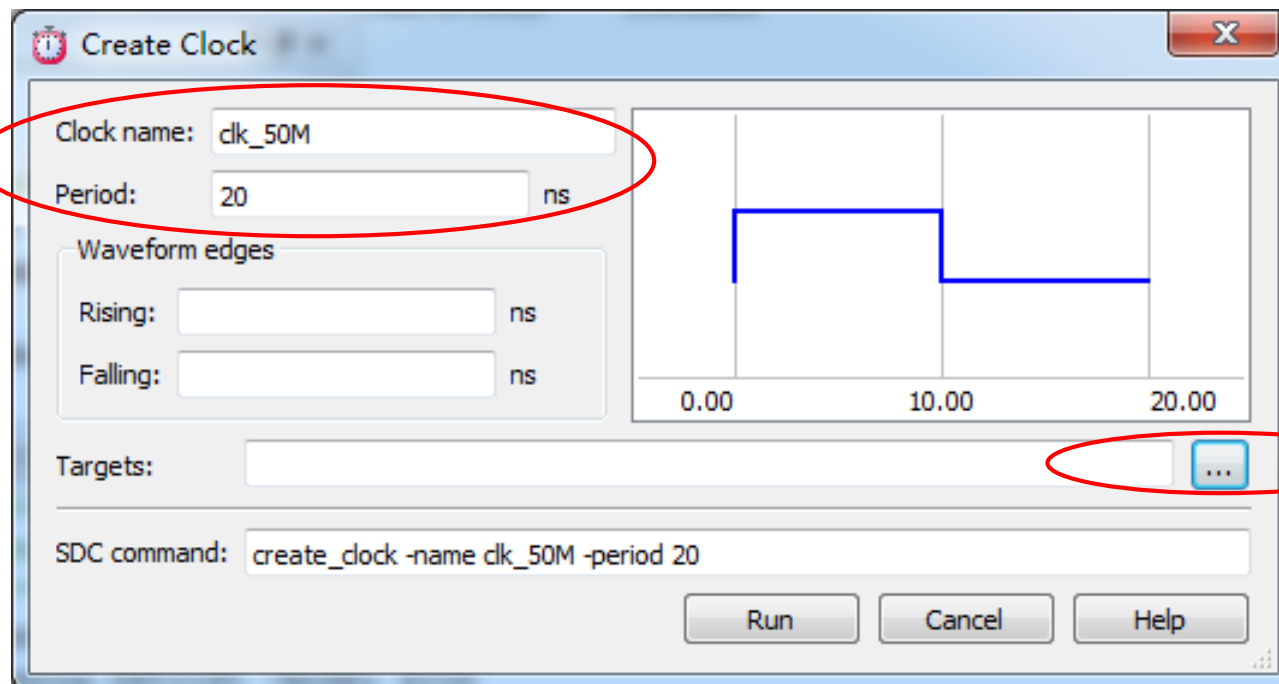
# TimeQuest时序约束

点击Constraints->Create Clock



# TimeQuest时序约束

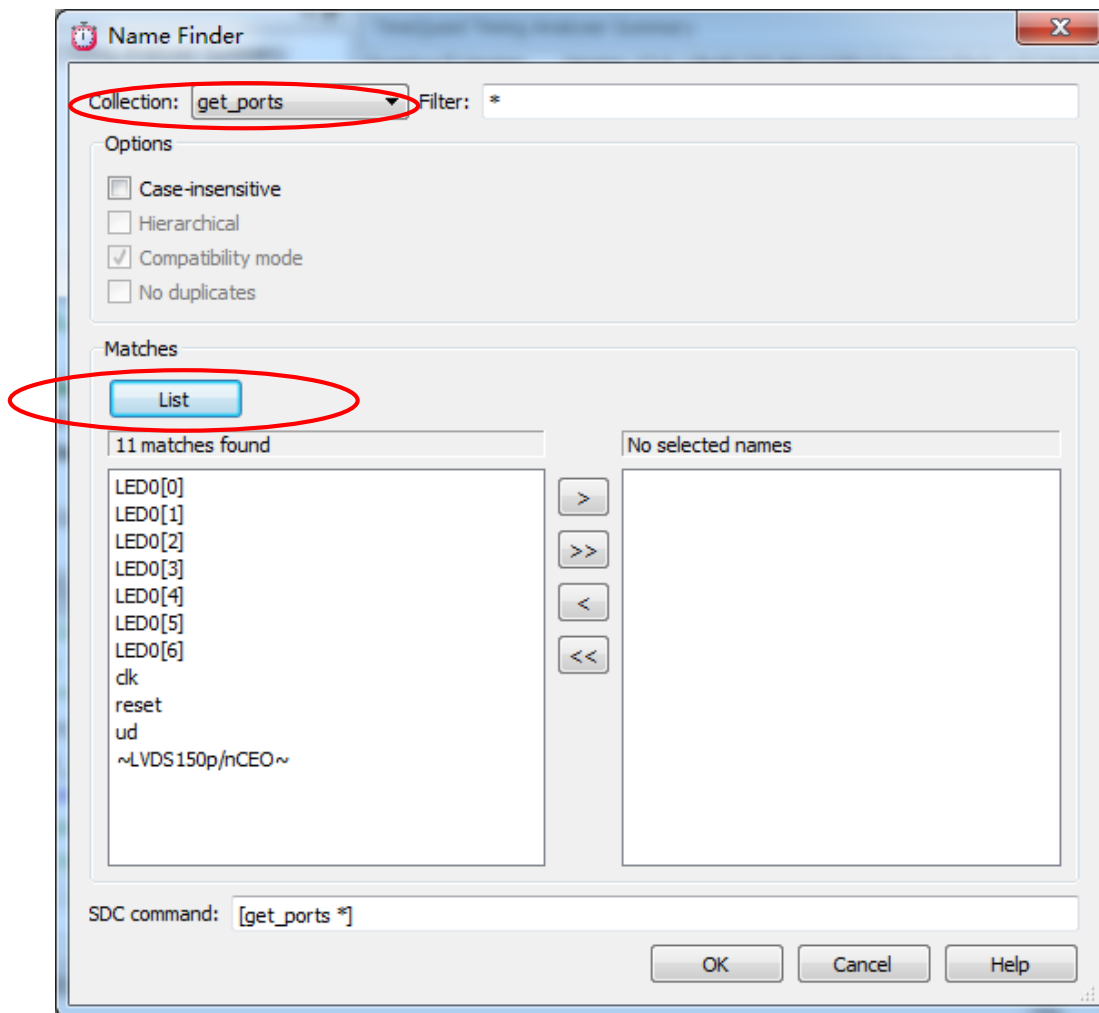
设置时钟约束名，时钟周期





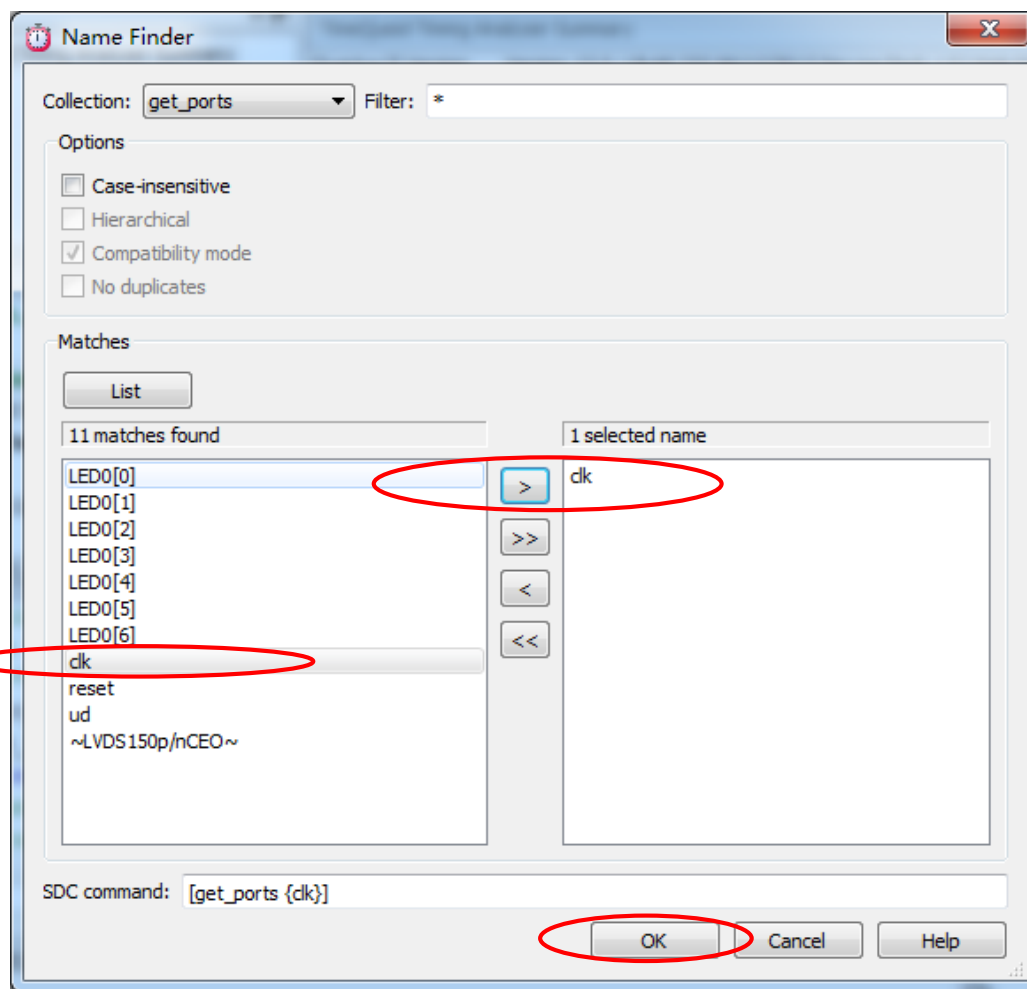
# TimeQuest时序约束

设置目标信号：单击Target右侧的浏览按钮，打开Name Finder，  
Collection选择缺省的get\_ports，之后单击List按钮



# TimeQuest时序约束

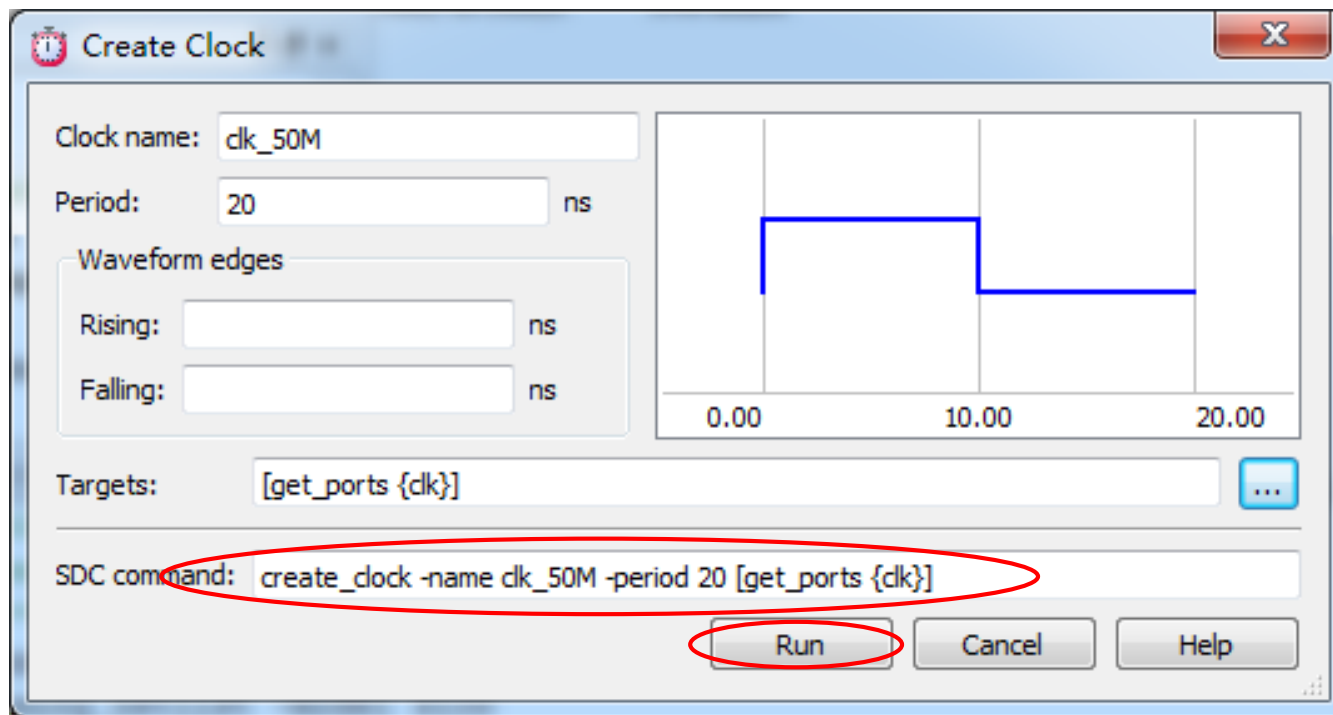
选择clk信号，单击>按钮，将clock添加到右侧列表，之后单击OK





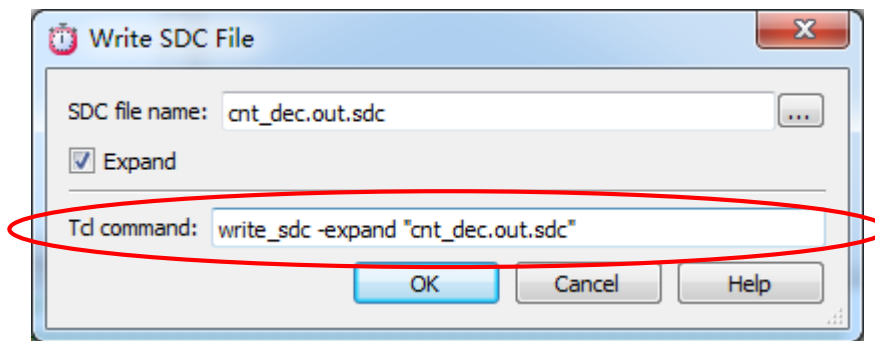
# TimeQuest时序约束

返回之后，在SDC command文本框中出现SDC命令，之后单击Run



# TimeQuest时序约束

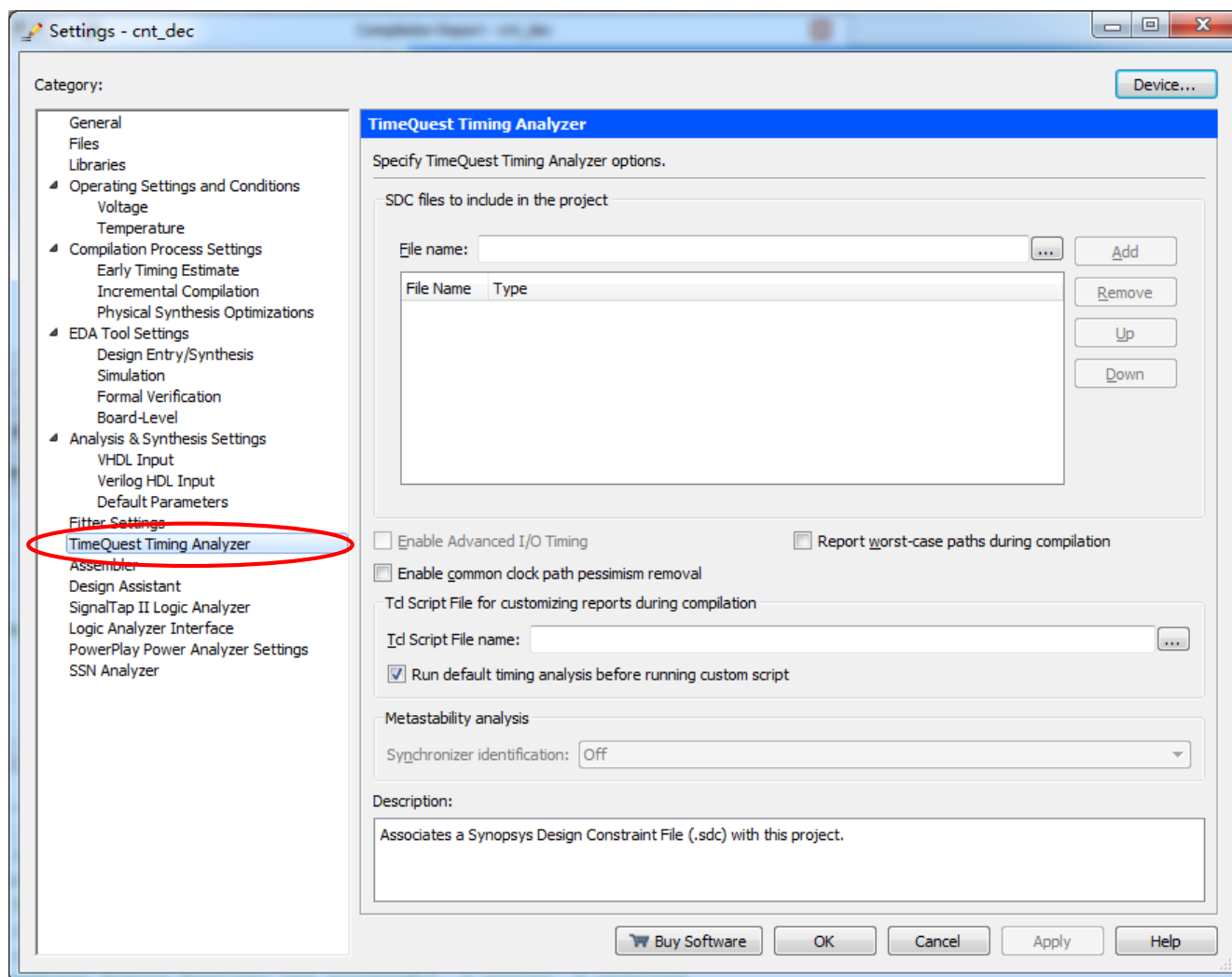
- 回到TimeQuest界面之后，单击Constraints->Write SDC file，用缺省设置，单击OK关闭窗口。写出的SDC文件名通常为“工程名.out.sdc”。
- 之后关闭TimeQuest。





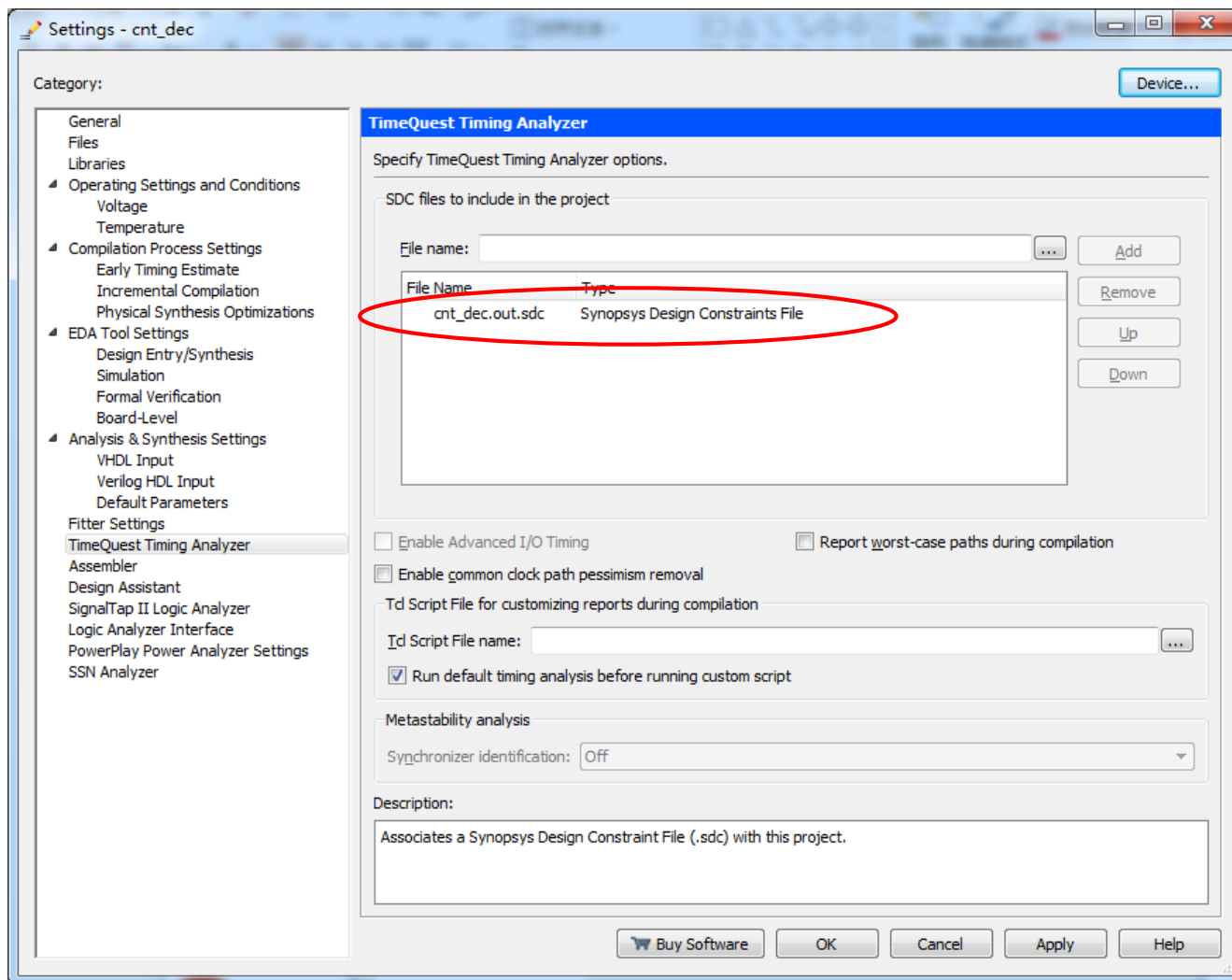
# TimeQuest时序约束

回到QuartusII，单击Assignment->Settings，选择TimeQuest Timing Analyzer



# TimeQuest时序约束

在右侧将生成的SDC文件添加到SDC file列表





# TimeQuest时序约束

重新编译工程，编译完成之后，可以在TimeQuest分析结果中查看时序报告

Quartus II 64-Bit - D:\Temp\cnt\_dec\cnt\_dec - cnt\_dec

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

- Cyclone II: EP2C35F672C6
  - cnt\_dec
    - clk\_gen:U0
    - count:U1
    - BCD7:U2

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  - Datasheet Report
- Fast Model

Compilation Report - cnt\_dec

Slow Model Setup Summary

	Clock	Slack	End Point TNS
1	clk_50M	14.800	0.000

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

Messages

Type ID Message

- 332140 No Removal paths to report
- 332146 Worst-case minimum pulse width slack is 9.000
- 332001 The selected device family is not supported by the report\_metastability command.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements

System (6) Processing (91)

100% 00:00:25