SARVESH SAI RAJESH

40231819

COEN 313 PROJECT

Faculty of Engineering and Computer Science
Expectations of Originality

This form sets out the requirements for originality for work submitted by students in the Faculty of Engineering and Computer Science. Submissions such as assignments, lab reports, project reports, computer programs and take-home exams must conform to the requirements stated on this form and to the Academic Code of Conduct. The course outline may stipulate additional requirements for the course.

1. Your submissions must be your own original work. Group submissions must be the original work of the students in the group.
2. Direct quotations must not exceed 5% of the content of a report, must be enclosed in quotation marks, and must be attributed to the source by a numerical reference citation[1]. Note that engineering reports rarely contain direct quotations.
3. Material paraphrased or taken from a source must be attributed to the source by a numerical reference citation.
4. Text that is inserted from a web site must be enclosed in quotation marks and attributed to the web site by numerical reference citation.
5. Drawings, diagrams, photos, maps or other visual material taken from a source must be attributed to that source by a numerical reference citation.
6. No part of any assignment, lab report or project report submitted for this course can be submitted for any other course.
7. In preparing your submissions, the work of other past or present students cannot be consulted, used, copied, paraphrased or relied upon in any manner whatsoever.
8. Your submissions must consist entirely of your own or your group's ideas, observations, calculations, information and conclusions, except for statements attributed to sources by numerical citation.
9. Your submissions cannot be edited or revised by any other student.
10. For lab reports, the data must be obtained from your own or your lab group's experimental work.
11. For software, the code must be composed by you or by the group submitting the work, except for code that is attributed to its sources by numerical reference.

You must write one of the following statements on each piece of work that you submit:
For individual work: **"I certify that this submission is my original work and meets the Faculty's Expectations of Originality",** with your signature, I.D. #, and the date.
For group work: **"We certify that this submission is the original work of members of the group and meets the Faculty's Expectations of Originality",** with the signatures and I.D. #s of all the team members and the date.

A signed copy of this form must be submitted to the instructor at the beginning of the semester in each course.

I certify that I have read the requirements set out on this form, and that I am aware of these requirements. I certify that all the work I will submit for this course will comply with these requirements and with additional requirements stated in the course outline.

Course Number: COEN 313 Instructor: Prof. Otmane Ait Mohamed
Name: Sarvesh Sai Rajesh I.D. # 40231819
Signature: Sarvesh Sai Rajesh Date: 13th November 2024

[1] Rules for reference citation can be found in "Form and Style" by Patrich MacDonagh and Jack Bordan, fourth edition, May, 2000, available at http://www.encs.concordia.ca/scs/Forms/Form&Style.pdf.
Approved by the ENCS Faculty Council February 10, 2012

Contents

Introduction

As technology advances, efficient monitoring and control of room occupancy have become essential in various fields, particularly in smart building management, public safety, and space optimization. This project aims to develop a digital room occupancy monitoring system that accurately tracks and controls the number of individuals in a room by employing a real-time counting mechanism. The system is designed to enhance safety by preventing overcrowding and ensuring that the room capacity adheres to predetermined limits.

The core functionality of the room occupancy system is to count the number of people entering and exiting a room using two binary signals - one triggered at the entry point and the other at the exit. When the occupancy count reaches a specified maximum threshold, the system outputs an indicator signal to restrict further entry, thus preventing any additional occupants from entering. This monitoring approach is integral to maintaining regulated occupancy levels in various settings, from corporate buildings and educational institutions to healthcare facilities and public venues.

This project employs VHDL (VHSIC Hardware Description Language) to design and simulate the room occupancy tracking system. The VHDL model provides the logic required to update the occupancy count dynamically, while a reset functionality allows the system to reinitialize as needed. The design is synthesized on a Xilinx Nexys A7 FPGA board, taking advantage of FPGA technology for its high-speed operation and resource efficiency. The FPGA platform not only enables real-time processing of occupancy data but also allows for flexible adjustments to the system's configuration, making it suitable for deployment in diverse environments with varying capacity requirements.

In conclusion, the report contains the design methodology, the VHDL code, and the testing procedure employed in the work for the digital room occupancy monitoring system. The results of the simulations as well as the FPGA synthesis validate the design and show that the project meets the objective of using a digital system to meet the needs of modern infrastructure with VHDL designed systems being efficient and adaptable for real time occupancy management applications.

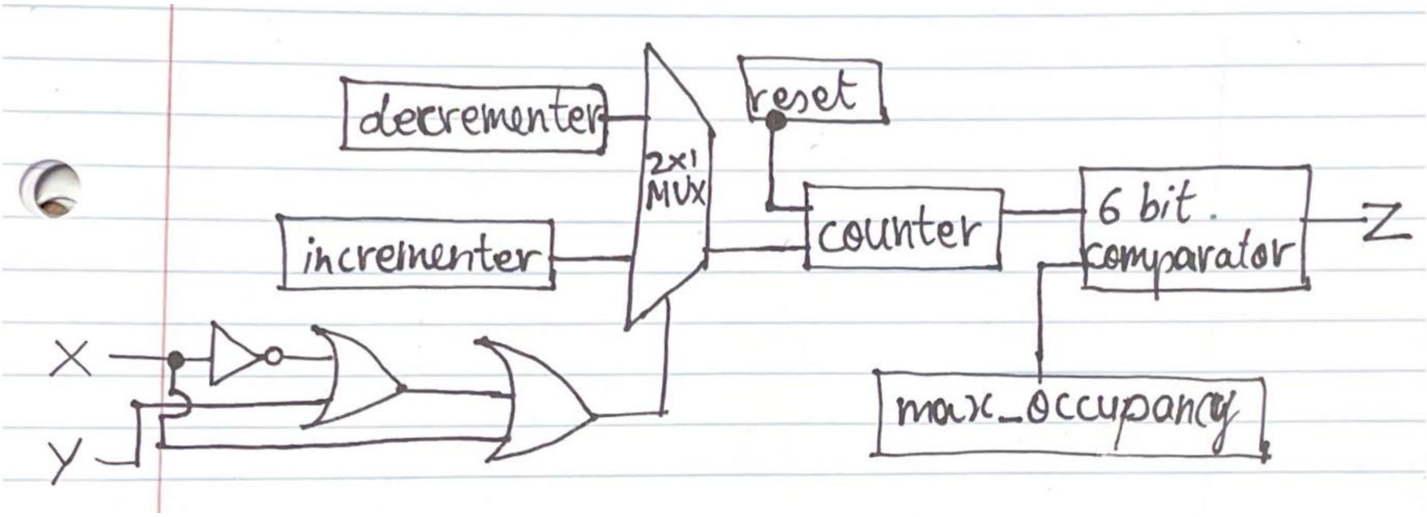
Abstract

This report presents the design, implementation, and verification of a digital room occupancy monitoring system, developed using VHDL (VHSIC Hardware Description Language) for application on an FPGA (Field-Programmable Gate Array) platform. The primary goal of the system is to ensure safe and efficient occupancy management by dynamically tracking the number of individuals within a room and preventing overcrowding through an automated alert system. The system relies on entry and exit sensors that trigger binary signals, updating an internal occupancy count, which is continuously compared against a maximum capacity threshold.

When the occupancy count reaches the specified threshold, the system triggers an indicator to signal that no further entries should be allowed, maintaining adherence to safety regulations. This functionality is crucial in environments such as smart buildings, educational institutions, and public venues, where real-time occupancy control is essential.

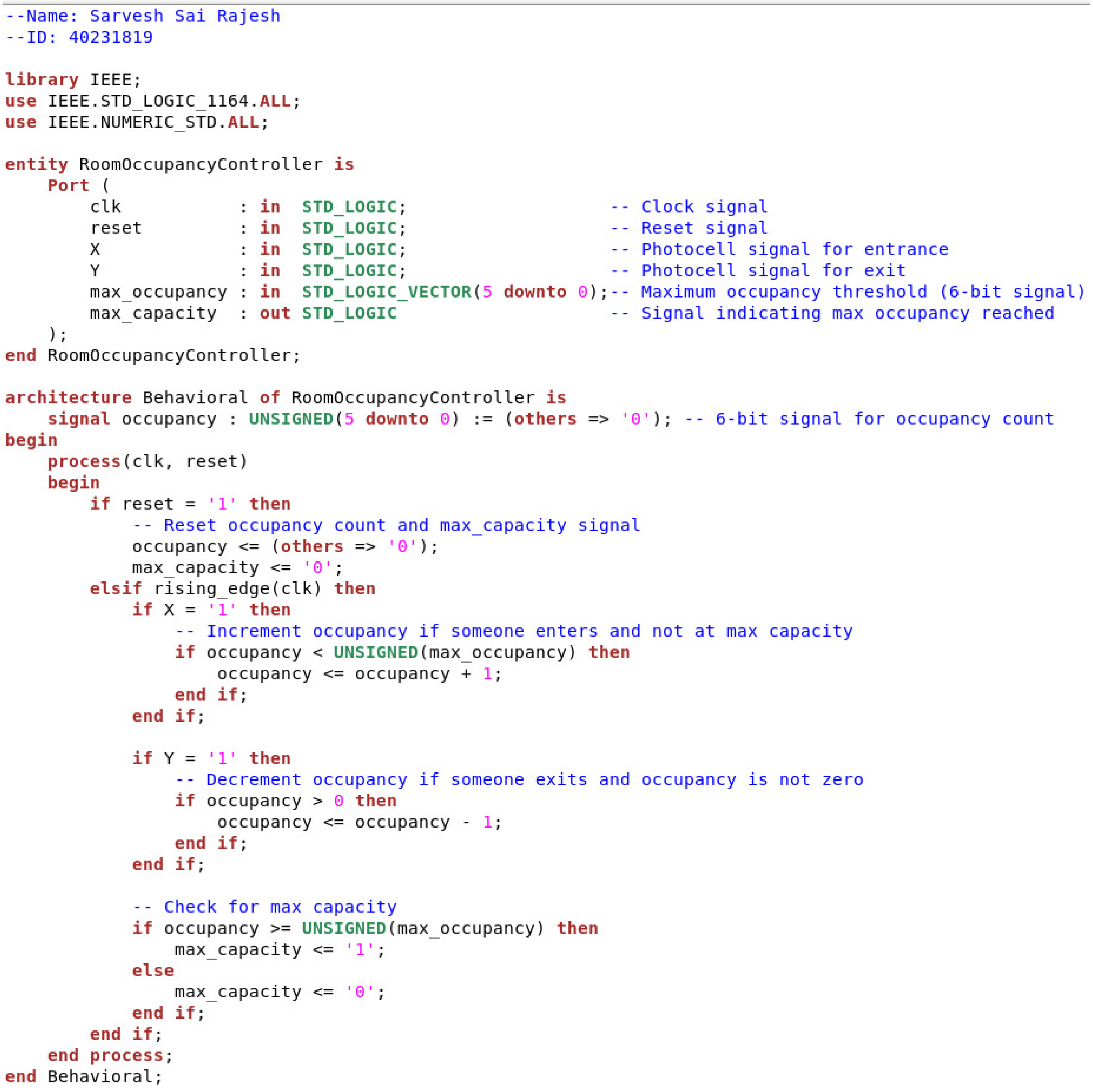
The project focuses on VHDL modeling of the system with the addition of a testbench aimed at testing the functionality of differential entry, exit and reset scenarios. The design is executed and tested with a Xilinx Nexys A7 FPGA board while the speed, utilization of resources and reliability are used to evaluate the results. From the simulation results, it is certain that the system works well in the defined operational region and the synthesis was able to utilize the FPGA resources well. The project in particular demonstrates the relevance and the potential of using VHDL and FPGAs in developing flexible, resilient, and real time monitoring reports for the present day infrastructural requirements.

Conceptual Diagram:



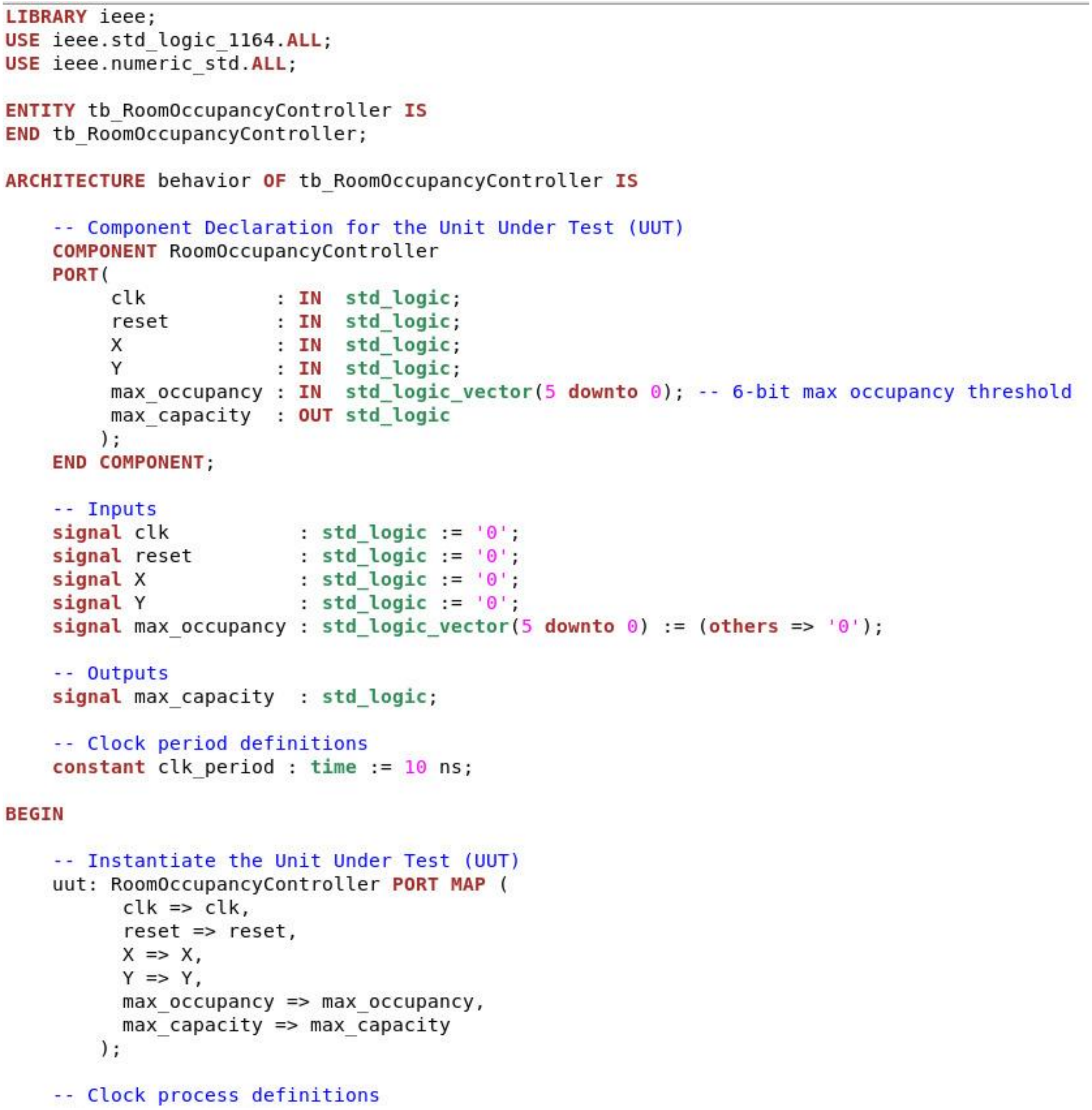
VHDL CODE:

RoomOccupancyController.vhd:



```
--Name: Sarvesh Sai Rajesh
--ID: 40231819

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity RoomOccupancyController is
    Port (
        clk           : in  STD_LOGIC;                    -- Clock signal
        reset         : in  STD_LOGIC;                    -- Reset signal
        X             : in  STD_LOGIC;                    -- Photocell signal for entrance
        Y             : in  STD_LOGIC;                    -- Photocell signal for exit
        max_occupancy : in  STD_LOGIC_VECTOR(5 downto 0);-- Maximum occupancy threshold (6-bit signal)
        max_capacity  : out STD_LOGIC                     -- Signal indicating max occupancy reached
    );
end RoomOccupancyController;

architecture Behavioral of RoomOccupancyController is
    signal occupancy : UNSIGNED(5 downto 0) := (others => '0'); -- 6-bit signal for occupancy count
begin
    process(clk, reset)
    begin
        if reset = '1' then
            -- Reset occupancy count and max_capacity signal
            occupancy <= (others => '0');
            max_capacity <= '0';
        elsif rising_edge(clk) then
            if X = '1' then
                -- Increment occupancy if someone enters and not at max capacity
                if occupancy < UNSIGNED(max_occupancy) then
                    occupancy <= occupancy + 1;
                end if;
            end if;

            if Y = '1' then
                -- Decrement occupancy if someone exits and occupancy is not zero
                if occupancy > 0 then
                    occupancy <= occupancy - 1;
                end if;
            end if;

            -- Check for max capacity
            if occupancy >= UNSIGNED(max_occupancy) then
                max_capacity <= '1';
            else
                max_capacity <= '0';
            end if;
        end if;
    end process;
end Behavioral;
```

tb_RoomOccupancyController.vhd:

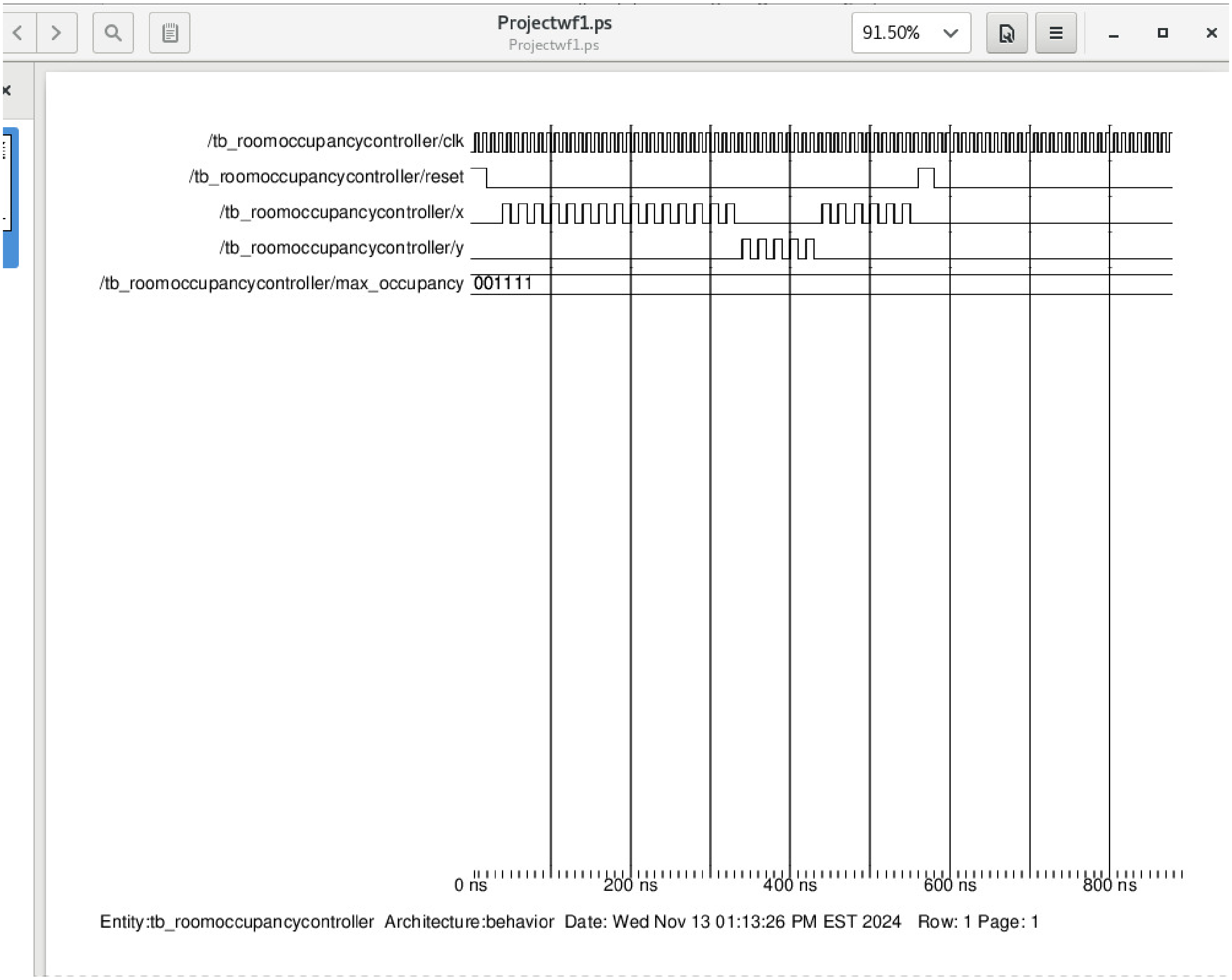


```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY tb_RoomOccupancyController IS
END tb_RoomOccupancyController;

ARCHITECTURE behavior OF tb_RoomOccupancyController IS

    -- Component Declaration for the Unit Under Test (UUT)
    COMPONENT RoomOccupancyController
    PORT(
         clk           : IN  std_logic;
         reset         : IN  std_logic;
         X             : IN  std_logic;
         Y             : IN  std_logic;
         max_occupancy : IN  std_logic_vector(5 downto 0); -- 6-bit max occupancy threshold
         max_capacity  : OUT std_logic
        );
    END COMPONENT;

    -- Inputs
    signal clk           : std_logic := '0';
    signal reset         : std_logic := '0';
    signal X             : std_logic := '0';
    signal Y             : std_logic := '0';
    signal max_occupancy : std_logic_vector(5 downto 0) := (others => '0');

    -- Outputs
    signal max_capacity  : std_logic;

    -- Clock period definitions
    constant clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test (UUT)
    uut: RoomOccupancyController PORT MAP (
          clk => clk,
          reset => reset,
          X => X,
          Y => Y,
          max_occupancy => max_occupancy,
          max_capacity => max_capacity
        );

    -- Clock process definitions
    -- Clock process definitions
    clk_process :process
    begin
        clk <= '0';
        wait for clk_period/2;
        clk <= '1';
        wait for clk_period/2;
    end process;

    -- Testbench process
    stim_proc: process
    begin
        -- Scenario 1: Reset and set max occupancy to 15
        reset <= '1';
        max_occupancy <= "001111"; -- Set max occupancy to 15 (within 6-bit limit)
        wait for 20 ns;
        reset <= '0';
        wait for 20 ns;

        -- Scenario 2: Simulate entry of 15 people
        for i in 1 to 15 loop
            X <= '1'; wait for clk_period;
            X <= '0'; wait for clk_period;
        end loop;

        -- Scenario 3: Simulate exit of 5 people
        for i in 1 to 5 loop
            Y <= '1'; wait for clk_period;
            Y <= '0'; wait for clk_period;
        end loop;

        -- Scenario 4: Simulate entry of 1 person, should not trigger max_capacity
        X <= '1'; wait for clk_period;
        X <= '0'; wait for clk_period;

        -- Scenario 5: Simulate max capacity reached
        for i in 1 to 5 loop
            X <= '1'; wait for clk_period;
            X <= '0'; wait for clk_period;
        end loop;

        -- Scenario 6: Simulate reset at max capacity
        reset <= '1'; wait for 20 ns;
        reset <= '0';
        wait;

    end process;
END behavior;
```

Quality of Design:

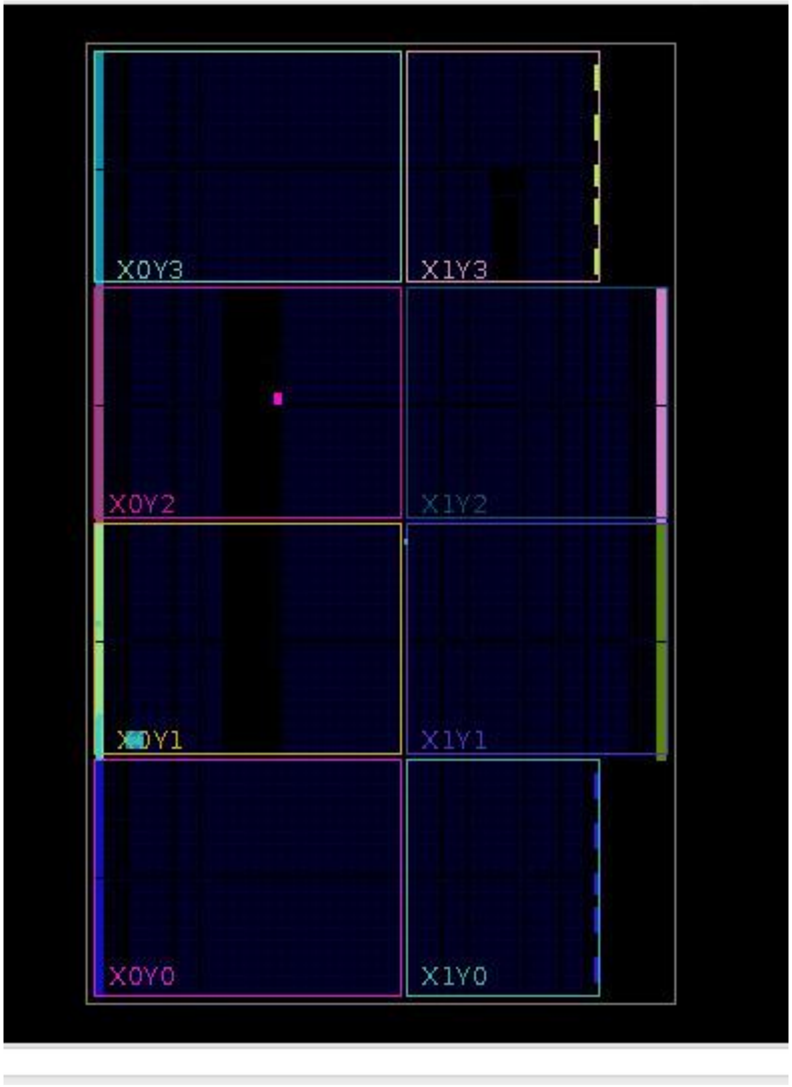
The VHDL code for the room occupancy monitoring system is well-structured, readable, and adheres to the design requirements. It uses clear signal names, modular processes, and efficient 6-bit occupancy tracking to manage hardware resources. The design includes robust checks to prevent invalid states, such as occupancy dropping below zero or exceeding the maximum threshold. A comprehensive testbench covers a range of scenarios - reset, entry, exit, and capacity limits - to verify functionality and ensure reliability. This modular and adaptable code supports scalability, allowing easy adjustments for different occupancy limits. Overall, the code demonstrates good engineering practices in digital design.

SIMULATION AND SYNTHESIS RESULTS:

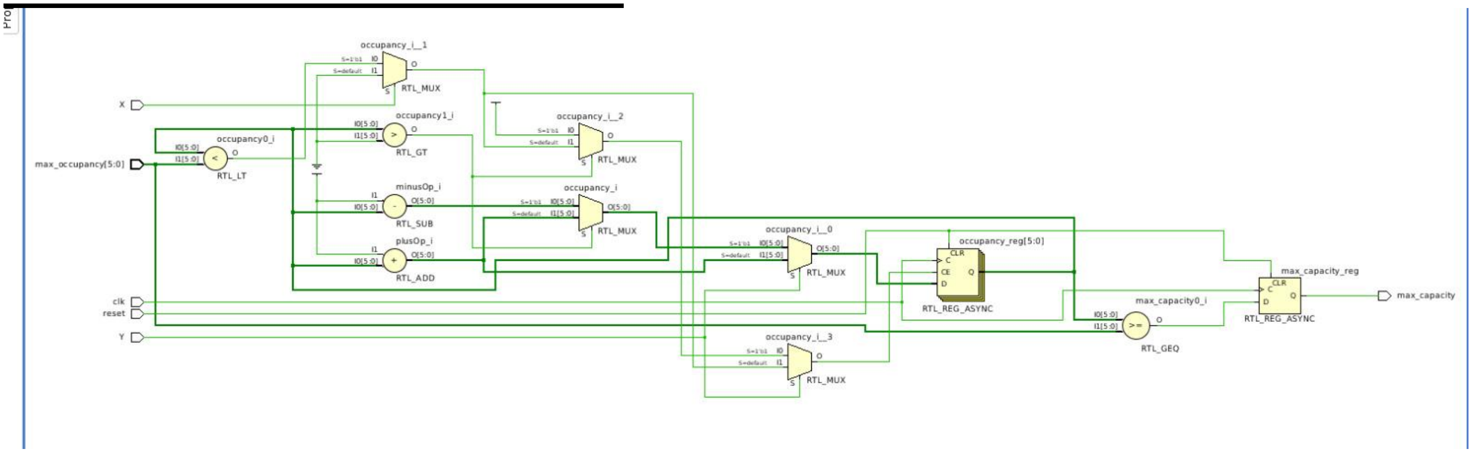

Projectwf1.ps
Projectwf1.ps
91.50%
/tb_roomoccupancycontroller/clk
/tb_roomoccupancycontroller/reset
/tb_roomoccupancycontroller/x
/tb_roomoccupancycontroller/y
/tb_roomoccupancycontroller/max_occupancy
001111
0 ns
200 ns
400 ns
600 ns
800 ns

Entity:tb_roomoccupancycontroller Architecture:behavior Date: Wed Nov 13 01:13:26 PM EST 2024 Row: 1 Page: 1

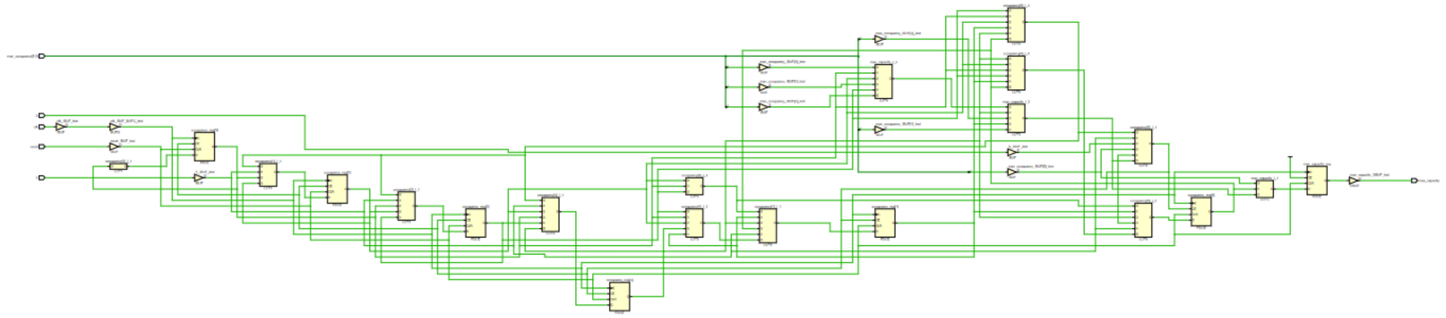
Implemented Design:



Elaborated RTL View Schematics:



Synthesis Schematic:



Vivado Log File:

```
*** Running vivado
    with args -log RoomOccupancyController.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -
notrace -source RoomOccupancyController.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source RoomOccupancyController.tcl -notrace
Command: synth_design -top RoomOccupancyController -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 14473
---------------------------------------------------------------------------------
Starting Synthesize : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.582 ; gain =
85.801 ; free physical = 9948 ; free virtual = 22084
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'RoomOccupancyController'
[/nfs/home/s/sa_rajes/COEN313/PROJECT/RoomOccupancyController.vhd:16]
INFO: [Synth 8-256] done synthesizing module 'RoomOccupancyController' (1#1)
[/nfs/home/s/sa_rajes/COEN313/PROJECT/RoomOccupancyController.vhd:16]
---------------------------------------------------------------------------------
Finished Synthesize : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1446.223 ; gain =
130.441 ; free physical = 9960 ; free virtual = 22097
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1446.223
; gain = 130.441 ; free physical = 9960 ; free virtual = 22097
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB):
peak = 1454.219 ; gain = 138.438 ; free physical = 9959 ; free virtual = 22096
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak =
1462.223 ; gain = 146.441 ; free physical = 9950 ; free virtual = 22087
```

```
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
No constraint files found.
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
	   2 Input      6 Bit       Adders := 3
+---Registers :
	                6 Bit    Registers := 1
	                1 Bit    Registers := 1
+---Muxes :
	   2 Input      6 Bit        Muxes := 2
	   2 Input      1 Bit        Muxes := 2
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module RoomOccupancyController
Detailed RTL Component Info :
+---Adders :
	   2 Input      6 Bit       Adders := 3
+---Registers :
	                6 Bit    Registers := 1
	                1 Bit    Registers := 1
+---Muxes :
	   2 Input      6 Bit        Muxes := 2
	   2 Input      1 Bit        Muxes := 2
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
No constraint files found.
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
```

```
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:05 ; elapsed = 00:00:19 . Memory (MB): peak = 1596.055 ; gain = 280.273 ; free physical = 9784 ; free virtual = 21922
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
No constraint files found.
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak = 1596.055 ; gain = 280.273 ; free physical = 9784 ; free virtual = 21922
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak = 1596.055 ; gain = 280.273 ; free physical = 9783 ; free virtual = 21921
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
```

```
Finished Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak = 1596.055 ; gain =
280.273 ; free physical = 9783 ; free virtual = 21921
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Renaming Generated Instances
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak =
1596.055 ; gain = 280.273 ; free physical = 9783 ; free virtual = 21921
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak =
1596.055 ; gain = 280.273 ; free physical = 9783 ; free virtual = 21921
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Ports
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak =
1596.055 ; gain = 280.273 ; free physical = 9783 ; free virtual = 21921
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak =
1596.055 ; gain = 280.273 ; free physical = 9783 ; free virtual = 21921
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak =
1596.055 ; gain = 280.273 ; free physical = 9783 ; free virtual = 21921
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT3 |     2|
|4     |LUT4 |     1|
|5     |LUT5 |     3|
|6     |LUT6 |     7|
|7     |FDCE |     7|
|8     |IBUF |    10|
|9     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    33|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak =
1596.055 ; gain = 280.273 ; free physical = 9783 ; free virtual = 21921
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak =
1596.055 ; gain = 280.273 ; free physical = 9786 ; free virtual = 21923
Synthesis Optimization Complete : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak =
1596.055 ; gain = 280.273 ; free physical = 9795 ; free virtual = 21933
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 10 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
11 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
```

```
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:21 . Memory (MB): peak = 1748.023 ; gain = 444.895 ;
free physical = 9754 ; free virtual = 21892
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint
'/nfs/home/s/sa_rajes/COEN313/PROJECT/COEN313Projectt/COEN313Projectt.runs/synth_1/RoomOccupancy
Controller.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file RoomOccupancyController_utilization_synth.rpt -pb
RoomOccupancyController_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 1772.047 ; gain =
0.000 ; free physical = 9755 ; free virtual = 21893
INFO: [Common 17-206] Exiting Vivado at Wed Nov 13 15:49:58 2024...
```