1. Description

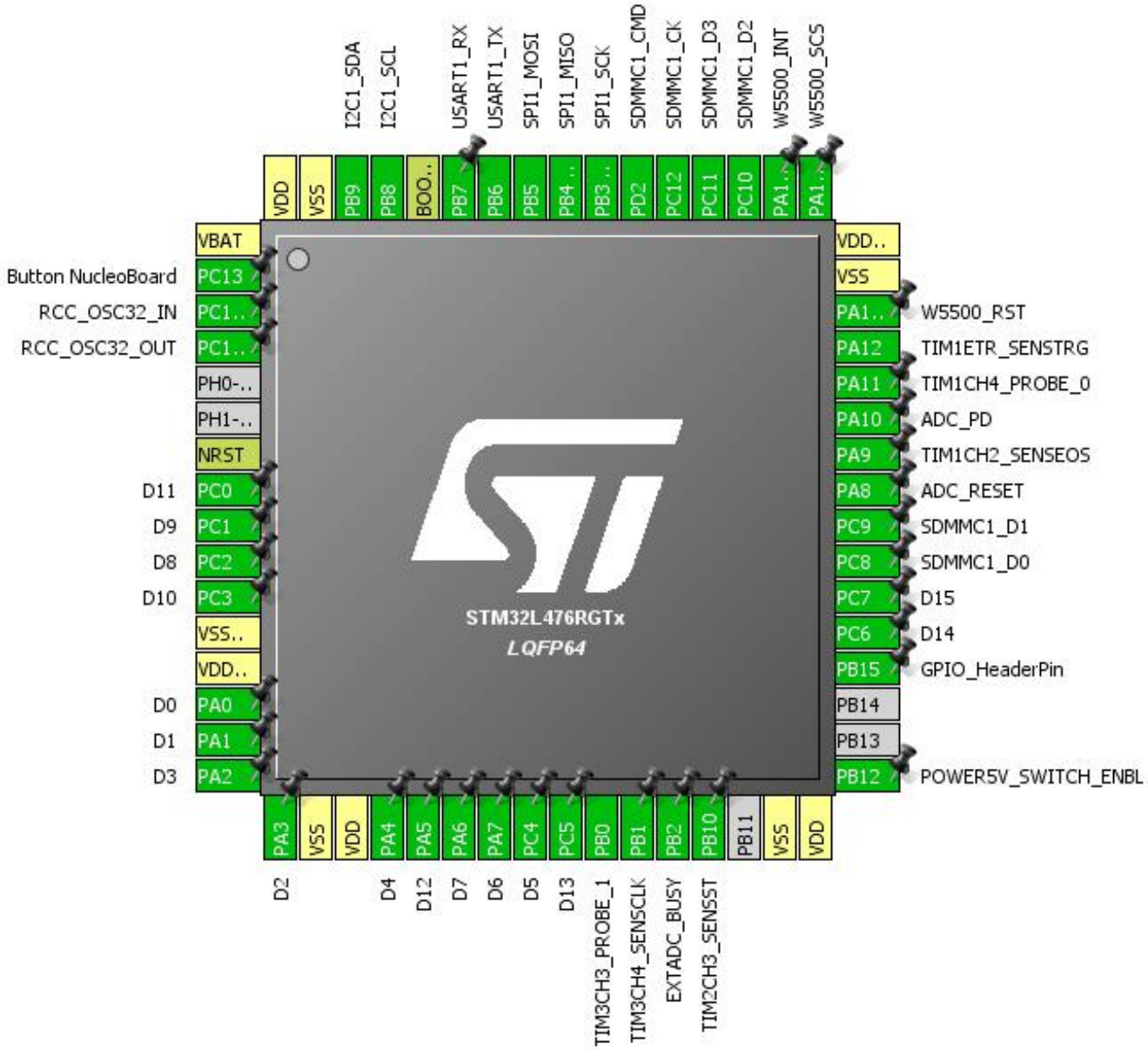
1.1. Project

Project Name	minispec_CubeMX
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 4.23.0
Date	11/22/2018

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



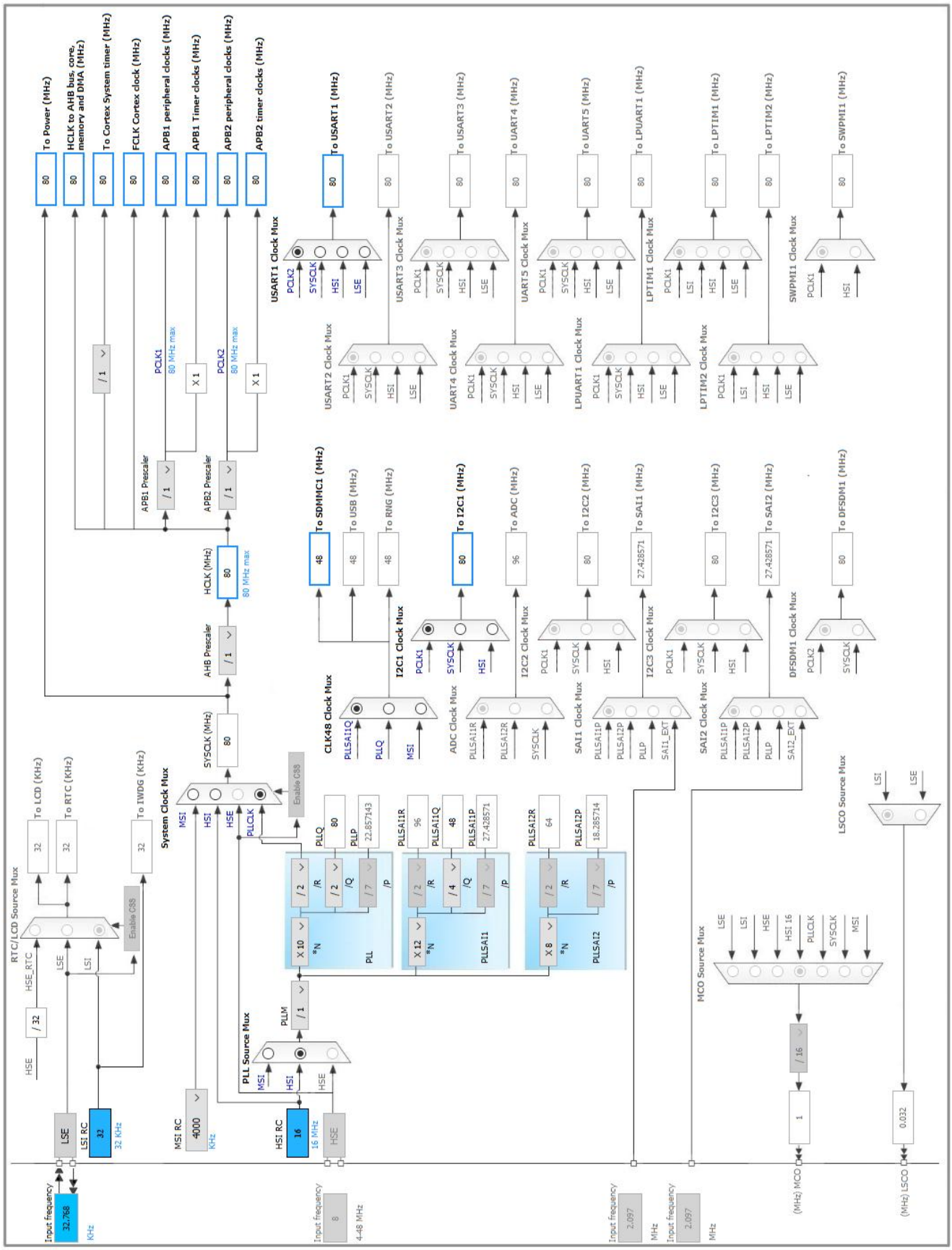
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	Button NucleoBoard
3	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	D11
9	PC1 *	I/O	GPIO_Input	D9
10	PC2 *	I/O	GPIO_Input	D8
11	PC3 *	I/O	GPIO_Input	D10
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0 *	I/O	GPIO_Input	D0
15	PA1 *	I/O	GPIO_Input	D1
16	PA2 *	I/O	GPIO_Input	D3
17	PA3 *	I/O	GPIO_Input	D2
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Input	D4
21	PA5 *	I/O	GPIO_Input	D12
22	PA6 *	I/O	GPIO_Input	D7
23	PA7 *	I/O	GPIO_Input	D6
24	PC4 *	I/O	GPIO_Input	D5
25	PC5 *	I/O	GPIO_Input	D13
26	PB0	I/O	TIM3_CH3	TIM3CH3_PROBE_1
27	PB1	I/O	TIM3_CH4	TIM3CH4_SENSCLK
28	PB2	I/O	GPIO_EXTI2	EXTADC_BUSY
29	PB10	I/O	TIM2_CH3	TIM2CH3_SENSST
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	POWER5V_SWITCH_ENBL
36	PB15 *	I/O	GPIO_Input	GPIO_HeaderPin
37	PC6 *	I/O	GPIO_Input	D14
38	PC7 *	I/O	GPIO_Input	D15
39	PC8	I/O	SDMMC1_D0	
40	PC9	I/O	SDMMC1_D1	
41	PA8 *	I/O	GPIO_Output	ADC_RESET

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PA9	I/O	TIM1_CH2	TIM1CH2_SENSEOS
43	PA10 *	I/O	GPIO_Output	ADC_PD
44	PA11	I/O	TIM1_CH4	TIM1CH4_PROBE_0
45	PA12	I/O	TIM1_ETR	TIM1ETR_SENSTRG
46	PA13 (JTMS-SWDIO) *	I/O	GPIO_Output	W5500_RST
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK) *	I/O	GPIO_Output	W5500_SCS
50	PA15 (JTDI) *	I/O	GPIO_Input	W5500_INT
51	PC10	I/O	SDMMC1_D2	
52	PC11	I/O	SDMMC1_D3	
53	PC12	I/O	SDMMC1_CK	
54	PD2	I/O	SDMMC1_CMD	
55	PB3 (JTDO-TRACESWO)	I/O	SPI1_SCK	
56	PB4 (NJTRST)	I/O	SPI1_MISO	
57	PB5	I/O	SPI1_MOSI	
58	PB6	I/O	USART1_TX	
59	PB7	I/O	USART1_RX	
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. I2C1

I2C: I2C

5.1.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10909CEC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.2. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled

HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

5.3. SDMMC1

Mode: SD 4 bits Wide bus

5.3.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

5.4. SPI1

Mode: Full-Duplex Master

5.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**40.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.5. SYS

Timebase Source: SysTick

5.6. TIM1

Slave Mode: Trigger Mode
Trigger Source: ITR1
Clock Source : ETR2
Channel2: Input Capture direct mode
Channel4: PWM Generation CH4
mode: One Pulse Mode

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**300 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	Trigger Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High

BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clock:

Clock Filter (4 bits value)	0
Clock Polarity	**Inverted ***
Clock Prescaler	Prescaler not used

Clear Input:

Clear Input Source	Disable

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

PWM Generation Channel 4:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	**80 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.7. TIM2

Slave Mode: External Clock Mode 1
Trigger Source: ITR2
Channel3: PWM Generation CH3
mode: One Pulse Mode

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1100 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode	**Enable (sync between this TIM (Master) and its Slaves (through TRGO)) ***
Trigger Event Selection TRGO	**Update Event ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	**PWM mode 2 ***
Pulse (32 bits value)	**1 ***
Fast Mode	Disable
CH Polarity	High

5.8. TIM3

Clock Source : Internal Clock
Channel3: Output Compare CH3
Channel4: Output Compare CH4

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**39 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	**Enable (sync between this TIM (Master) and its Slaves (through TRGO)) ***
Trigger Event Selection TRGO	**Output Compare (OC3REF) ***

Clear Input:

Clear Input Source	Disable

Output Compare Channel 3:

Mode	**Toggle on match ***
Pulse (16 bits value)	**10 ***
CH Polarity	High

Output Compare Channel 4:

Mode	**Toggle on match ***
Pulse (16 bits value)	**30 ***
CH Polarity	High

5.9. TIM5

Slave Mode: Trigger Mode
Trigger Source: ITR0
mode: Clock Source
mode: One Pulse Mode

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**80 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**500 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	Trigger Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.10. USART1

Mode: Asynchronous

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PB3 (JTDO-TRACESWO)	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4 (NJTRST)	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
TIM1	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1CH2_SENSEOS
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1CH4_PROBE_0
	PA12	TIM1_ETR	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1ETR_SENSTRG
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM2CH3_SENSST
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3CH3_PROBE_1
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3CH4_SENSCLK
USART1	PB6	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PB7	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Button NucleoBoard

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D11
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D9
	PC2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D8
	PC3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D10
	PA0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D0
	PA1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D1
	PA2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D3
	PA3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D2
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D4
	PA5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D12
	PA6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D7
	PA7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D6
	PC4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D5
	PC5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D13
	PB2	GPIO_EXTI2	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	EXTADC_BUSY
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	POWER5V_SWITCH_ENBL
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_HeaderPin
	PC6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D14
	PC7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D15
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADC_RESET
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADC_PD
	PA13 (JTMS-SWDIO)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	W5500_RST
	PA14 (JTCK-SWCLK)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	W5500_SCS
	PA15 (JTDI)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	W5500_INT

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line2 interrupt	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM5 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
USART1 global interrupt	unused		
SDMMC1 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	025976_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.0

8. Software Project

8.1. Project Settings

Name	Value
Project Name	minispec_CubeMX
Project Folder	C:\Users\remmlerp\Documents\Altium\2018
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_L4 V1.10.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No