TECHNICAL SPECIFICATION

Model Number : GDEW075C21

Description : Screen Size: 7.5"
Color: Black, White and Red
Display Resolution: 640*384

Chengdu Heltec Automation technology CO., LTD.

Revision History

Rev.	Issued Date	Revised Contents
1.0	Jul.01.2015	Preliminary
1.1	Aug.17.2015	1. In part 12: Delete block diagram.
1.2	Sep.21.2015	1. Modify GDEW075Z08 to GDEW075Z09.
1.3	Nov.04.2015	1. In part 11: Modify T=+40℃, RH=80% for 168 hrs to 240 hrs.
2.0	Mar.01.2017	1. In part 7-5): Modify Reference Circuit.

TECHNICAL SPECIFICATION

CONTENTS

1. Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 7.5" active area contains 640×384 pixels, and has 3-bit white/black/red full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

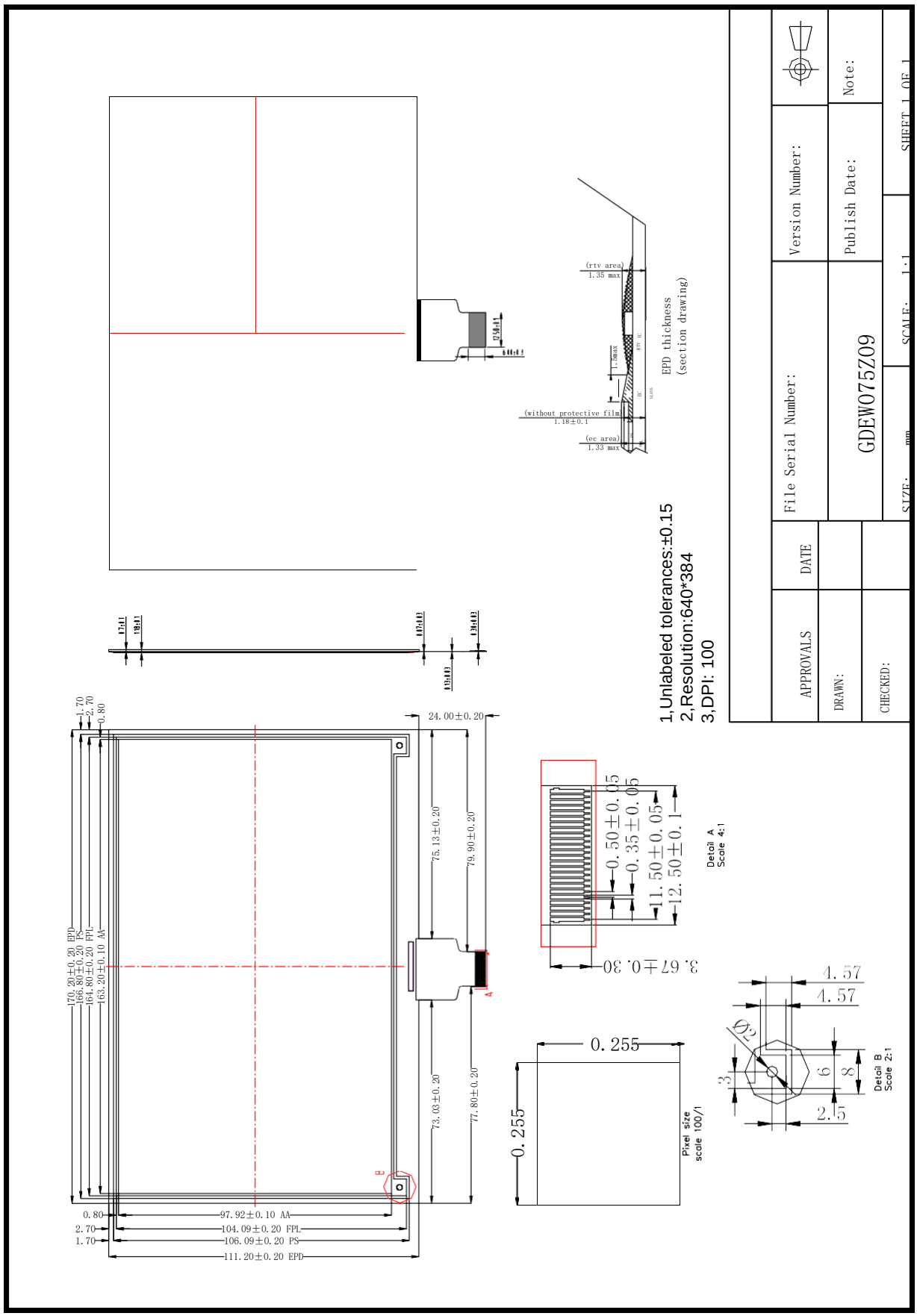
2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current sleep mode
- On chip display RAM
- External SPI flash/eeprom for Qiyun Display
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 280um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.5	Inch	
Display Resolution	640(H) ×384(V)	Pixel	Dpi:100
Active Area	163.20(H) ×97.92(V)	mm	
Pixel Pitch	0.255 ×0.255	mm	
Pixel Configuration	Rectangle		
Outline Dimension	170.20(H) ×111.20(V) ×1.18(D)	mm	
Weight	43.75±0.5	g	

4. Mechanical Drawing of EPD module



5. Input/Output Terminals

5-1) Pin out List

Pin #	Type	Single	Description	Remark
1	I	MFCSB	Serial communication chip select. It would bypass to MFCSB by R61H command.	
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 5-5
9	O	BUSY	Busy state output pin	Note 5-4
10	I	RES #	Reset	Note 5-3
11	I	D/C #	Data /Command control pin	Note 5-2
12	I	CS #	Chip Select input pin	Note 5-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	O	FMSDO	Serial communication data output. It would bypass to FMSDO by R61H command.	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled High, the data will be interpreted

as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

6. Command Table

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel setting(PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	-	#	#	#	#	RES[1],RES[0], LUT_EN, UD,SHL,SHD_N,RST_N	0Fh
		0	1	-	-	-	#	-	-	-	-	VCM_HZ	00h
2	Power setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	#	#	-	#	#	#	EDATA_SEL, EDATA_SET, VSource_LV_EN, VSource _EN, VGate_EN	07h
		0	1	-	-	-	-	-	#	#	#	VGHL_LV[1:0]	01h
		0	1	-	-	#	#	#	#	#	#	VDPS_LV[5:0]	05h
		0	1	-	-	#	#	#	#	#	#	VDNS_LV[5:0]	05h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting(PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OFF[1:0]	00h
5	Power ON(PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	00h
		0	1			#	#	#	#	#	#	BT_PHC[5:0]	00h
7	Deep sleep(DSLP)	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check code	A5h
8	Data Start Transmission 1 (DTM1) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	-	#	#	#	-	#	#	#	KPixel1[2:0], KPixel2[2:0]	00h
		0	1	..	..	..	..	..	..	..	..	..	..
		0	1	-	#	#	#	-	#	#	#	Kpixel[2M-1][2:0], Kpixel[2M][2:0]	00h
9	Data Stop(DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-	Data_flag	-
10	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
11	Image Process Command (IPC)	0	0	0	0	0	1	0	0	1	1		13h
		0	1	-	-	-	#	-	#	#	#	IP_EN, IP_SEL[2:0]	00h
12	VCOM LUT(LUTC) (221-byte command, bytes 2-12 repeated 20 times)	0	0	0	0	1	0	0	0	0	0		20h
13	LUT Blue(LUTB) (261-byte command, bytes 2-14 repeated 20 times)	0	0	0	0	1	0	0	0	0	1		21h
14	LUT White (LUTW) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	0	1	0		22h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	LUT Gray1(LUTG1) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	0	1	1		23h
16	LUT Gray2(LUTG2) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	0	0		24h
17	LUT Red0(LUTR0) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	0	1		25h
18	LUT Red1(LUTR1) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	1	0		26h
19	LUT Red2(LUTR2) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	1	1		27h
20	LUT Red3(LUTR3) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	1	0	0	0		28h
21	LUT XON (LUTXON) (201-byte command, bytes 2~11 repeated 20 times)	0	0	0	0	1	0	1	0	0	1		29h
22	PLL control(PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	-	#	#	#	#	#	#	M[2:0], N[2:0]	3Ch
23	Temperature Sensor Command (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3]/TS[7:1]	00h
		1	1	#	#	#	-	-	-	-	-	D[2:0]/TS[0]	00h
24	Temperature Sensor Calibration (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	-	-	-	-	TSE	00h
25	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
26	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
27	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[2:0], DDX, CDI[3:0]	F7h
28	Lower Power Detection(LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	-	-	-	-	-	-	-	-	#	LPD	01h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
29	TCON Setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
30	TCON resolution (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	#	#	#	#	#	#	#	#	HRES[9:0]	00h
		0	1	-	-	-	-	-	-	#	#		00h
		0	1	-	-	-	-	-	-	-	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
31	SPI flash control (DAM)	0	0	0	1	1	0	0	1	0	1		65h
		0	1	-	-	-	-	-	-	-	#	DAM	00h
32	Revision(REV)	0	0	0	1	1	1	0	0	0	0		70h
		0	1	-	-	#	#	#	#	#	#	MAN,SHRK,LUT_REV[3:0]	00h
33	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	-	#	#	#	#	#	#	I^2C_ERR,I^2C_BUSY, DATA_FLAG, PON, POF, BUSY	02h
34	Auto Measurement Vcom (AMV)	0	0	1	0	0	0	0	0	0	0		80h
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0],AMVX,AMVS, AMV,AMVE	10h
35	Read Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	#	#	#	#	#	#	#	VV[6:0]	00h
36	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	#	#	#	#	#	#	#	VDCS[6:0]	02h

1) Panel Setting (PSR) (R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	LUT_EN	-	UD	SHL	SHD_N	RST_N

RES[1:0]: Display resolution setting (source×gate)

00b: 640×480 (default)

01b: 600×450

10b: 640×448

11b: 600×448

LUT_EN: LUT selection

0: Using LUT from external Flash.

1: Using LUT from register.

UD: Gate Scan Direction

0: Scan down First line to last: Gn→……→G1

1: Scan up. (default) First line to last: G1→ ……→Gn

SHL: Source shift direction

0: Shift left. First data to last data: Sn→……→S1

1: Shift right First data to last data: S1→……→Sn

SHD_N: Booster switch

0: DC-DC converter OFF.

1: DC-DC converter ON (Default)

When SHD_N become low, DC-DC will turn OFF. Register and SRAM data will keep until VDD OFF. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.

RST_N: Soft Reset

0: The controller is reset. Reset all registers to their default value.

1: Normal operation (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V

When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

VCM_HZ: VCOM Hi-Z function

0: VCOM normal output. (Default)

1: VCOM floating.

2) Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0	0	1
Selecting	0	1	-	-	EDATA_SEL	EDATA_SET	-	VSource_LV_EN	VSource_EN	VGate_EN
Internal/External	0	1	-	-	-	-	-	-	VGHL_LVL[1:0]	
Power	0	1	-	-	VDPS_LV[5:0]					
	0	1	-	-	VDNS_LV[5:0]					

EDATA_SEL: EDATA selection for pure driver mode

0 : When EDATA_SET=1, pixel bit =2`b11 output VDPS_L level

1 : When EDATA_SET=1, pixel bit =2`b11 output VDNS_L level (default)

EDATA_SET: EDATA setting for pure driver mode

0: 3-bit data mode for pure driver

1: 2-bit data mode for pure driver (default)

Vsource_LV_EN: VSource LV power selection.

0: External source power from VSH_LV and VSL_LV pin.

1: Internal DCDC function for generate source power. (default)

VSource_EN: VSource power selection.

0: External source power from VSH and VSL pin.

1: Internal DCDC function for generate source power. (default)

VGate_EN: VGate power selection.

0: External gate power from VGH and VGL pin.

1: Internal DCDC function for generate gate power. (default)

VGHL_LVL[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage level
00	VGH=20V, VGL= -20V
01 (Default)	VGH=19V, VGL= -19V
10	VGH=18V, VGL= -18V
11	VGH=17V, VGL= -17V

VDPS_LV[5:0]: Internal VDH power selection for Red LUT.

VDPS_LV	VDH_V
000000	3.0V
000001	3.2V
000010	3.4V
000011	3.6V
000100	3.8V
000101	4.0V (Default)
..	..
111100	15.0V

VDNS_LV[5:0]: Internal VDL power selection for Red LUT.

VDNS_LV	VDL_V
000000	-3.0V
000001	-3.2V
000010	-3.4V
000011	-3.6V
000100	-3.8V
000101	-4.0V (Default)
..	..
111100	-15.0V

3) Power OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After power off command, driver will power off based on the Power OFF Sequence, BUSY signal will become “0”.

The Power OFF command will turn off DCDC, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data

will keep until VDD off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

4) Power OFF Sequence Setting(PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF Sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, driver will power on based on the Power ON Sequence.

After power on command and all power sequence are ready, then BUSY signal will become “1”.

6) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Booster Soft Start	0	0	0	0	0	0	0	1	0	0
	0	1	BTPHA7	BTPHA6	BTPHA5	BTPHA4	BTPHA3	BTPHA2	BTPHA1	BTPHA0
	0	1	BTPHB7	BTPHB6	BTPHB5	BTPHB4	BTPHB3	BTPHB2	BTPHB1	BTPHB0
	0	1			BTPHC5	BTPHC4	BTPHC3	BTPHC2	BTPHC1	BTPHC0

Name	Control	Value	Description
BT_PHA[7:6] BT_PHB[7:6]	Soft Start Phase Period	**00**	10ms
		01	20ms
		10	30ms
		11	40ms
BT_PHA[5:3] BT_PHB[5:3] BT_PHC[5:3]	Driving Strength	000	1
		001	2
		010	3
		011	4
		100	5
		101	6
		110	7
		111	8

Name	Control	Value	Description
BT_PHA[2:0] BT_PHB[2:0] BT_PHC[2:0]	Min. OFF Time	000	0.26us
		001	0.31us
		010	0.36us
		011	0.52us
		100	0.77us
		101	1.61us
		110	3.43us
		111	6.77us

7) Deep sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hard ward reset assertion.

The only one parameter is a check code, the command would be executed if check code is A5h.

8) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Dummy	KPixel12	KPixel11	KPixel10	Dummy	KPixel22	Kpixel21	Kpixel20
	0	1	..	..	..	..	..	..	..	..
	0	1	Dummy	Kpixel (2M-1)2	Kpixel (2M-1)1	Kpixel (2M-1)0	Dummy	Kpixel (2M)2	Kpixel (2M)1	Kpixel (2M)0

This Command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Datastop command (R11H). Then the chip will start to send data/VCOM for panel.

Kpixel[1~2M][2:0] :

Kpixel [2:0]	Source Driver Output	
	DDX=1(default)	DDX=0
	LUT	LUT
000	Black	White
001	Gray1	Gray2
010	Gray2	Gray1
011	White	Black
100	Red0	Red3
101	Red1	Red2
110	Red2	Red1
111	Red3	Red0

9) Data stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (10h) or "Data Stop" (11h) commands, BUSY signal will become "0" until display update is finished.

10) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY signal will become "0" until display update is finished.

11) Image Process Command (IPC) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Image Process Setting	0	0	0	0	1	0	0	0	1	1
	0	1	-	-	-	IP_EN	-	IP_SEL[2:0]		

After this command is issued, image process engine will find thin lines/pixels from frame SRAM and update the frame SRAM for

applying new gray level waveform.

IP_EN: Image process enable.

0: No action.

1: Image process enable (auto return to '0' after image process is finished.

IP_SEL[2:0]: Image process selection.

000 : Deal with 1-pixel width

001 : Deal with 2-pixel width

010 : Deal with 3-pixel width

011 : Deal with 1-pixel and 2-pixel width

100 : Deal with 1-pixel, 2-pixel and 3-pixel width

Others : Deal with 1-pixel width

After "Image Process Command" (13h), BUSY_N signal will become "0" until image process is finished

12) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for VCOM (221-byte command, bytes 2~12 repeated 20 times)	0	0	0	0	1	0	0	0	0	0

This command builds up VCOM Look-Up Table (LUT).

13) Black LUT (LUTB) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Black (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	0	0	1

This command builds LUTB.

14) White LUT(LUTW) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for White (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	0	1	0

This command builds LUTW.

15) Gray1 LUT (LUTG1) (R23H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Gray1 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	0	1	1

This command builds LUTG1.

16) Gray2 LUT (LUTG2) (R24H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Gray2 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	0	0

This command builds LUTG2.

17) Red0 LUT (LUTR0) (R25H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Red0 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	0	1

This command builds LUTR0.

18) Red1 LUT (LUTR1) (R26H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Red1 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	0	1

This command builds LUTR1.

19) Red2 LUT (LUTR2) (R27H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Red2 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	1	1

This command builds LUTR2.

20) Red3 LUT (LUTR3) (R28H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for Red3 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	1	0	0	0

This command builds LUTR3.

21) XON LUT (LUTXON) (R29H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-Up Table for XON (201-byte command, bytes 2~11 repeated 20 times)	0	0	0	0	1	0	1	0	0	1

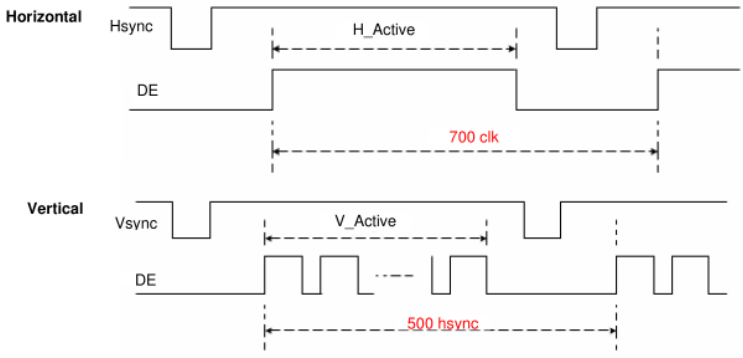
This command builds LUTXON.

22) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate
1	1	29 Hz	3	1	86 Hz	5	1	143Hz	7	1	200 Hz
	2	14 Hz		2	43 Hz		2	71 Hz		2	100 Hz
	3	10 Hz		3	29 Hz		3	48 Hz		3	67 Hz
	4	5 Hz		4	21 Hz		4	36 Hz		4	50 Hz (Default)
	5	7 Hz		5	17 Hz		5	29 Hz		5	40 Hz
	6	6 Hz		6	14 Hz		6	24 Hz		6	33Hz
	7	5 Hz		7	12Hz		7	20 Hz		7	29 Hz
2	1	57 Hz	4	1	114 Hz	6	1	171 Hz			
	2	29 Hz		2	57 Hz		2	86 Hz			
	3	19 Hz		3	38 Hz		3	57 Hz			
	4	14 Hz		4	29Hz		4	43 Hz			
	5	11 Hz		5	23 Hz		5	34 Hz			
	6	10 Hz		6	19 Hz		6	29 Hz			
	7	8 Hz		7	16 Hz		7	24 Hz			



23) Temperature Sensor Calibration(TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10	D9/TS7	D8/TS6	D7/TS5	D6/TS4	D5/TS3	D4/TS2	D3/TS1
	1	1	D2/TSO	D1	D0	-	-	-	-	-

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

Bit 7~0	Temperature(℃)
0000 0000b	0
0000 0001b	0.5
0000 0010b	1
..	..
0101 1010b	45
..	..
0110 0100b	50
..	..
1100 1110b	-25
..	..
1111 1110b	-1
1111 1111b	-0.5

BUSY become low after TSC command. When BUSY become high, Parameter can be read.

24) Temperature Sensor Internal/External(TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Selection	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-						

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Select internal temperature sensor (default) 1: Select external temperature sensor.

25) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Selection	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

This command could write data to the external temperature sensor.

WATTR: D[7:6]: I^2C Write Byte Number

00: 1 byte (head byte only)

01: 2 bytes (head byte + pointer)

10: 3 bytes (head byte + pointer + 1st parameter)

11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor.

26) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensor Selection	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command could read data from the external temperature sensor.

RMSB[7:0]: MSByte of read-data from external temperature sensor.

RLSB[7:0]: LSByte of read-data from external temperature sensor.

27) VCOM and Data Interval Setting(CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between	0	0	0	1	0	1	0	0	0	0
Vcom and Data	0	1	VBD[2:0]			DDX	CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[2:0]: Border output selection.

DDX: Data polality.

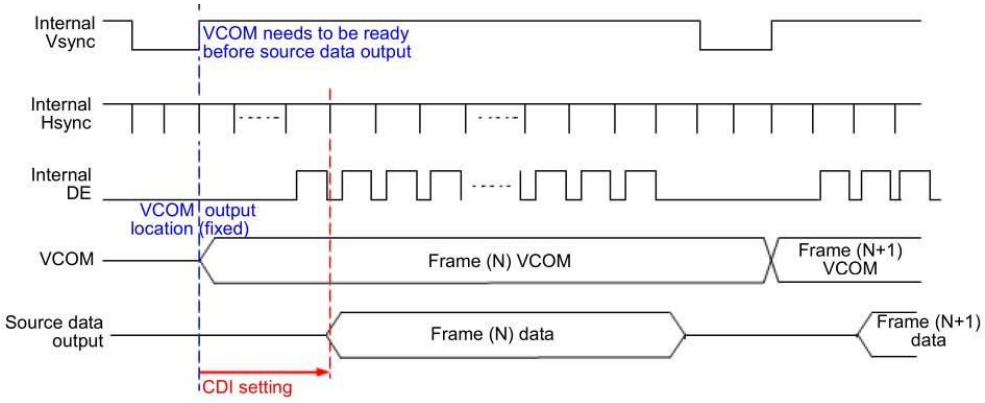
The mapping table of VBD[2:0] and DDX is listed as below.

	Border Output	
VBD[2:0]	DDX=1(default)	DDX=0
	LUT	LUT
000	Black	White
001	Gray1	Gray2
010	Gray2	Gray1
011	White	Black
100	Red0	Floating
101	Red1	Red2
110	Red2	Red1
111	Floating	Red0

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval	CDI[3:0]	Vcom and Data Interval
0000b	17 hsync	1000	9
0001	16	1001	8
0010	15	1010	7

…	…	…	…
0110	11	1110	3
0111	10(Default)	1111	2



28) Low Power Detection(LPD) (R51h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input (VDD<2.5V) 1: Normal status (default)

29) TCON Setting(TCON) (R60h)

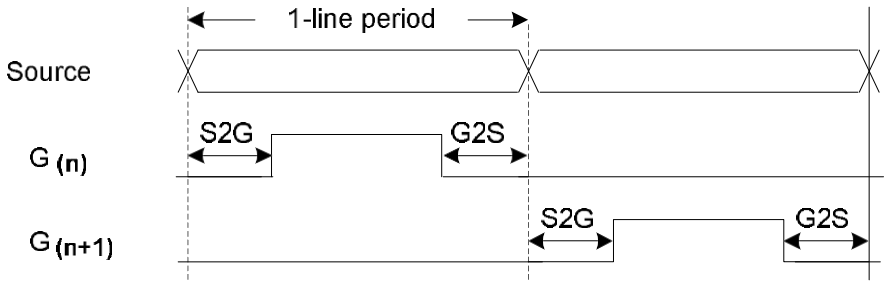
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000b	4		…	…
0001	8		1011	48
0010	12(Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



30) Resolution Setting(TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:0]							
	0	1	-	-	-	-	-	-	HRES[9:8]	
	0	1	VRES[7:0]							
	0	1	-	-	-	-	-	-	-	VRES[8]

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[9:0]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Resolution setting (R61H) has higher priority than RES[1:0] (R00H). Resolution should be even number.

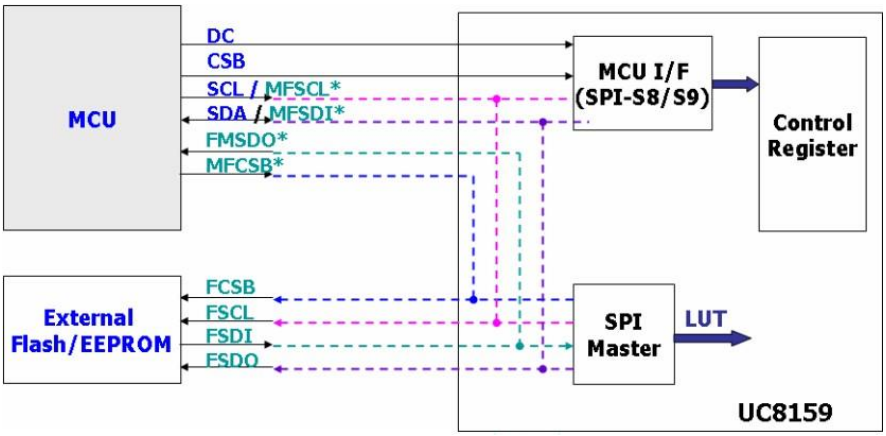
31) SPI Flash Control(DAM) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	1	0	0	0	0	1
	0	1	-	-	-	-	-	-	-	DAM

This command defines MCU host direct access external memory mode.

DAM: 0: Disable (default)

1: Enable. By pass MFSCL*, MFSDI*, MFSDO*, AND MFCSB* to external flash.



32) Revision(REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LUT/Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	LUTVER[7:0]							
	1	1	LUTVER[15:8]							
	1	1	0	0	0	0	CHREV[3:0]			

The LUTVER[15:0] is read from OTP address = 25001 and 25000.

LUTVER[15:0]: LUT versionL.

CHREV [3:0]: Chip Revision.

33) Get status(FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	-	I^2C_ERR	I^2C_BUSY	Data_flag	PON	POF	BUSY

This command reads the IC status.

I^2C_ERR: I^2C master error status

I^2C_BUSY: I^2C master busy status (low active)

Data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY: Driver busy status (low active)

34) Auto measure vcom(AMV) (R80h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		AMVX	AMVS	AMV	AMVE

This command implements related VCOM sensing setting.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s 01b: 5s (default)

10b: 8s 11b: 10s

AMVX: Auto Measure VCOM without XON function

0: Measure VCOM without XON function. (Gate scanning) (default)

1: Measure VCOM without XON function. (All Gate ON)

AMVS: Source output of AMV

0: Set Source output to 0V during Auto Measure VCOM period. (default)

1: Set Source output to 3V (or VDPS_L) during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Enable (/Disable)

0: Disabled 1: Enabled

35) VCOM Value(VV) (R81h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	VV [6:0]						

This command gets the Vcom value.

VV[6:0]: Vcom Value Output

VV[6:0]	Vcom value
000 0000b	0 V
000 0001b	-0.05 V
000 0010b	-0.10 V
000 0011b	-0.15 V
:	:
101 0000b	-4.00 V
(Others)	-4.00V

36) VCOM-DC Setting(VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	VDCS[6:0]						

This command sets VCOM_DC value.

VDCS[6:0]: VCOM_DC Setting

VDCS[6:0]	VCOM_DC Value
000 0000b	(Reserved)
000 0001b	(Reserved)
000 0010b	-0.10v
000 0011b	-0.15v
000 0100b	-0.20v
..	..
101 0000b	-4.0v
(others)	-4.0v

7. Electrical Characteristics

7-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.3 to +6.0	V
Logic Input Voltage	V_{IN}	-0.3 to VCI +0.3	V
Operating Temp. range	T_{OPR}	0 to +40	℃
Storage Temp. range	T_{STG}	-25 to +60	℃

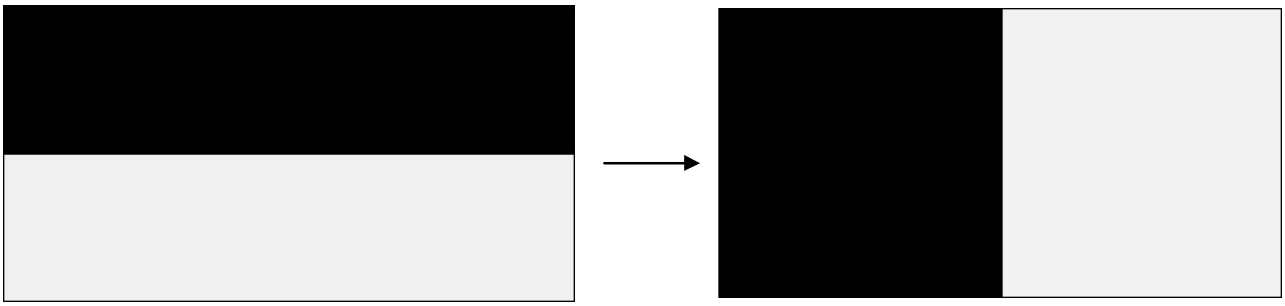
7-2) Panel DC Characteristics

The following specifications apply for: VSS = 0V, VCI = 3.3V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.3	3.3	3.6	V
High level input voltage	VIH	-	0.7VCI	-	VCI	V
Low level input voltage	VIL	-	GND	-	0.3VCI	V
High level output voltage	VOH	IOH= 400uA	VCI-0.4	-	-	V
Low level output voltage	VOL	IOH= -400uA	GND	-	GND + 0.4	V
Image update current	I_{UPDATE}	-	TBD	TBD	TBD	mA
Standby panel current	Istandby	-	TBD	TBD	TBD	uA
Power panel (update)	P_{UPDATE}	-	TBD	TBD	TBD	mW
Standby power panel	P_{STBY}	-	TBD	TBD	TBD	mW
Operating temperature	-	-	0	-	40	℃
Storage temperature	-	-	-25	-	60	℃
Image update Time at 25 ℃	-	-	TBD	TBD	TBD	Sec
POF	VCI	DC/DC off No clock No input load Ram data not retain	TBD	TBD	TBD	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Note 7-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Qiyun Display
- Vcom is recommended to be set in the range of assigned value ± 0.1V.

Note 7-1: The Typical power consumption



7-3) Panel AC Characteristics

7-3-1) MCU Interface

7-3-1-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDin	SCLK	CS#	D/C#	RES#
SPI3	SDin	SCLK	CS#	L	RES#

Table 7-4-1-1: MCU interface assignment under different bus interface mode

Note 7-2: L is connected to VSS

Note 7-3: H is connected to VCI

7-3-1-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

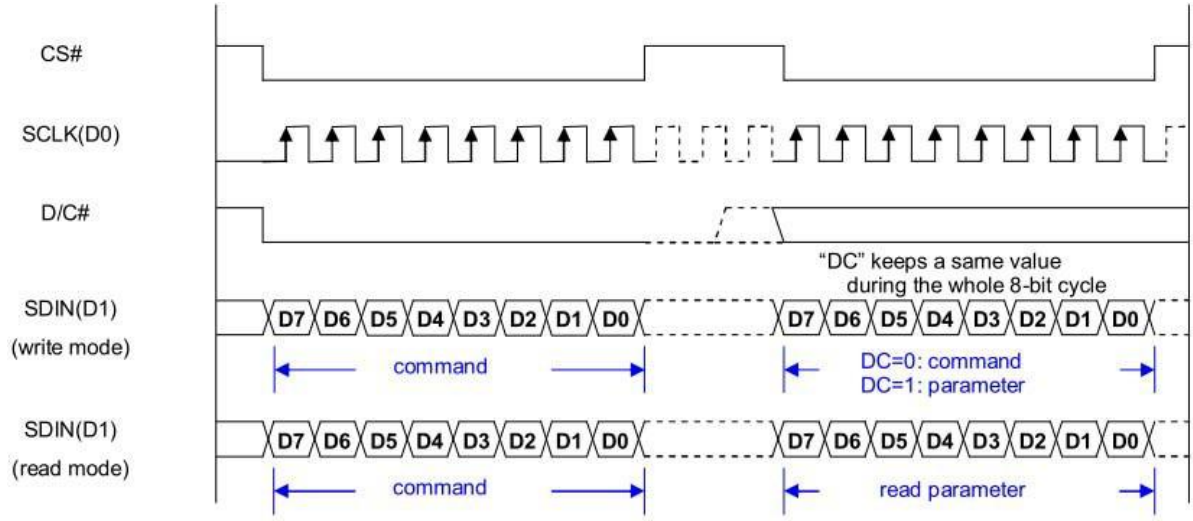
Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 7-4-1-2: Control pins of 4-wire Serial Peripheral interface

Note 7-4: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Figure 7-4-1-2: Write procedure in 4-wire Serial Peripheral Interface mode



7-3-1-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

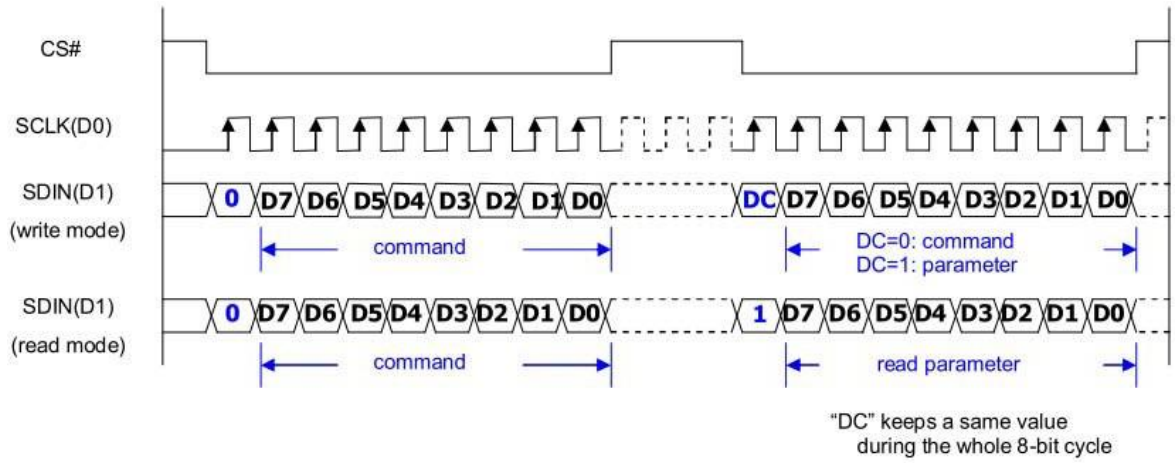
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

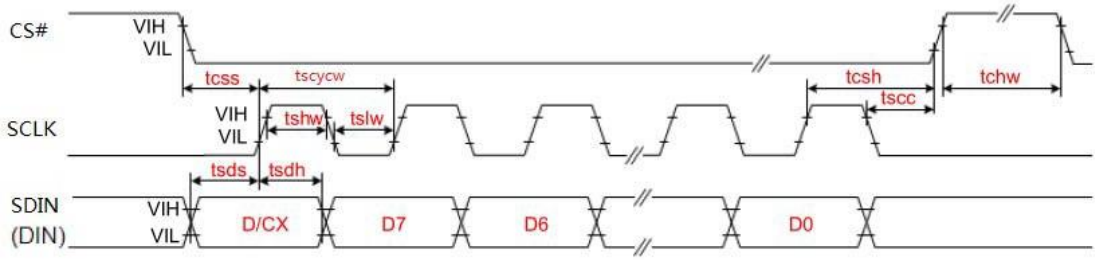
Table 7-4-1-3: Control pins of 3-wire Serial Peripheral Interface

Note 7-5: ↑stands for rising edge of signal

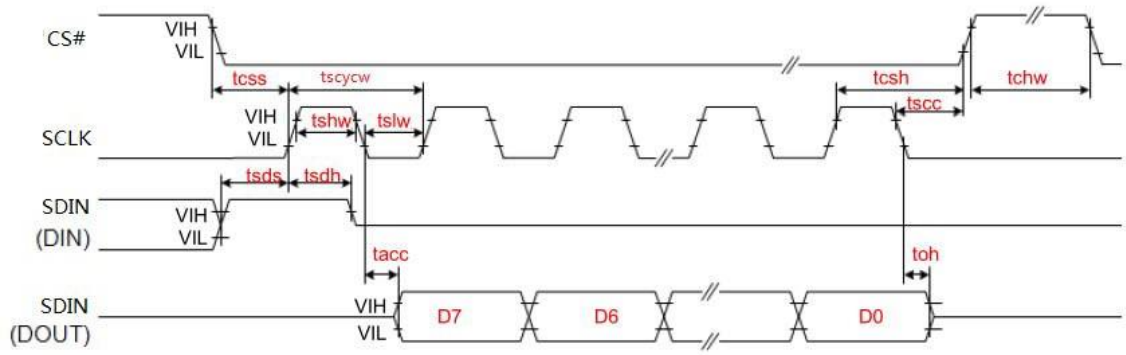
Figure 7-4-1-3: Write procedure in 3-wire Serial Peripheral Interface mode



7-3-2) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCLK	Serial clock cycle (write)	100	-	-	ns
tshw		SCL “H” pulse width (write)	35	-	-	ns
tslw		SCL“L” pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	150	-	-	ns
tshr		SCL “H” pulse width (Read)	60	-	-	ns
tslr		SCL “L” pulse width (Read)	60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	10	-	-	ns
toh		Output disable time	15	-	-	ns

7-4) Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	26.4	40	mW	-
Power consumption in standby mode	-	25℃	-	0.0165	mW	-

7-5) Reference Circuit

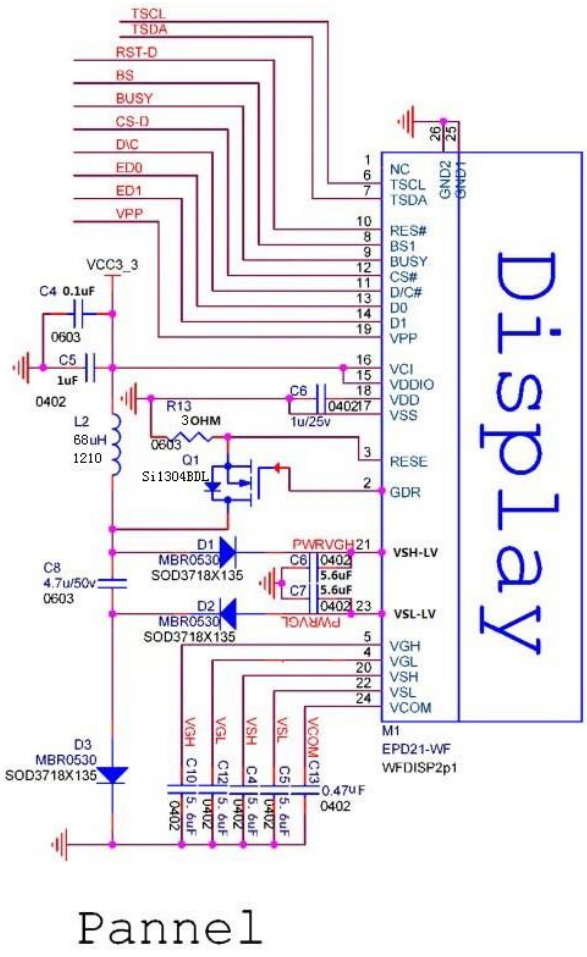


Figure. 7-5(1)

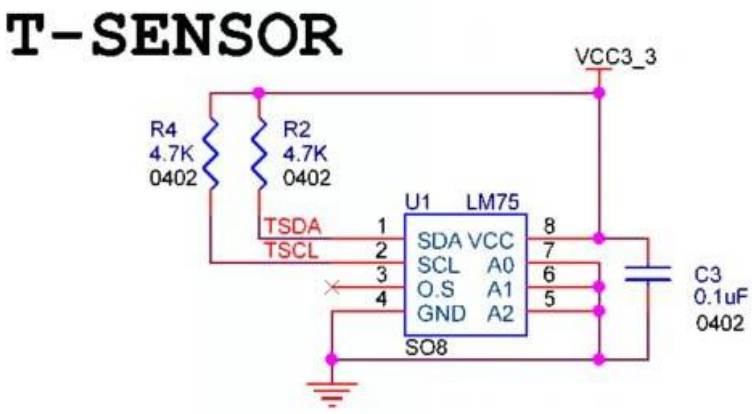
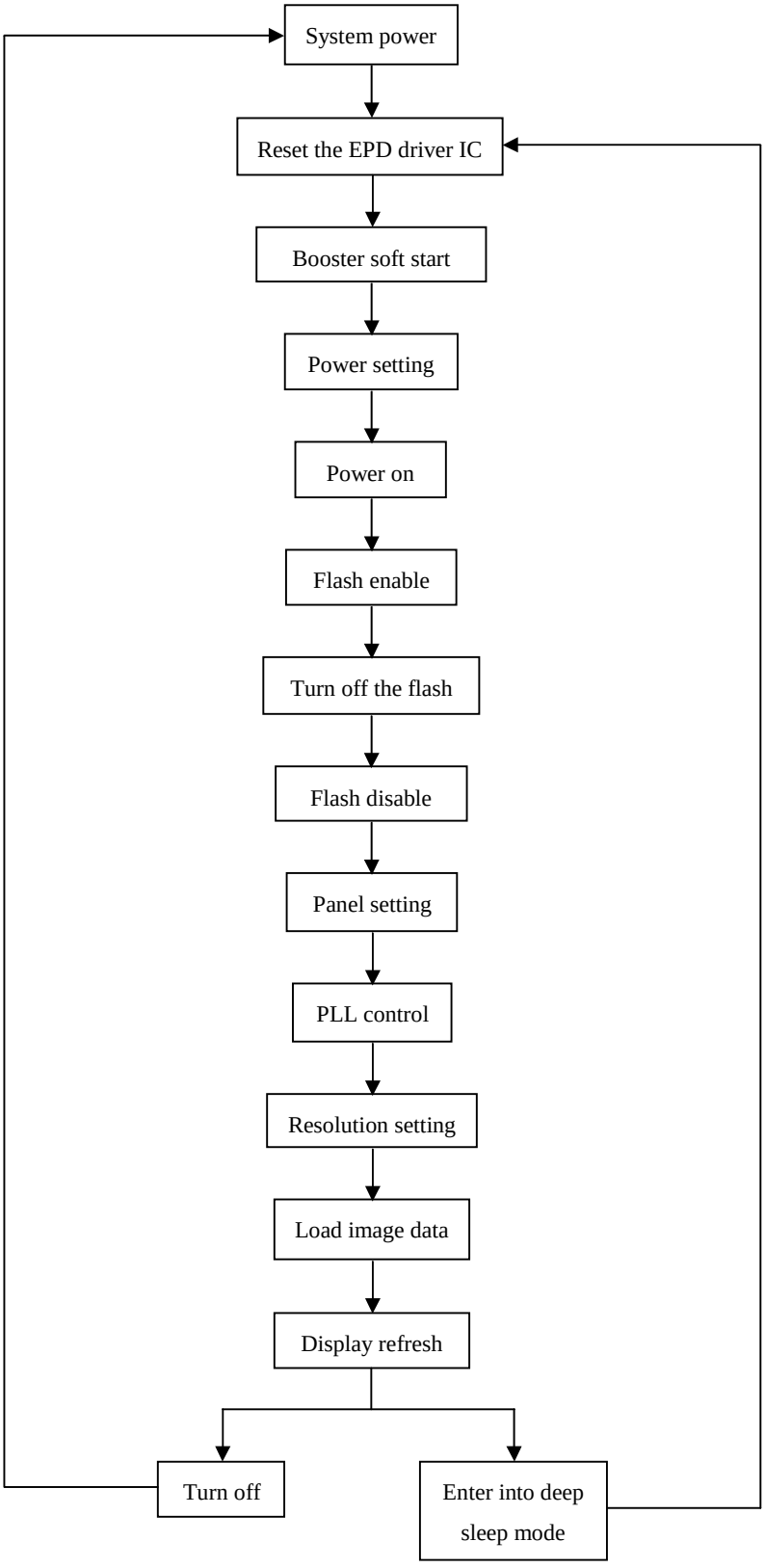


Figure. 7-5(2)

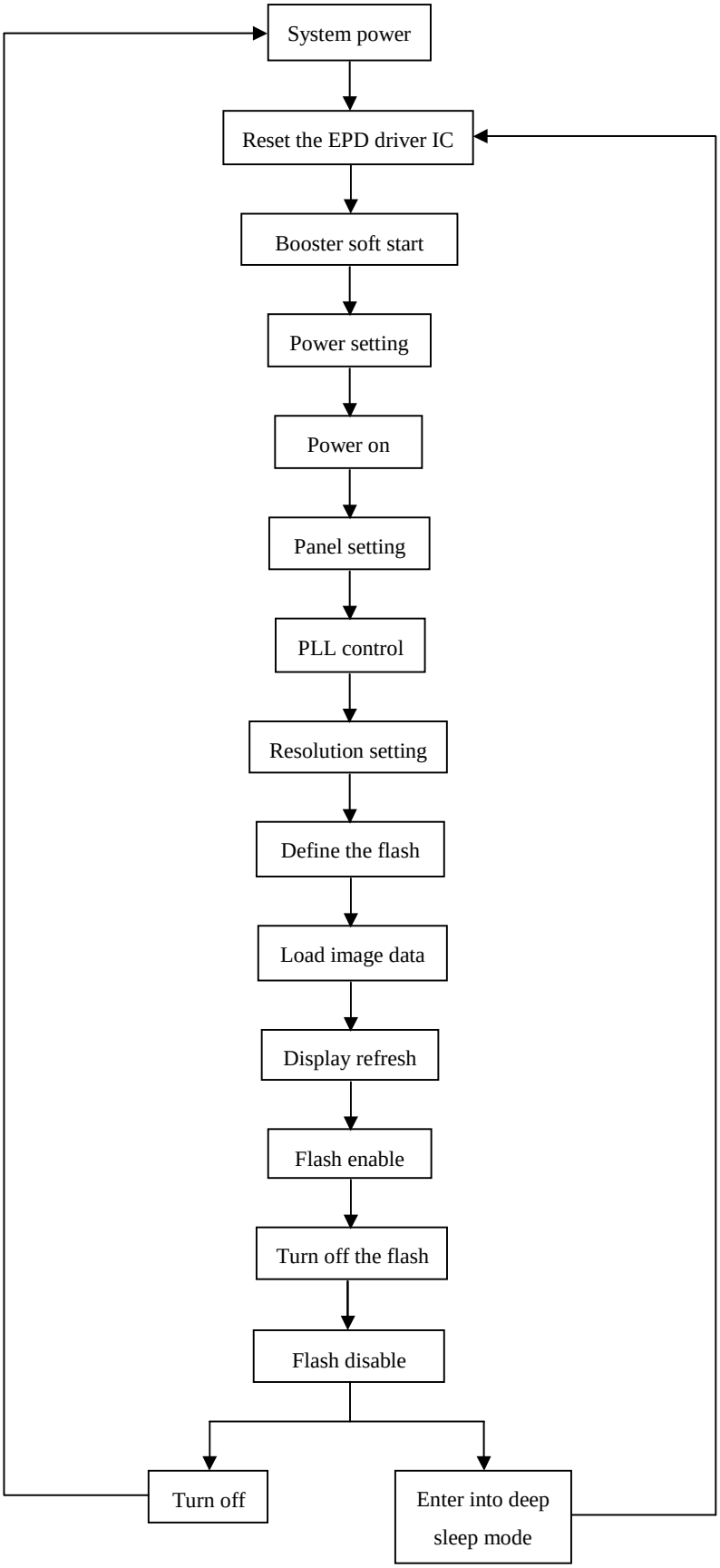
8. Typical Operating Sequence

8-1) Normal Operation Flow

1. LUT from register

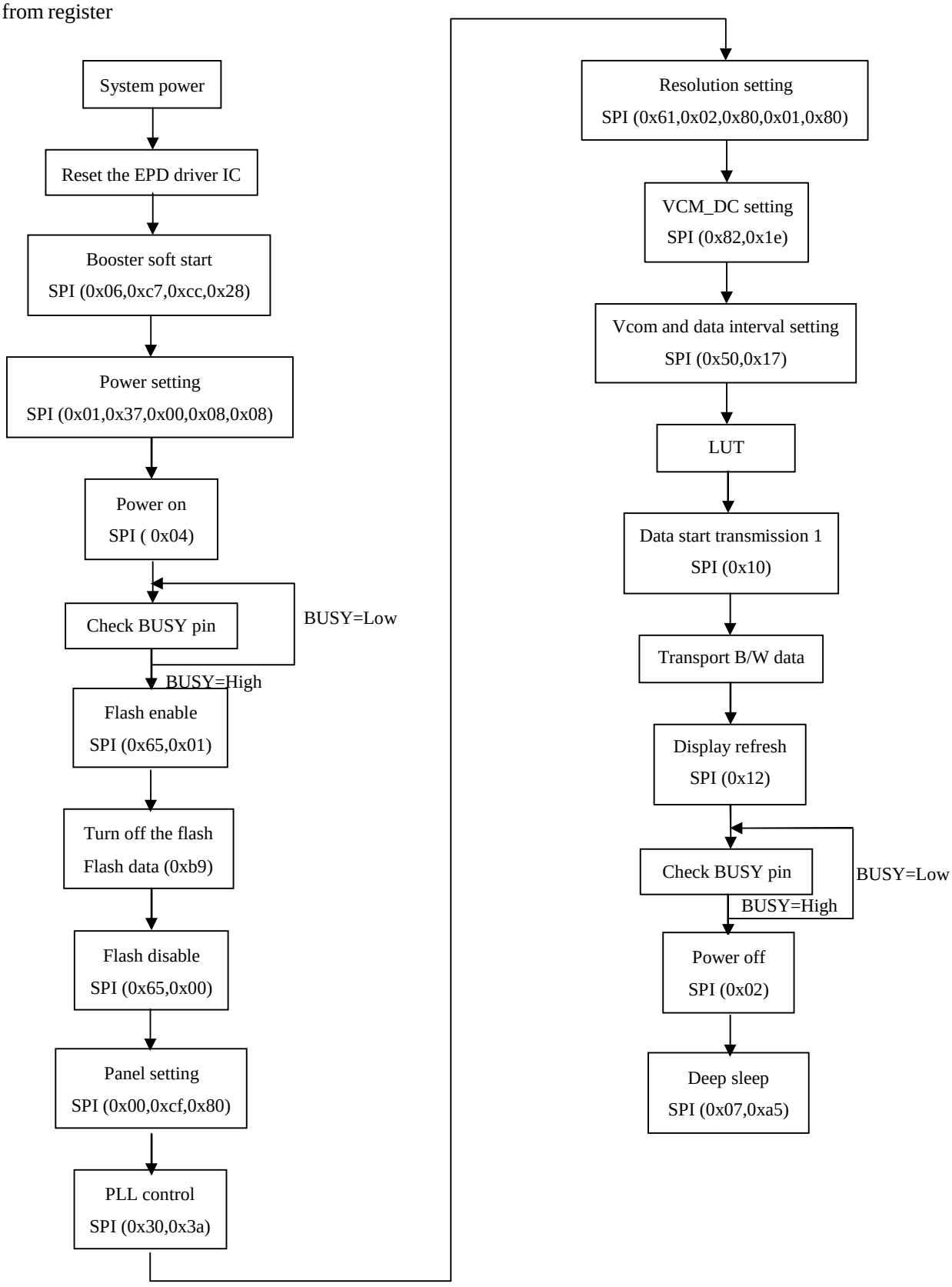


2. LUT from flash

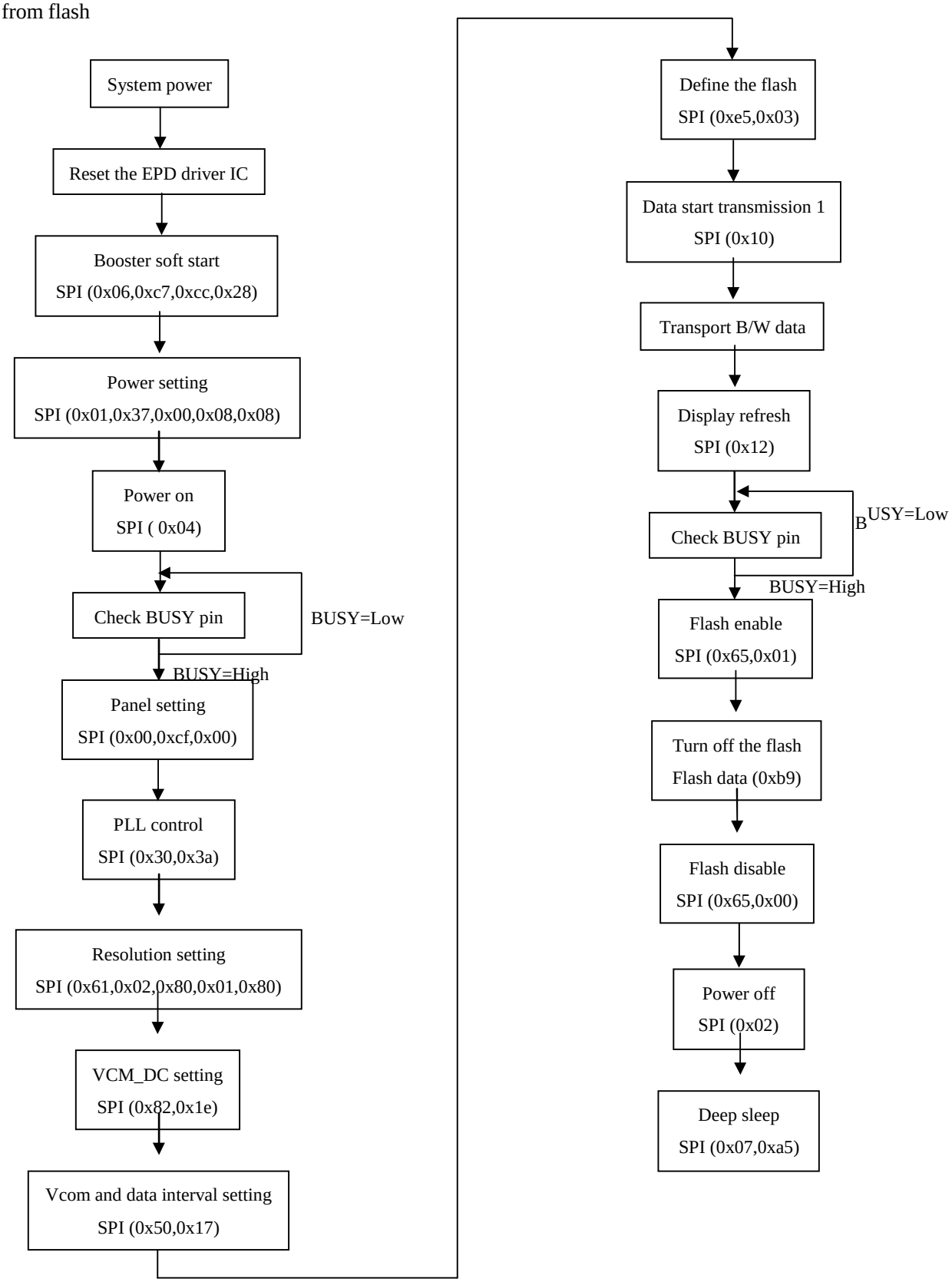


8-2) Reference Program Code

1. LUT from register



2. LUT from flash



9. Optical characteristics

9-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 9-1
Gn	2Grey Level	-	-	DS+(WS-DS)xn(m-1)	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
Panel's life		0℃~40℃		1000000 times or 5 years			Note 9-2
Panel	Image Update	Storage and transportation		Update the white screen			
	Update Time	Operation		Suggest update once every 24 hours or at least 10 days to update again.			

WS: White state, DS: Dark state

Gray state from Dark to White : DS、WS

m: 2

Note 9-1: Luminance meter: Eye – One Pro Spectrophotometer

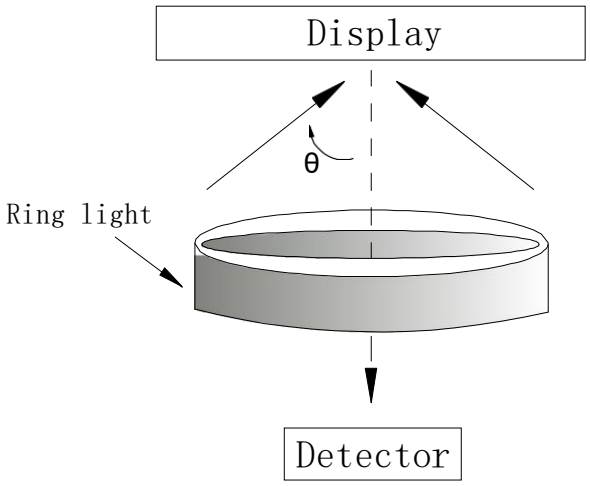
Note 9-2: Panel life will not guaranteed when work in temperature below 0 degree or above 40 degree. Each update interval time should be minimum at 180 seconds.

9-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

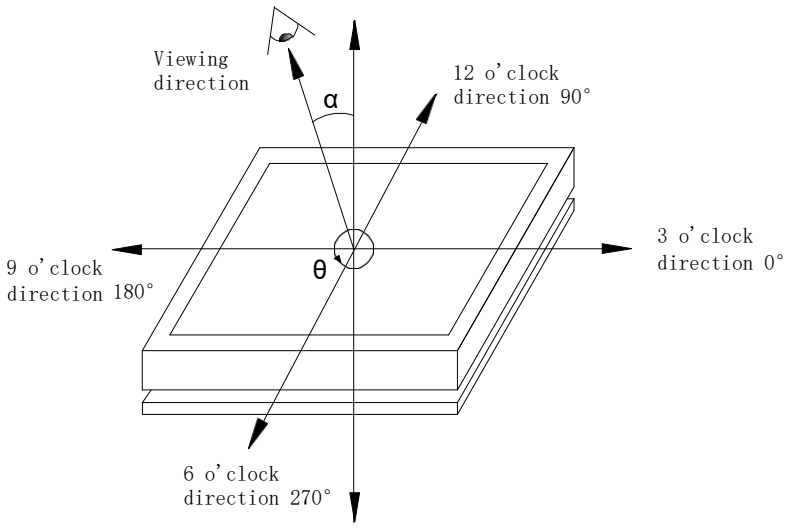


9-3) Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



9-4) Bi-stability

The Bi-stability standard as follows:

Bi-stability	Result		
24 hours Luminance drift		AVG	MAX
	White state △L*	-	3
	Black state △L*	-	3

10. Handling, Safety and Environmental Requirement

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Product Environmental certification
RoHS

11. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 40℃, RH=35%, for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperature Operation	T = 0℃ for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperature Storage	T = +60℃, RH= 35%, for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Ab	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperature, High-Humidity Operation	T=+40℃, RH=80% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperature, High-Humidity Storage	T=+50℃, RH=80% For 240hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
7	Temperature Cycle	[-25℃ 30mins]→ [+60℃, RH=35% 30mins], 50cycles Test in white	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25℃, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 60℃. After 30min, temperature will be adjusted to 60℃, RH=35% and storage period	When experiment finished, the EPD must meet electrical and optical performance

		pattern	is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25℃. One temperature cycle (2hrs) is complete. 2. Temperature cycle repeats 70 times. 3. When 70 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-14NB.	standards.
8	UV exposure Resistance	765 W/m^2 for 168 hrs,40℃	Standard # IEC 60068-2-5 Sa	
9	Electrostatic discharge	Machine model: +/-250V, 0Ω,200pF	Standard # IEC 61000-4-2	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note: (1) The protective film must be removed before temperature test.

(2) There's temperature vs display quality limitation in our display module, we guarantee 1 pixel display quality from 5℃ ~ 30℃, and 2 pixel display quality for 0℃~ 5℃ & 30℃ ~ 40℃.

(3) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 15 mins.

12. Point and line standard

Shipment Inseption Standard

Part-A：Active area　　Part-B：Border area

Equipment：Electrical test fixture, Point gauge

Outline dimension：

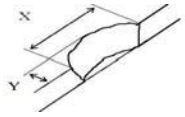
170.2(H)×111.2(V)×1.18(D)　　Unit：mm

Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	23±2℃	55± 5%RH	1200～ 1500Lux	300 mm	35 Sec	

Name	Causes	Spot size	Part-A	Part-B
Spot	B/W spot in glass or protection sheet, foreign mat. Pin hole	D ≤ 0.25mm	Ignore	Ignore
		0.25mm < D ≤ 0.4mm	4	
		0.4mm < D ≤ 0.5mm	1	
		0.5mm < D	0	

Scratch or line defect	Scratch on glass or Scratch on FPL or Particle is Protection sheet.	Length	Width	Part-A	Ignore
		L ≤2.0mm	W≤0.2 mm	Ignore	
		2.0 mm < L≤ 8.0mm	0.2 mm<W≤ 0.5mm	2	
		8.0 mm < L	0.5mm < W	0	

Air bubble	Air bubble	D1, D2 ≤ 0.25 mm	Ignore	Ignore
		0.25 mm < D1,D2 ≤ 0.4mm	4	
		0.4mm < D1, D2	0	

Side Fragment	
	X≤6mm，Y≤1mm & display is ok, Ignore

Remarks: Spot define: That only can be seen under WS or DS defects.

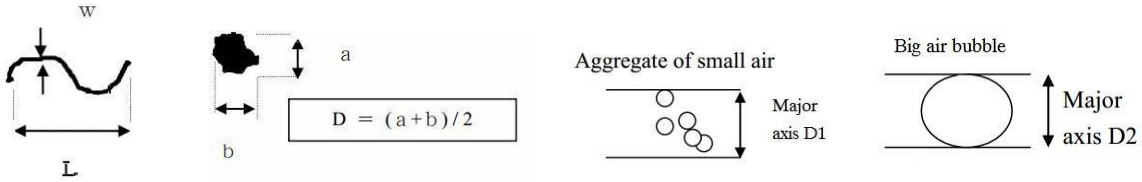
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Here is definition of the “Spot” and “Scratch or line defect”.

Spot: W > 1/4L　　Scratch or line defect: W ≤1/4L

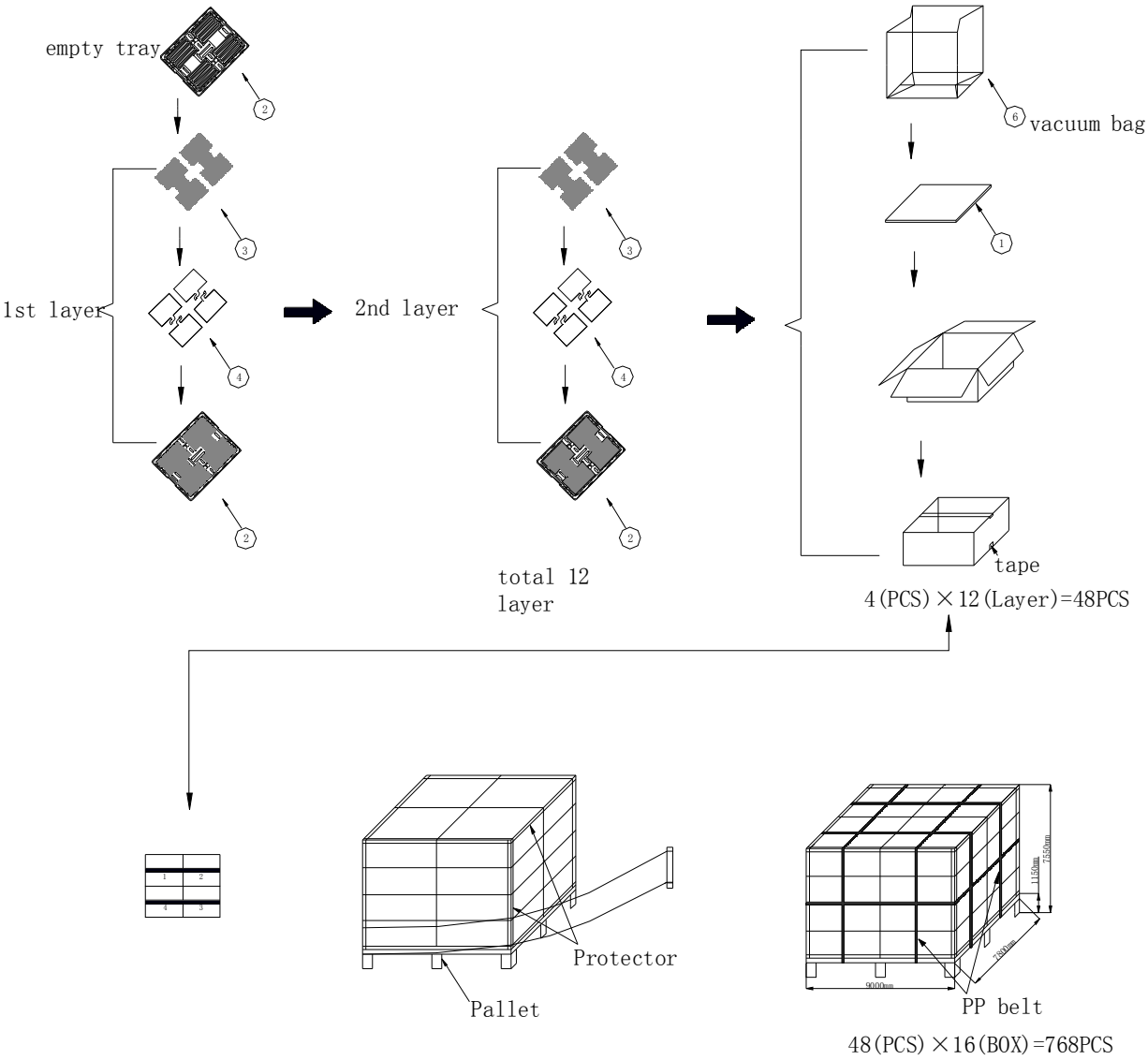
Definition for L/W and D (major axis)

FPC bonding area pad doesn’t allowed visual inspection.



Note: AQL = 0.4

13. Packing


empty tray
2
3
4
1st layer
2nd layer
total 12
layer
6
vacuum bag
1
tape
4(PCS)×12(Layer)=48PCS
Protector
Pallet
PP belt
48(PCS)×16(BOX)=768PCS