**DARSHAN BALLARI**

**Summary:**

Enthusiastic VLSI engineer **with 2+ years** Quick in adapting to new challenges.

**Skills**:

* Hardware Verification Languages : SystemVerilog Assertions, **UVM, System Verilog, Verilog**
* Good understanding in Formal Verification.
* Good understanding and coding in SV Functional Coverage, Constraints and Assertions.
* Scripting skills : Good understanding of Python.
* OS Platforms : Windows, Linux
* Knowledge on OOPS Concept
* Tools: Cadence, Altera Modelsim, Xilinx ISE, Aldec Riviera Pro, Questasim, Questa Formal
* Domain : Digital logic design , FPGA/ASIC design flow
* Good knowledge on Clear case
* Worked on the App which helps in finding if some rule is not used
* Created some of the Examples for PASS and FAIL Test Cases for all the rules

**Projects:**

**Title: FPGA Verification of OC192 (FLASHWAVE 4100 ES) Line Unit**

FLASHWAVE 4100 ES Micro Packet Optical Networking Platform (Packet ONP) is ideal for Ethernet and TDM access service delivery and aggregation over networks up to 10 Gbps.

OC192 (EL91/EL92) Line unit being verified in this project.

* Replace the Previous ASIC Chip with new FPGA.
* Integrate the 9.93Gbps SERDES function internal to New FPGA.
* Merging 3 different FPGAs into single FPGA based on newer technology (28 or 20nm)

This New designed FPGA handles an OC-192 SONET traffic on the line side through the 10G 16-bit interface. This FPGA processes STS-1, STS-3c, STS-12c and STS-48c traffic and VT1.5 traffic.

**Team Size: 5**

**Tools: Cadence (12.2, 15.2) simulator (SimVision),**

**Roles:**

* Verification of New FPGA (**FLASHWAVE 4100 ES**).
* Understand the **SONET** protocol and flow of architecture of NEW FPGA verification is being verified.
* Worked on developing the verification plan for the new design of OC192.
* Worked on preparation of register verification plan for block level blocks, which are the sub-module of New FPGA.
* Development of new test cases for different operating modes-OC192, OC48, OC12 and OC3.
* Worked on Register Verification of every blocks of New FPGA**.**
* Created Definition for Every registers in a particular block of FPGA.
* Created Task Definitions for RW, RO, RCLR, W1S, INTR, PMC, SMT, and Default Register Check.
* Developed Test cases for RW, RO, RCLR, W1S, INTR, PMC, SMT, and Default Register Check.
* Created function for Displaying the Register Name and for accessing the write data and default data.
* Good knowledge on Clear case like Check-in files, Check-out files and Deliver the files.
* Worked on the provisioning sequence on which the basic data traffic depends and worked on debugging the output of different blocks, which are sub modules of New FPGA.

**Title: Machine Learning Coverage Closure**

**Team Size: 4**

**Tools: VCS**

* I have coded the SV testcases for the ML algorithm considering the different types of coverages and constraints.
* Testcases being the trained data, all the testcases are constrained to achieve the 100% functional coverage.
* **XULA-1200 AES block level Verification**

**Description:** XULA-1200 is a Soc with dual processors and subsystems such as DMA, AES (Crypto engine), Camera subsystem and smaller peripherals such as I2C, GPIO, and UART etc. Individual IPs are verified using UVM. AES block has cipher and decryptor engines. It supports 128-bit and 256-bit keys.

**Roles:**

* Read XULA-1200 AES specification
* Create test plan for AES block level tests for XULA-1200
* Reuse existing UVM environment
* Run sequences, collect coverage
* Develop new sequences to close coverage gaps
* **RTL Design for UVM RAL model for a client PoC system:**
  + Involved various **RAL access modes** (18+ modes)
  + Support for Quirky register in RTL with volatile counters
  + Support DV team during integration of DUT with **UVM-RAL**
* **AMBA APB 3 Interface**
  + Learn protocol
  + Understand micro architecture provided by the leads
  + RTL design for APB3 slave
  + Integrate with in house APB3 VIP and verify
* **AMBA AHB-3 Lite Interface protocol** 
  + Learning the protocol
  + **Using existing CIP (Checker IP) with System Verilog Assertions**
* **RTL design of several digital building blocks including:**
  + Synchronous FIFO with Watermark
  + VLBus – Slave Memory Controller
  + Four PORT Packet Parser

**Formal Projects:**

**Title: Zipline Design Verification**

Zipline is a complex compression IP from Microsoft.

Roles :

* Understanding Zipline specification
* Bring up the design in Questa Formal, resolve setup issues
* Perform connectivity verification using Formal & UVM (via Go2UVM app)
* Perform register check using Formal

**Team Size: 3**

**Tools Used : Questa Formal**

**Title: Register Design Verification Using Questa Formal**

DMA and ETH\_MAC

**Roles :**

* Understanding specification
* Doing Register Check for both the blocks

**Team Size: 2**

**Tools Used : Questa Formal**

**Title: Formal Based Verification of AMBA APB**

* **Tool Used:** Questa Formal
* **Responsibilities:** 
  + Understood and Presented design specification and Developed verification plan and Test plan.
  + Developed assertion based formal testbench for APB.
  + Development of Assertions for Verifying the Functionality of APB.
  + Creating New Assert and Cover Properties for Verifying the Functionality.