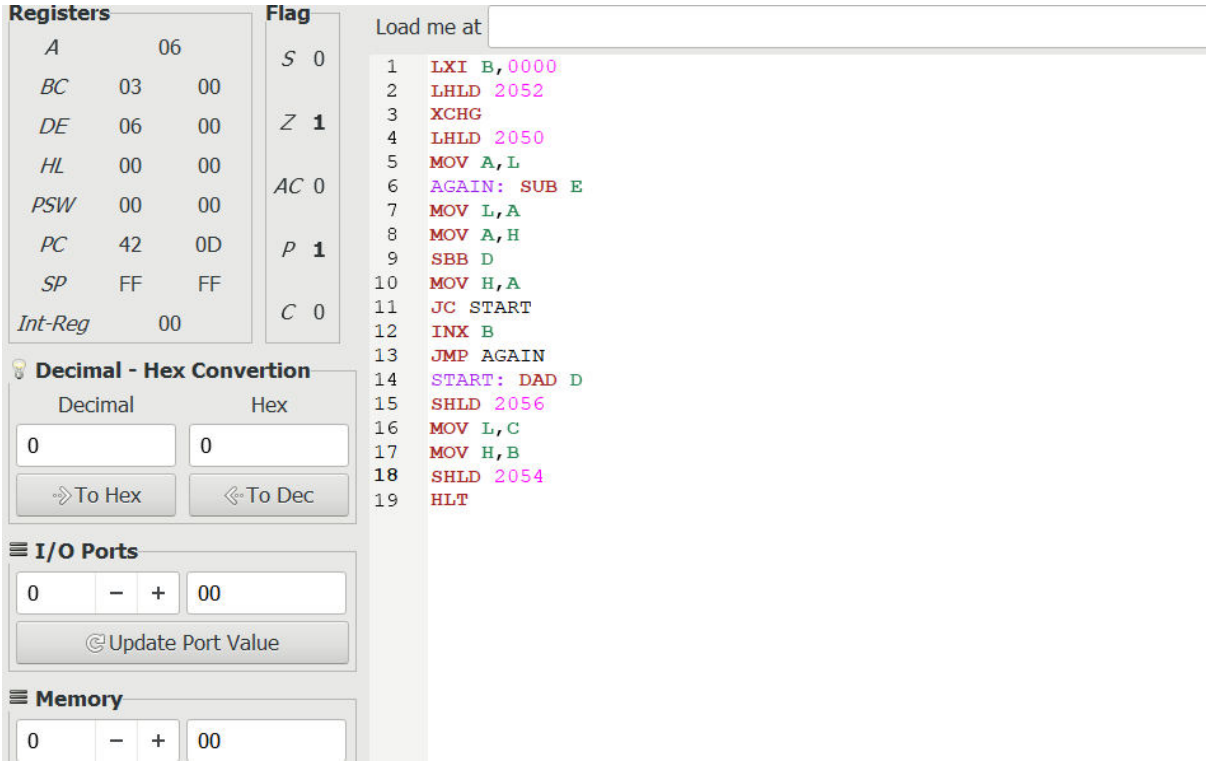
27-16-bit division

Program

```
LXI B,0000
LHLD 2052
XCHG
LHLD 2050
MOV A,L
AGAIN: SUB E
MOV L,A
MOV A,H
SBB D
MOV H,A
JC START
INX B
JMP AGAIN
START: DAD D
SHLD 2056
MOV L,C
MOV H,B
SHLD 2054
HLT
```

Output


Registers
A 06
BC 03 00
DE 06 00
HL 00 00
PSW 00 00
PC 42 0D
SP FF FF
Int-Reg 00
Flag
S 0
Z 1
AC 0
P 1
C 0
Decimal - Hex Convertion
Decimal
Hex
0
0
To Hex
To Dec
I/O Ports
0
00
Update Port Value
Memory
0
00
Load me at
1 LXI B,0000
2 LHLD 2052
3 XCHG
4 LHLD 2050
5 MOV A,L
6 AGAIN: SUB E
7 MOV L,A
8 MOV A,H
9 SBB D
10 MOV H,A
11 JC START
12 INX B
13 JMP AGAIN
14 START: DAD D
15 SHLD 2056
16 MOV L,C
17 MOV H,B
18 SHLD 2054
19 HLT