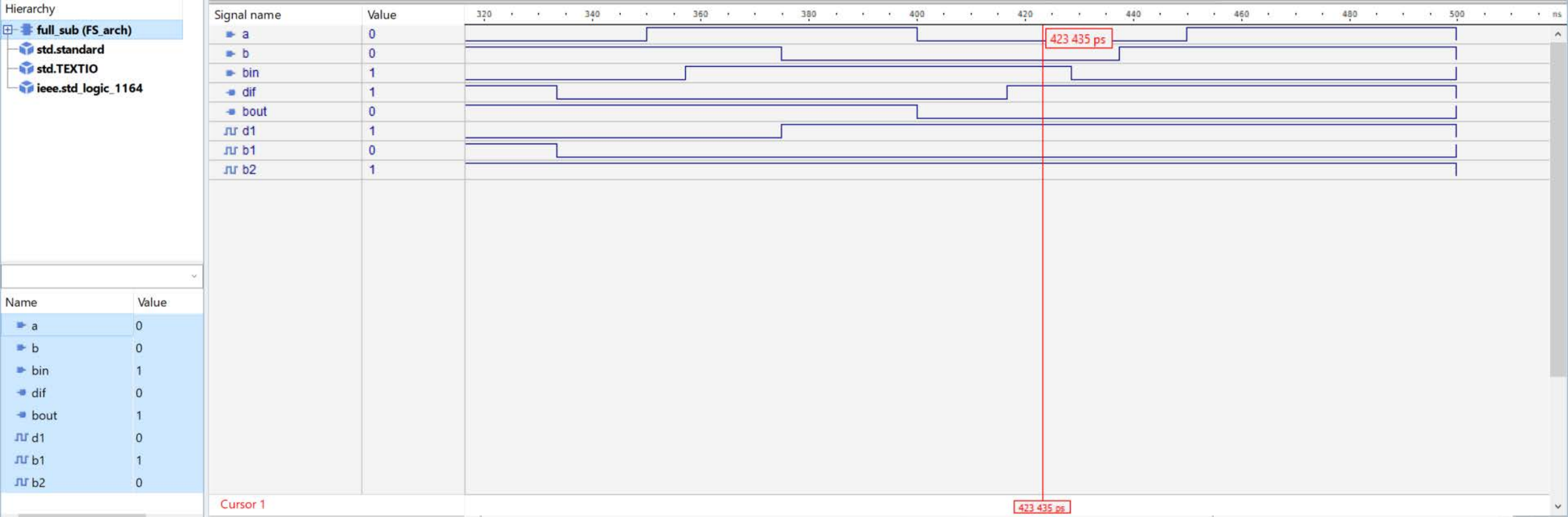
Full Subtractor Using Half Subtractor

```
1   library IEEE;
2   Use IEEE. STD_LOGIC_1164.all;
3   entity full_sub IS
4   port (a,b,bin :in STD_LOGIC;
5         dif,bout : out STD_LOGIC);
6   end full_sub;
7   architecture FS_arch of full_sub is
8   component half_sub is
9   port (p,q :in STD_LOGIC;
10        dif,bo: out STD_LOGIC);
11  end component;
12  component or_gate is
13  port (p1,q1 :in STD_LOGIC;
14        r1: out STD_LOGIC);
15  end component;
16  signal d1,b1,b2 : STD_LOGIC;
17  begin
18   w1: half_sub port map (a,b,d1,b1);
19   w2: half_sub port map (d1,bin,dif,b2);
20   w3: or_gate port map (b1,b2,bout);
21  end FS_arch;
```


Hierarchy
full_sub (FS_arch)
std.standard
std.TEXTIO
ieee.std_logic_1164
Name
Value
a 0
b 0
bin 1
dif 0
bout 1
d1 0
b1 1
b2 0
Signal name
Value
320
340
360
380
400
420
440
460
480
500
ns
423 435 ps
Cursor 1
423 435 ps