Gray to Binary Code Converter

```vhdl
1
2   library ieee;
3   use ieee.std_logic_1164.all;
4
5   entity g2b_code is
6   port (g : in std_logic_vector(3 downto 0);
7         b : out std_logic_vector(3 downto 0));
8   end g2b_code;
9
10  architecture g2b_arch of g2b_code is
11    begin
12      b(3) <= g(3);
13      b(2) <= g(3) xor g(2);
14      b(1) <= g(3) xor g(2) xor g(1);
15      b(0) <= g(3) xor g(2) xor g(1) xor g(0);
16  end g2b_arch;
```

Signal name	Value
g	7
g[3]	0
g[2]	1
g[1]	1
g[0]	1
b	5
b[3]	0
b[2]	1
b[1]	0
b[0]	1

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Cursor 1

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