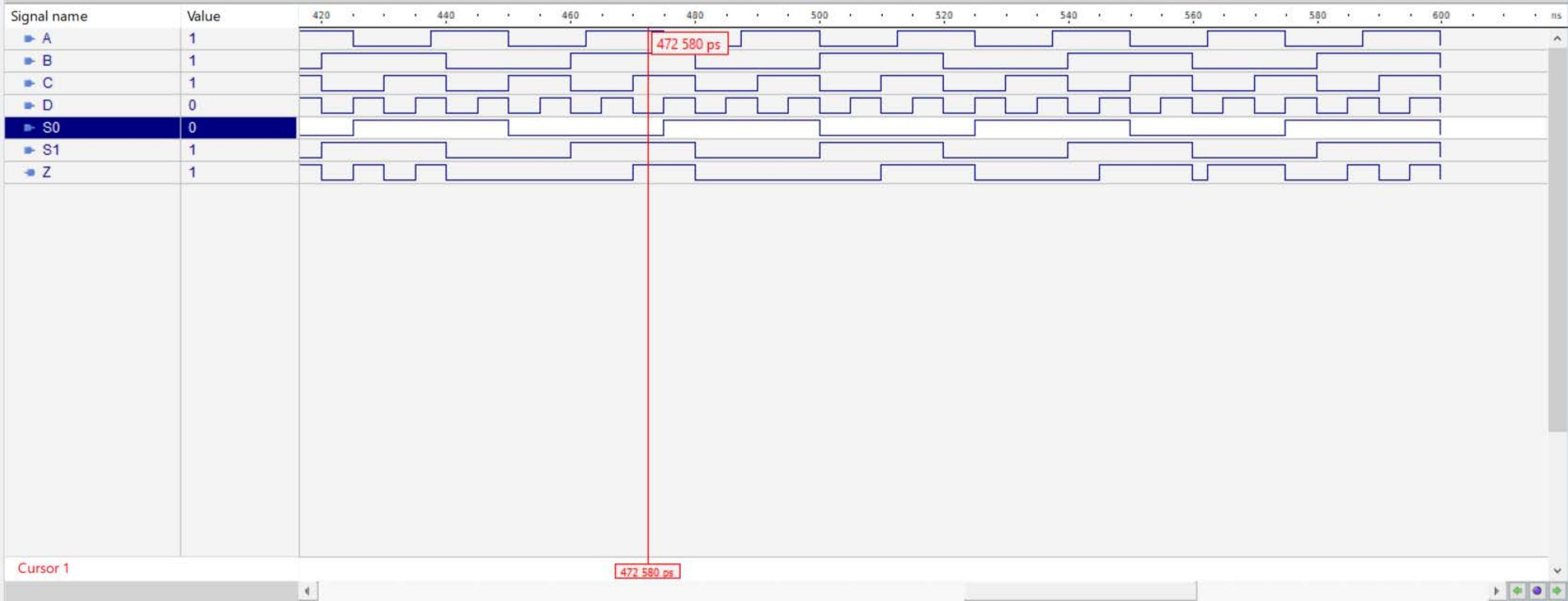
4:1 MUX

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.all;
3
4   entity mux_4to1 is
5    port(
6        A,B,C,D : in STD_LOGIC;
7        S0,S1: in STD_LOGIC;
8        Z: out STD_LOGIC);
9   end mux_4to1;
10
11  architecture MUX of mux_4to1 is
12  begin
13  process (A,B,C,D,S0,S1) is
14  begin
15    if (S0 ='0' and S1 = '0') then
16        Z <= A;
17    elsif (S0 ='1' and S1 = '0') then
18        Z <= B;
19    elsif (S0 ='0' and S1 = '1') then
20        Z <= C;
21    else
22        Z <= D;
23    end if;
24  end process;
25  end MUX;
26
```


Signal name
Value
420
440
460
480
500
520
540
560
580
600
ns
A
1
B
1
C
1
D
0
S0
0
S1
1
Z
1
472 580 ps
Cursor 1
472 580 ps