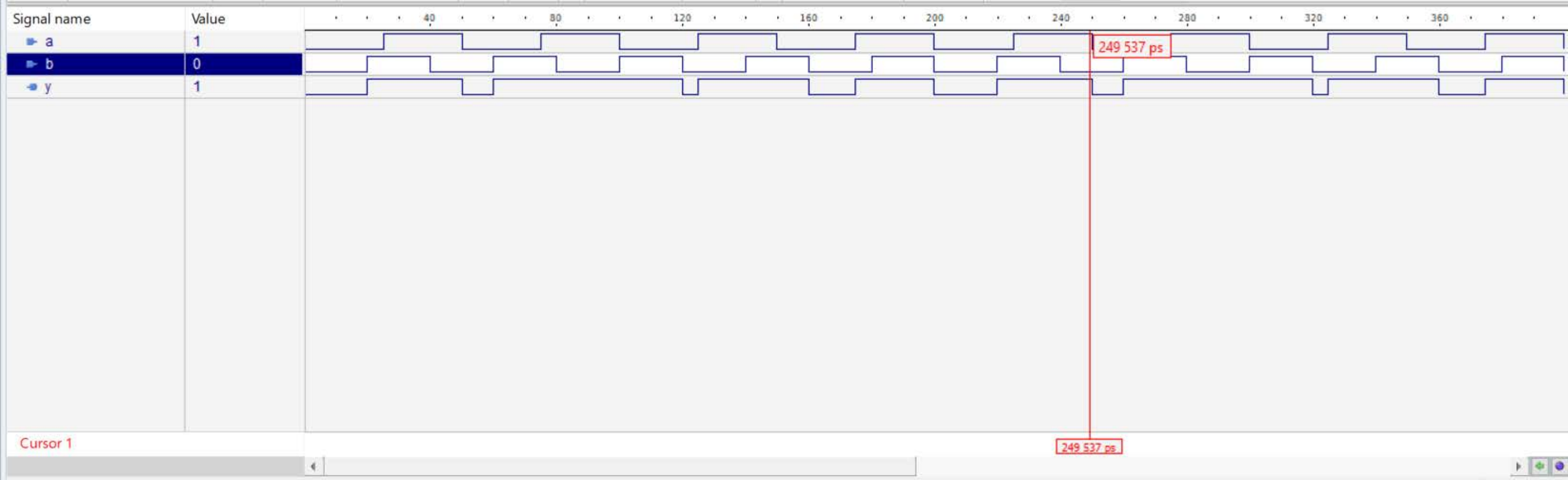
OR gate using 2:1 MUX

```
1
2   library ieee;
3    use IEEE.STD_LOGIC_1164.ALL;
4   entity orgate is
5        port(  A:IN std_logic;
6               B:IN std_logic;
7               Y:IN std_logic  );
8    end orgate;
9     architecture sms of orgate is
10    component mux is
11       port(  I0:IN std_logic;
12              I1:IN std_logic;
13              S1:IN std_logic;
14              y:OUT std_logic     );
15   end component;
16
17    begin
18
19    mux1:mux port map(IO=>B,I1=>A,S1=>A,y=>Y);
20  end sms;
21
22    library ieee; use
23  IEEE.STD_LOGIC_1164.ALL;
24
25  entity mux is
26   port(  I0:IN std_logic;
27          I1:IN std_logic;
28          S1:IN std_logic;
29          y:OUT std_logic     );
30   end mux;
31
32    architecture orgate_arch of mux is
33  begin
34   y<= I0
35  when S1='0'
36  Else
37  I1;
38
39  end orgate_arch
```


Signal name
Value
40
80
120
160
200
240
280
320
360
a
1
b
0
y
1
249 537 ps
Cursor 1
249 537 ps