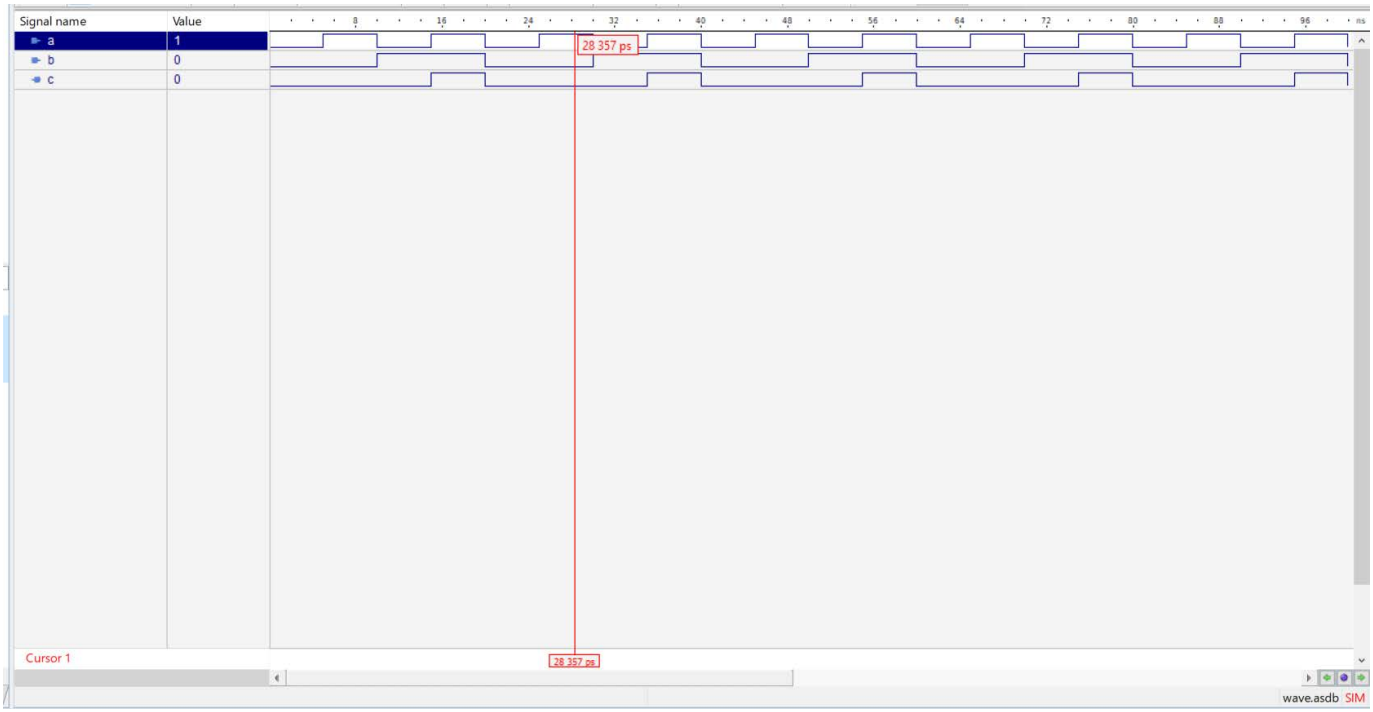
2 input AND gate

```
1   Library IEEE;
2
3   use IEEE.std_logic_1164.all;
4
5
6   entity andgate is
7
8       port(a,b : in bit;
9
10          c : out bit );
11
12  end andgate;
13
14
15  architecture andLogic of andgate is
16
17      begin
18
19          c <= a AND b;
20
21  end andLogic;
22
```

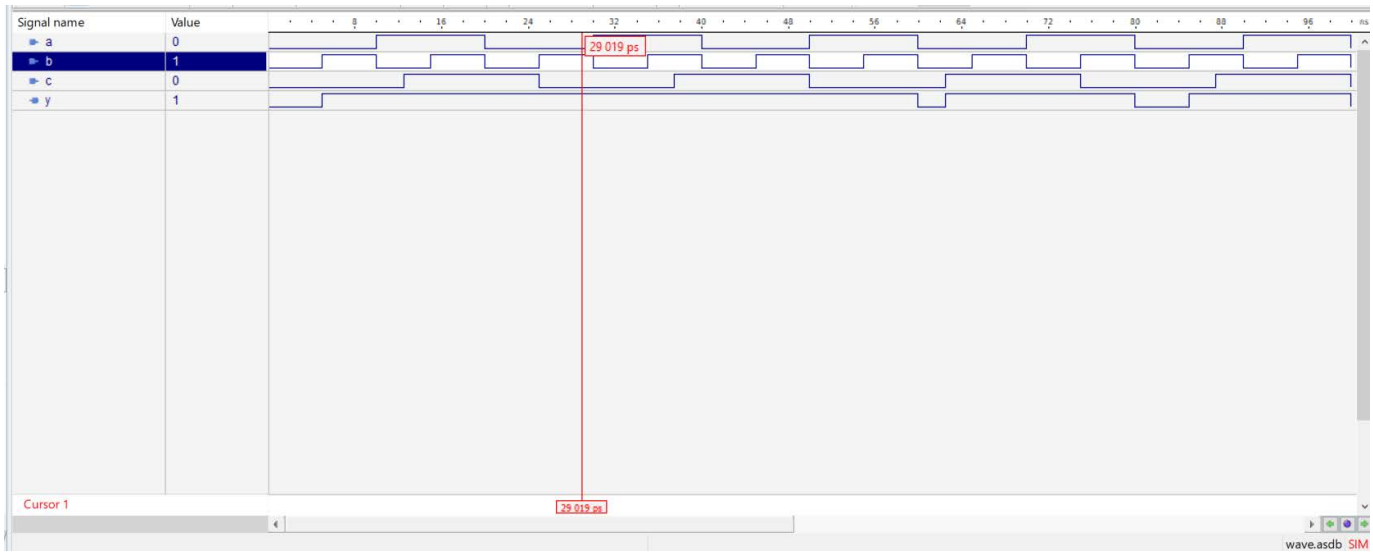
Waveform



3 input OR gate.

```
1   Library IEEE;
2
3   use IEEE.std_logic_1164.all;
4
5
6   entity orgate is
7
8       port(a,b,c : in bit;
9
10          y : out bit );
11
12  end orgate;
13
14
15  architecture orLogic of orgate is
16
17      begin
18
19          y <= a OR b OR c;
20
21  end orLogic;
22
```

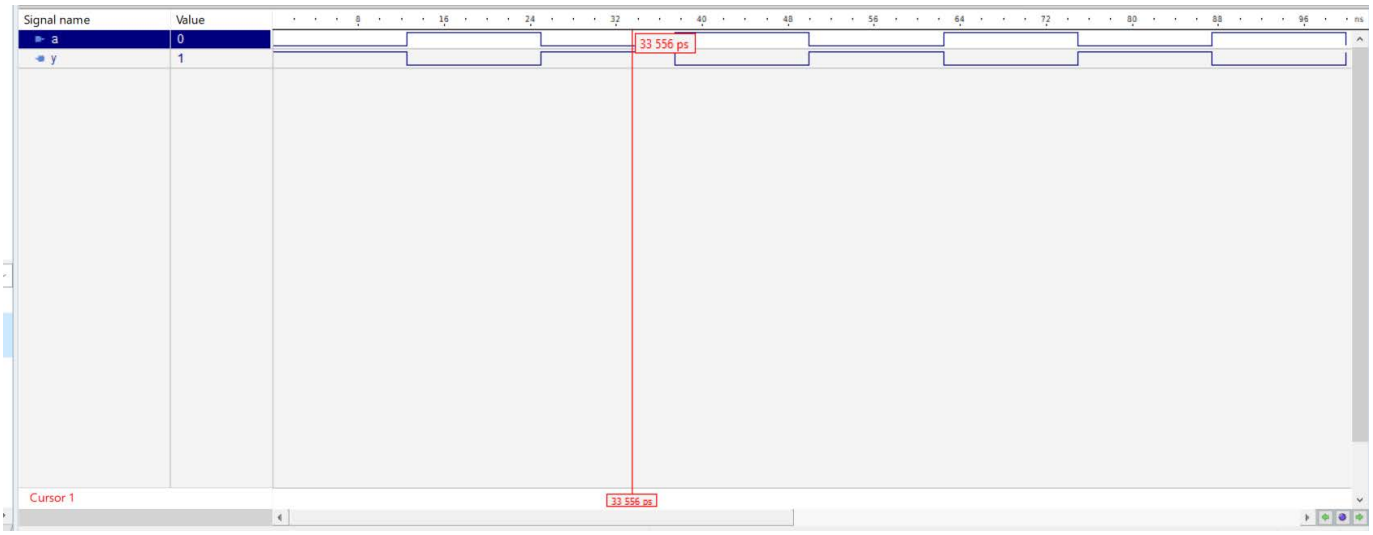
Waveform



1 input NOT gate.

```
1   Library IEEE;
2
3   use IEEE.std_logic_1164.all;
4
5
6   entity notgate is
7
8       port(a: in bit;
9
10           y : out bit );
11
12  end notgate;
13
14
15  architecture notLogic of notgate is
16
17      begin
18
19          y <= NOT a;
20
21
22  end notLogic;
23
```

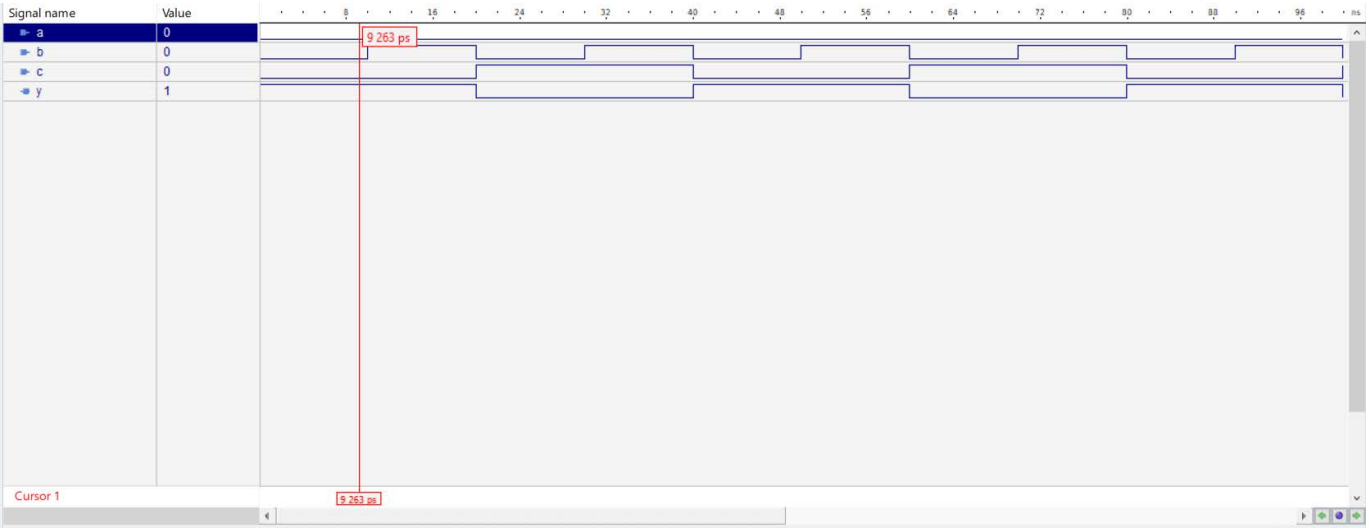
Waveform



3 input NAND gate.

```
1   Library IEEE;
2
3   use IEEE.std_logic_1164.all;
4
5
6   entity nandgate is
7
8       port(a,b,c : in bit;
9
10          y : out bit );
11
12  end nandgate;
13
14
15  architecture nandLogic of nandgate is
16
17      begin
18
19          y <= (a nand b) nand c;
20
21  end nandLogic;
22
```

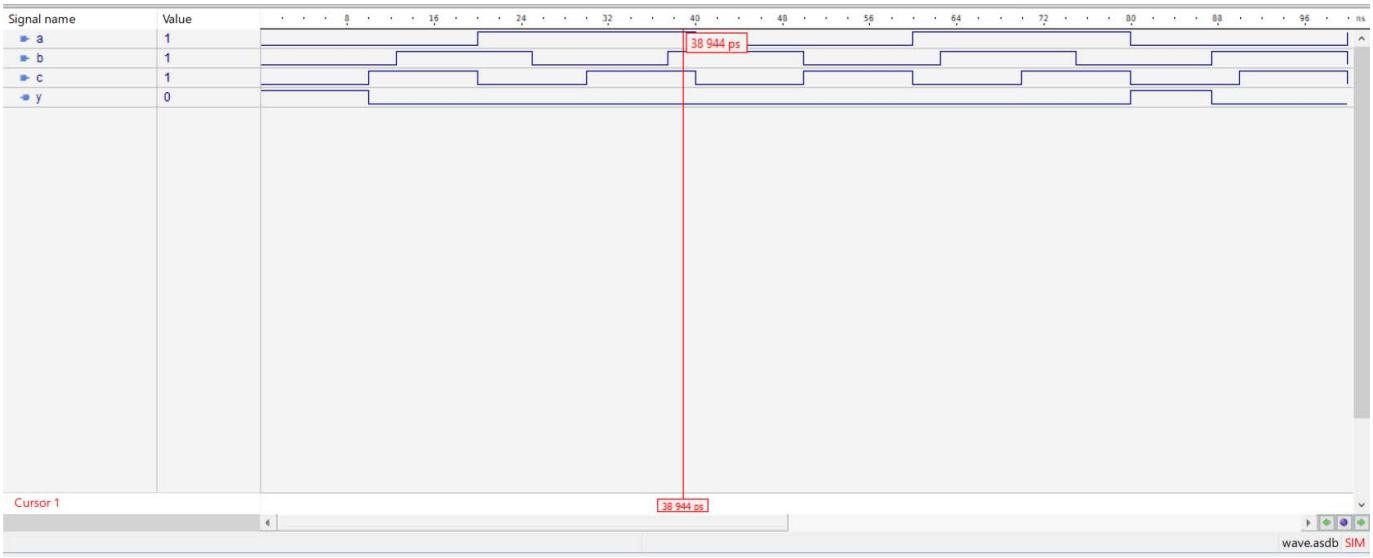
Waveform



3 input NOR gate.

```
1   Library IEEE;
2
3   use IEEE.std_logic_1164.all;
4
5
6   entity norgate is
7
8       port(a,b,c : in bit;
9
10          y : out bit );
11
12  end norgate;
13
14
15  architecture norLogic of norgate is
16
17      begin
18
19          y <= (a nor b) nor c;
20
21  end norLogic;
22
```

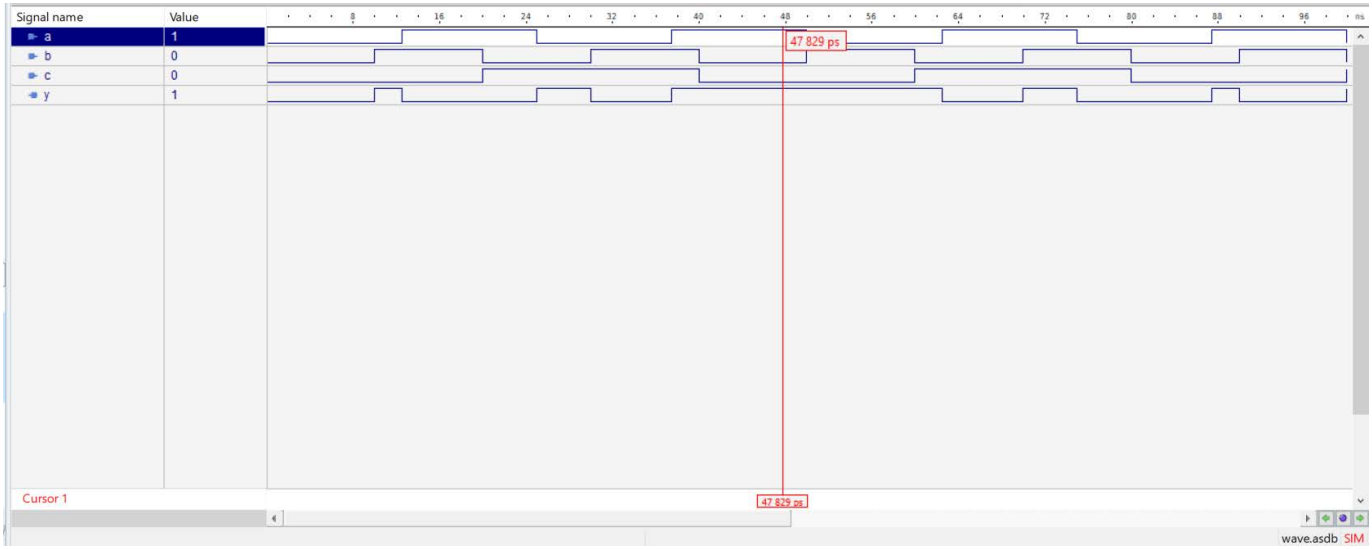
Waveform



3 input XOR gate

```
1   Library IEEE;
2
3   use IEEE.std_logic_1164.all;
4
5
6   entity exorgate is
7
8       port(a,b,c : in bit;
9
10          y : out bit );
11
12  end exorgate;
13
14
15  architecture exorLogic of exorgate is
16
17      begin
18
19          y <= a xor b xor c;
20
21  end exorLogic;
22
```

Waveform



2 input XNOR gate

```
1   Library IEEE;
2
3   use IEEE.std_logic_1164.all;
4
5
6   entity exnorgate is
7
8       port(a,b : in bit;
9
10          y : out bit );
11
12  end exnorgate;
13
14
15  architecture exnorLogic of exnorgate is
16
17      begin
18
19          y <= a xnor b ;
20
21  end exnorLogic;
22
```

Waveform