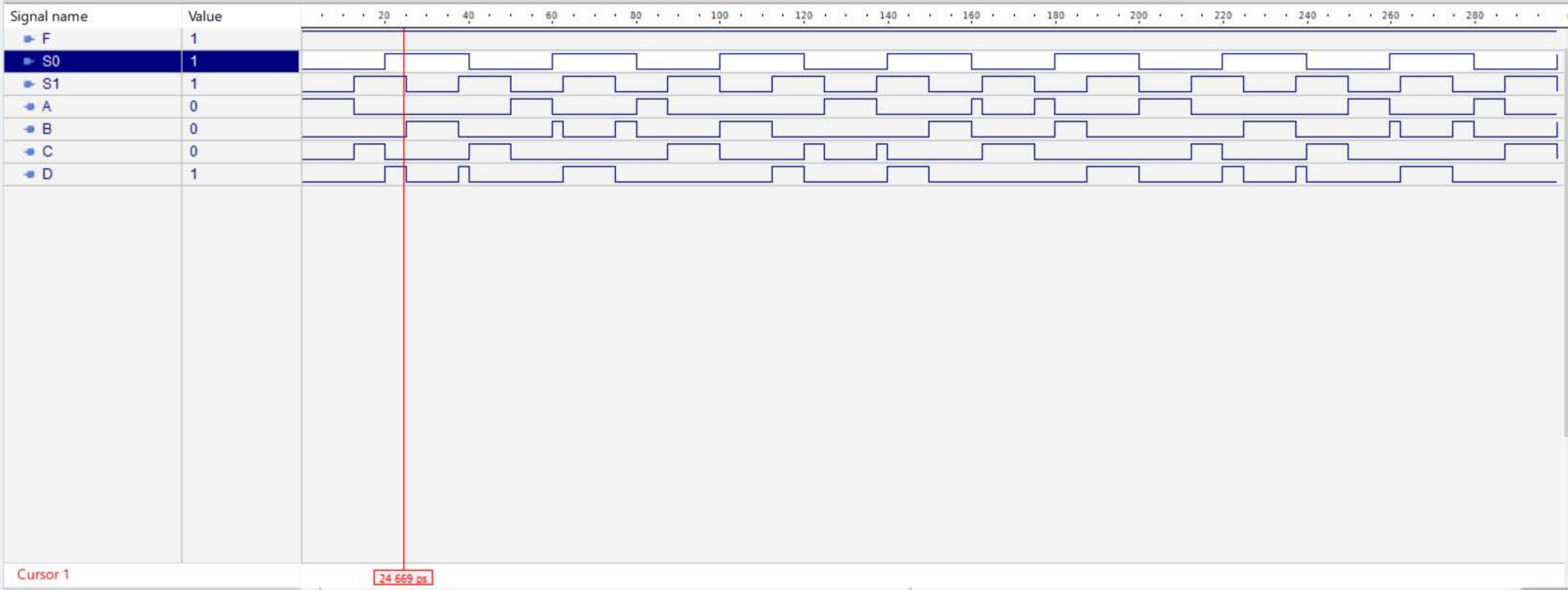
1:4 DE-MUX

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.all;
3
4   entity demux_1to4 is
5    port(
6
7    F : in STD_LOGIC;
8    S0,S1: in STD_LOGIC;
9    A,B,C,D: out STD_LOGIC
10   );
11  end demux_1to4;
12
13  architecture bhv of demux_1to4 is
14  begin
15  process (F,S0,S1) is
16  begin
17   if (S0 ='0' and S1 = '0') then
18   A <= F;
19   B <='0';
20   C <='0';
21   D <='0';
22
23   elsif (S0 ='1' and S1 = '0') then
24   B <= F;
25   A <='0';
26   C <='0';
27   D <='0';
28
29   elsif (S0 ='0' and S1 = '1') then
30   C <= F;
31   A <= '0';
32   B <= '0';
33   D <= '0';
34
35   else
36   D <= F;
37   A <= '0';
38   B <= '0';
39   C <= '0';
40   end if;
41
42  end process;
43  end bhv;
44
```


Signal name
Value
20
40
60
80
100
120
140
160
180
200
220
240
260
280
F
1
S0
1
S1
1
A
0
B
0
C
0
D
1
Cursor 1
24 669 ps