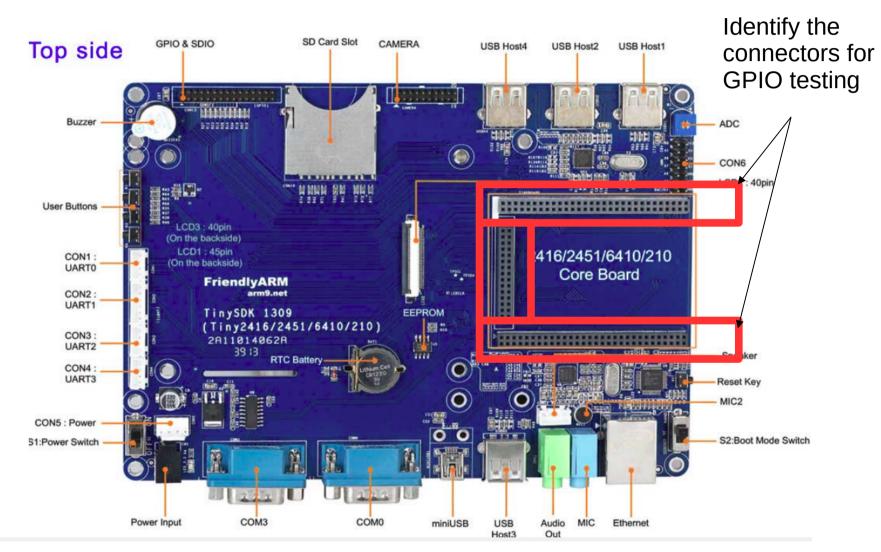
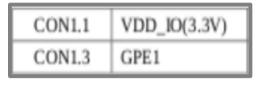
Connector with CPU GPIO Pins



Note: Check your board revision number, you may have different type of board and different connectors, check the vendor document

CON1 Connector with GPIO Pins

Table 1. CON1 Pin Assignment



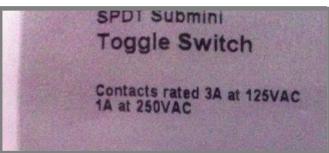
CON 1.2	GND
CON 1.4	GPE2

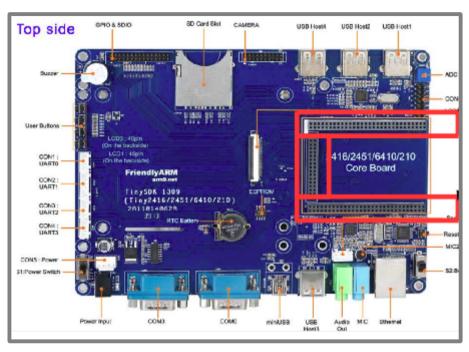
Reference: Vendor Document, or my class handout, see github.com/hualili

Table 2. GPIO I/O testing

CPU	CON1	Description	
GPE1	1.3	output	
GPE2	1.4	input	







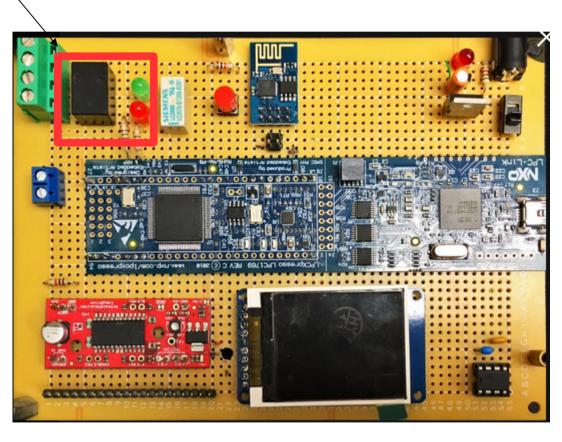
- 1. SPDT switch for GPIO input testing;
- 2. Build circuit for input testing and output testing. Output testing will have to

allow GPP port to drive LED On/Off.

A Single Pole Double Throw (SPDT) switch is a switch that only has a single input and can connect to and switch between 2 outputs.

GPIO (GPP) Output with SSR

SSR: Solid State Relay

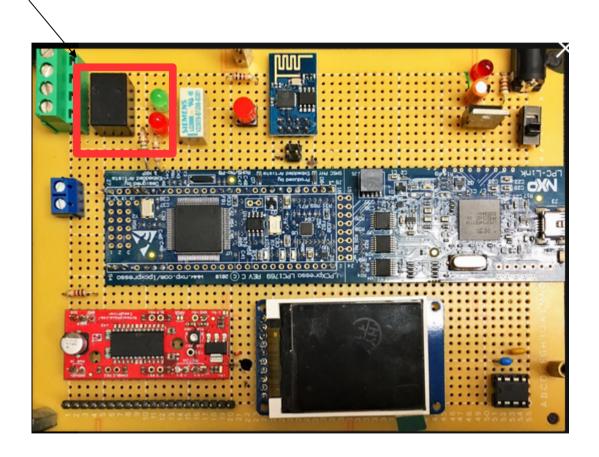




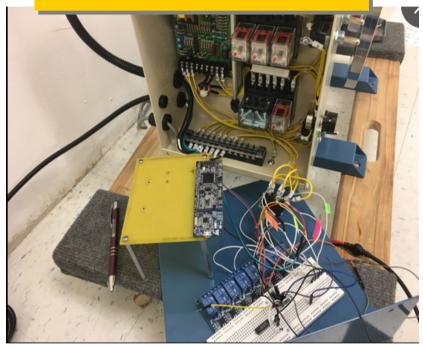
SSR: Solid State Relay

GPIO (GPP) Output SSR Applications

SSR: Solid State Relay



SMT-POS Positioner





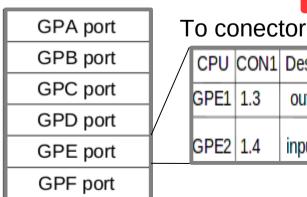
ARM GPIO (GPP) Controller and **SPRs**

1. Definition of SPRs: Special purpose registers are those to perform init and config functions.

2. 32 bit each with unique address.

3. In IDE (software, e.g., linux-arm-gcc in this case), *.h file with something looks like the following #define SPR 0x2000 0000 map the CPU architecture

to the arm gcc compiler



ARM Core Multimedia Acceleration System Peripheral Camera I/F RTC ARM1176JZF-S Multi Format CODEC I/D-Cache 16KB PLL x 3 (H.264/MPEG4/VC1) I/D-TCM 16KB 533/667MHz Timer w/ PWM NTSC. PAL TV out with Image Enhancement Watch-Dog Timer **JPEG** DMA(32 ch) 2D Graphics Keypad (8 x 8) 3D Graphics X64 / 32 Multi - Layer AHB / AXI Bus Connectivity 12S / 12S 5-ch Memory Subsystem 12C x 2 SRAM/ROM/NOR/ OneNAND UART x 4 Mobile SDRAM Mobile DDR SDRAM SPI (Full Duplex) NAND Flash CPU CON1 Description HIS (Modern 1/F) USB OTG 2.0 output Power TFT LCD USB Host 1.1 Controller Management HS-MMC/SD input Resolution typically Normal, Idle 97 / PCM Audio I/F 800x480 Stop, Sleep

Ref: pp. 306 datasheet

Harry Li, Ph.D. SJSU CMPE 242

GPE1 1.3

GPE2 | 1.4

CPU datasheet Chapter1 Ref: pp. 61 datasheet

Pwr up address 0x0000 0000

Memory Map

SPR: GPECON Description

Reference: CPU Datasheet, 10.4 REGISTER DESCRIPTION

GPECON (Compiler used name: GPECON)

GPECON	0x7F008080	Configuration Register	
GPEDAT	0x7F008084	Data Register	
GPEPUD	0x7F008088	Pull up/down Register	

Example: GPE Init & Config,

Set GPE1 output, "1" GPE2 input, "0"

So the binary pattern is 0x10

GPE1	[7:4]	0000 = Input 0010 = PCM EXTCLK[1]	0001 = Output 0011 = I2S CDCLK[1]
		0100 = AC97 RESETn 0110 = Reserved	0101 = Reserved 0111 = Reserved
GPE2	[11:8]	0000 = Input 0010 = PCM FSYNC[1] 0100 = AC97 SYNC 0110 = Reserved	0001 = Output 0011 = I2S LRCLK[1] 0101 = Reserved 0111 = Reserved

