

# A/D Converter

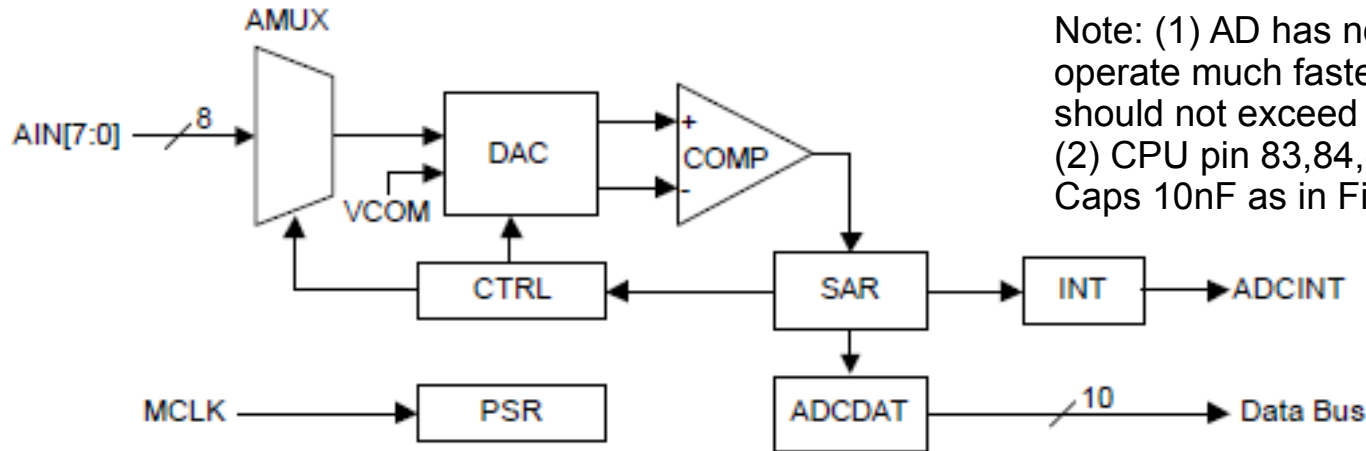


Fig 1

Note: (1) AD has no built-in S/H circuit. Even it can operate much faster, but without S/H, the sampling speed should not exceed 100 Hz;  
(2) CPU pin 83,84,85 must have external compensation Caps 10nF as in Fig 2;

(3) Problem 1 of the ADC: ADCCON's ADC state flag off by 1 right after the conversion starts and right before the conversion ends;

PSR	Prescaler register: define sample speed	
ADCCON	ADC control register	
ADCDAT	ADC data register	
SAR	Successive approximation register	

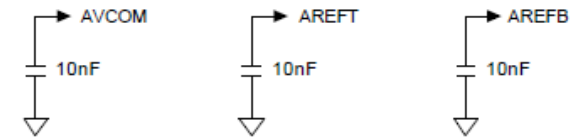


Fig 2

(4) Problem 2 of the ADC: No S/H therefore ADC error can be large, need to reduce the output impedance of the analog signal source.

$$f_{Conv} = \frac{CLK_{CPU}}{2 * (N_{PSR} + 1)} \quad \dots(1)$$

$$T_{Conv} = 1/f_{Conv} \quad \dots(2)$$

Example: For a given signal, we have  $f_{Sampling} = 98.2 \text{ KHz}$ , find  $N_{PSR}$  to realize this AD design requirement. Ans:  $N_{PSR} = 20$

# ADC Theoretical Background

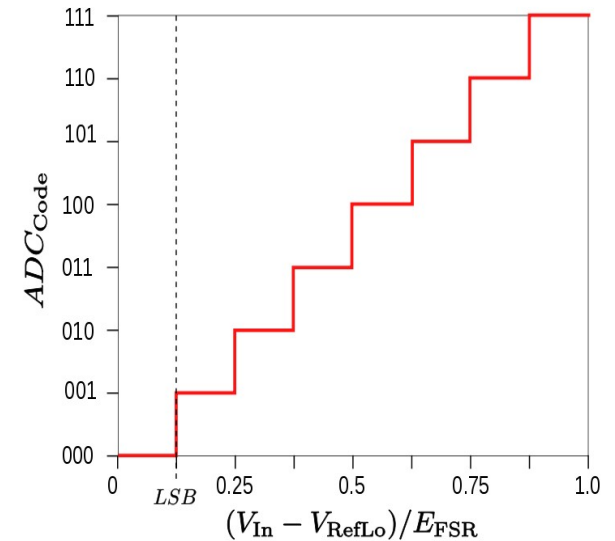
ADC voltage resolution Q calculation

$$Q = \frac{E_{FSR}}{N}$$

Where  $E_{FSR} = V_{R,High} - V_{R,Low}$

and

$$N = 2^x$$



[http://en.wikipedia.org/wiki/File:ADC\\_voltage\\_resolution.svg](http://en.wikipedia.org/wiki/File:ADC_voltage_resolution.svg)

Fig 3

Example 1

- \* Coding scheme as in figure 3
- \* Full scale measurement range = 0 to 10 volts
- \* ADC resolution is 12 bits:  $2^{12} = 4096$  quantization levels (codes)
- \* ADC voltage resolution,  $Q = (10V - 0V) / 4096 = 10V / 4096 \approx 0.00244 V \approx 2.44 mV$ .

DFT (FFT: fast Fourier Transform) based AD conversion validation.

# ADC Characterization

Today's Topics:

1° Introduction to ADC. (CPU Datasheet)

2° Data Validation.

Reference: CPU ADC Chapter (392)  
for ARM11 or Equivalent

Table 1 ADC Characterization

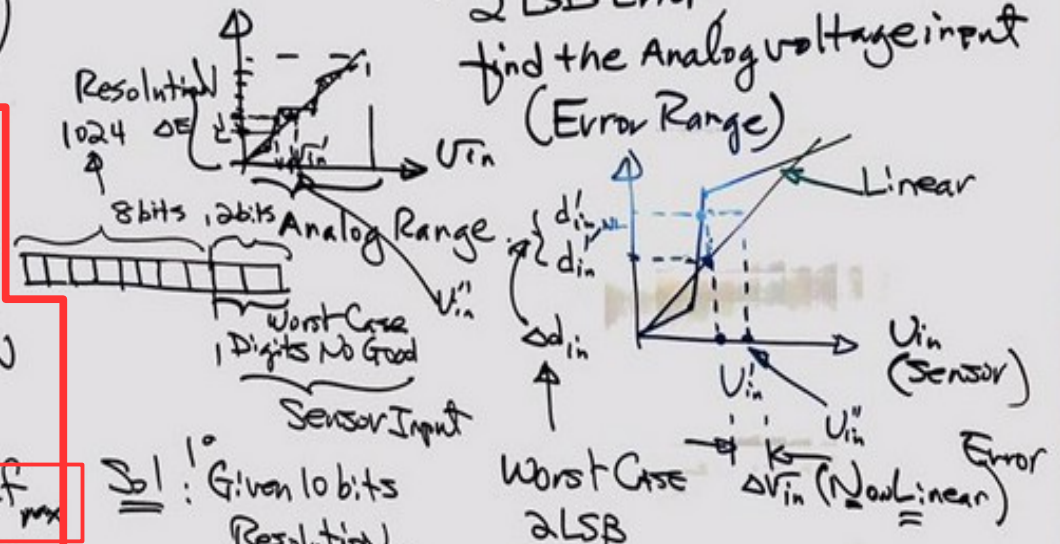
No	Description	Note
1° Resolution	10 bit (1024) 12 bit (4096)	Quantization Levels per given Resolution
2° Conversion Rate	1 MSPS	Conversion Time per Sample $f_{\text{Sampling}} \geq 2f_{\text{max}}$
3° Analog Input Range	[0, 3.3]	for Sensor I/F Design. OpAmp Preprocessing CKT.
4° Linearity (Non)	2LSB Difference	Calculation for Sensor Input

Note:

1° Conversion Time,  $T_{\text{conv}} = \frac{1}{f_{\text{Sampling}}} = 1 \times 10^{-6}$   
 $\mu\text{S} = 1 \times 10^{-6}$

2° Non-Linearity

Example: Given 2 LSB Error  
find the Analog voltage input (Error Range)



Sol: 1° Given 10 bits Resolution.

2° Analog Range 3.3V.

3° Therefore for LSB (1 bit):  $\frac{3.3V (\text{Full Range})}{1024 (\text{Full Resolution})} \approx 3.3 \times 10^{-3} \text{ VDC}$

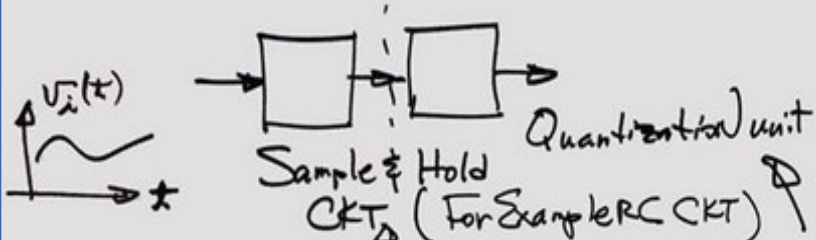
4° For Additional Bits:  $2^{10} (\text{LSB}) \rightarrow 1024$

Hence  $\frac{3.3V}{2^9} = 6.6 \times 10^{-3}$   
 $2^9 (\text{2 bits, LSB}) \rightarrow 512 \rightarrow \text{bit Error 1 Additional}$

# Introduction To DFT For Data Validation

April 16/2018 CMPE42 2/.

## ADC Hardware Aspects.



Quantization unit

Sample & Hold CKT (For Sample RC CKT)

Nyquist Theory

$f_{\text{Sampling}} \geq 2f_{\text{Max}}$

$\Delta t = \frac{1}{f_{\text{Sampling}}}$

Signal itself

$U_{\text{in}}$  from S+H.

$U_{\text{Ref}+}$

$U_{\text{Ref}-}$

$\tau = RC$

Define D.F.T.

Analog Sensor Output  $x(t)$

$x(t)$  (Vol/Current)

$x(n)$

$\Delta t = \frac{1}{f_{\text{Sampling}}}$

$f_{\text{Sampling}} = \frac{1}{\Delta t}$

$X(n) \leftrightarrow X(m)$  D.F.T.

Fourier Transform.

Frequency Index:  $0, 1, 2, \dots, N-1$

$m=0$ . D.C.

$m = \frac{N}{2}-1$  highest Freq. Index

$X(\frac{N}{2}-1)$  highest Freq. Component

$N$ : Total of Pts per period

$X(m) = X(m+k \cdot N)$   $k=1, 2, \dots$

$N$  pts: ONE period.

Signal

Basis function

Compare to Taylor Expansion.

$f(x) = f(x_0) + \frac{f'(x_0)}{1!}(x-x_0) + \frac{f''(x_0)}{2!}(x-x_0)^2 + \dots$

$f(x) = c + a(x-x_0)$

$y = ax + b$

\* Let's Consider Data Validation.  
(To verify if  $f_{\text{Sampling}} \geq 2f_{\text{Max}}$ )

$X(m) = \frac{1}{N} \sum_{n=0}^{N-1} X(n) e^{-j2\pi \frac{mn}{N}}$  ... (I)