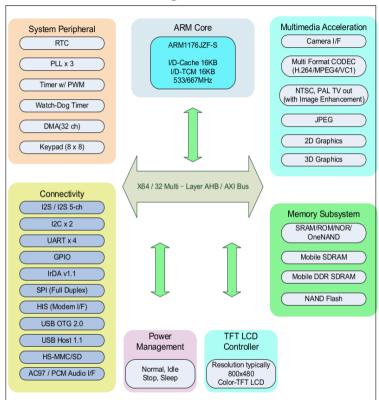
ARM11 Architecture

CPU Block Diagram

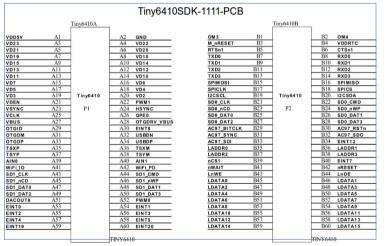


GPIO Special Purpose Registers

	•	i			
PortName	Number of Pins.	Muxed pins	Power Inform.		
GPA port	8	UART/EINT	1.8~3.3V		
GPB port	7	UART/IrDA/I2C/CF/Ext.DMA/EINT	1.8~3.3V		
GPC port	8	SPI/SDMMC/I2S_V40/EINT	1.8~3.3V		
GPD port	5	PCM/I2S/AC97/EINT	1.8~3.3V		
GPE port	5	PCM/I2S/AC97	1.8~3.3V		
GPF port	16	CAMIF/PWM/EINT	1.8~3.3V		
GPG port	7	SDMMC/EINT	1.8~3.3V		

Memory Map (Partial)

Start	End	Int.	Stepping	SROM	One	One	DRAM
Address	Address	ROM	Stone	Ctrl.	NAND	NAND	Ctrl 1
			(NAND Ctrl.)		Ctrl. 0	Ctrl. 1	
0x00000000	0x07FFFFF	O ¹	-	O ¹	O ¹	-	-
0x08000000	0x0BFFFFFF	0	-	-	-	-	-
0x0C000000	0x0FFFFFFF	-	0	-	-	-	-
0x10000000	0x17FFFFFF	-	-	0	-	-	-
0x18000000	0x1FFFFFFF	-	-	0	-	-	-
0x20000000	0x27FFFFFF	-	-	O ²	O ²	-	-
0x28000000	0x2FFFFFFF	-	-	O ²		O ²	-
0x30000000	0x37FFFFFF	-	-	0	-	-	-
0x38000000	0x3FFFFFFF	-	-	0	-	-	-
0x40000000	0x47FFFFF	-	-	-	-	-	-
0x48000000	0x4FFFFFF	-	-	-	-	-	-
0x50000000	0x5FFFFFFF	-	-	-	-	-	0
0x60000000	0x6FFFFFF	-	-	-	-	-	0

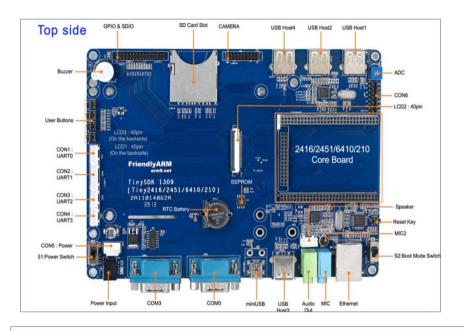


Connector information

Process for GPIO Testing

Development Kit

Schematic of the development kit



				Tiny6410SD	K-1111-PCB				
		Tiny6410A	1				Tiny6410B	1	
VDD5V	A1		A2	GND	OM 3	Bl		B2	OM4
VD23	A3	1	A4	VD22	M_nRESET	B3	1	B4	VDDRTC
/D21	A5	1	A6	VD20	RT Sn1	B5	1	B6	CTSn1
/D19	A7	1	A8	VD18	TXD0	B7	1	B8	RXD0
/D15	A9	1	A10	VD14	TXD1	B9	1	B10	RXD1
/D13	A11	1	A12	VD12	TXD2	B11	1	B12	RXD2
/D11	A13	1	A14	VD10	TXD3	B13	1	B14	RXD3
/D7	A15	1	A16	VD6	SPIMOSI	B15	1	B16	SPIMISO
/D5	A17	1	A18	VD4	SPICLK	B17	1	B18	SPICS
/D3	A19	Tiny6410	A20	VD2	12CSCL	B19	Tiny6410	B20	12CSDA
/DEN	A21		A22	PWM1	SD0_CLK	B21		B22	SD0_CMD
SYNC	A23	P1	A24	HSYNC	SD0_nCD	B23	P2	B24	SD0_nWP
/CLK	A25	1	A26	GPE0	SD0_DAT0	B25	1	B26	SD0_DAT1
/BUS	A27	1	A28	OT GDRV_VBUS	SD0_DAT2	B27	1	B28	SD0_DAT3
OTGID	A29	1	A30	EINT8	AC97_BITCLK	B29	1	B30	AC97_RSTn
OTGDM	A31	1	A32	USBDN	AC97_SYNC	B31	1	B32	AC97_SDO
OTGDP	A33	1	A34	USBDP	AC97_SDI	B33	1	B34	EINT12
SXP	A35	1	A36	TSXM	LADDR0	B35	1	B36	LADDR1
SYP	A37	1	A38	TSYM	LADDR2	B37	1	B38	LADDR3
AINO	A39	1	A40	AIN1	nCS1	B39	1	B40	EINT7
NiFi_IO	A41	1	A42	WiFi_PD	nWAIT	B41	1	B42	nRESET
SD1_CLK	A43	1	A44	SD1_CMD	LnWE	B43	1	B44	LnOE
SD1_nCD	A45	1	A46	SD1 nWP	LDATA0	B45	1	B46	LDATA1
SD1 DAT0	A47	1	A48	SD1 DAT1	LDATA2	B47	1	B48	LDATA3
SD1 DAT2	A49	1	A50	SD1 DAT3	LDATA4	B49	1	B50	LDATA5
DACOUT0	A51	1	A52	PWM0	LDATA6	B51	1	B52	LDATA7
EINTO	A53	1	A54	EINT1	LDATA8	B53	1	B54	LDATA9
EINT2	A55	1	A56	EINT3	LDATA10	B55		B56	LDATA11
EINT4	A57	1	A58	EINT5	LDATA12	B57	1	B58	LDATA13
EINT19	A59	1	A60	EINT20	LDATA14	B59	1	B60	LDATA15

Connector information

Device driver

Modify menuconfig script

Compile and build device driver module

Upload the device driver module and user application program to the target platform

\$insmod device-driver.ko
Then run the user application program

User space: user application program, compile and build the executable

Kernel space:

Device driver example code from source distribution

ARM11 6410 Connectors

Tiny6410-1107

				Imiyorio i	107			
	P1					P2		
VDDIN	1	2	GND		OM3		OM4	į
VD23	3	4	VD22		M_nRESET	1 2		RTC
VD21	5	6	VD20		RTSn1	3 4	CTS	 n1
VD19	7	8	∨D18		TXD0	5 6	RXD	0
VD15	9	10	VD14		TXD1	7 8	RXD	1
VD13	11	12	VD12		TXD2	9 10	RXD	2
VD11	13	14	VD10		TXD3	11 12	RXD	3
VD7	15	16	VD6		SPIMOSI	13 14		/IISO
VD5	17	18	VD4		SPICLK	15 16	SPIC	
VD3	19	20	VD2		I2CSCL	17 18	I2CS	
VDEN	21	22	PWM1		SD0_CLK	19 20		CMD
VSYNC	23	24	HSYNC		MMC0_CDn	21 22		0 WPn
VCLK	25	26	GPE0		SD0_DAT0	23 24		DAT1
VBUS	27	28	OTGDRV_V	BUS	SD0_DAT2	25 26		DAT3
OTGID	29	30	XEINT8		AC97 BITCLK	27 28	() 	7 RSTn
OTGDM	31	32	USBDN		AC97_SYNC	29 30		7_SDO
OTGDP	33	34	USBDP		AC97_SDI	31 32		NT12
TSXP	35	36	TSXM		LADDR0	33 34	LAD	
TSYP	37	38	TSYM		LADDR2	35 36	LAD	
AIN0	39	40	AIN1		nCS1	37 38	XEIN	
WiFi_IO	41	42	WiFi_PD		nWAIT	39 40	nRE	
SD1_CLK	43	44	SD1_CMD		LnWE	41 42	LnOI	
SD1_nCD	45	46	SD1_nWP		LDATA0	43 44	LDA	TA1
SD1_DAT0	47	48	SD1_DAT1		LDATA2	45 46	LDA	TA3
SD1_DAT2	49	50	SD1_DAT3		LDATA4	47 48	LDA	TA5
DACOUT0	51	52	PWM0		LDATA6	49 50	LDA	TA7
XEINT0	53	54	XEINT1		LDAT A8	51 52	LDA	
XEINT2	55	56	XEINT3		LDATA10	53 54	LDA	TA11
XEINT4	57	58	XEINT5		LDATA12	55 56	LDA	TA13
XEINT19	59	60	XEINT20		LDATA14	57 58		TA15
						59 60	<u> </u>	
	HEADE	R 302	X2			HEADER 30	X2	

ARM11 6410 Connectors

Tiny6410SDK-1111-PCB

		Tiny6410A	_				Tiny6410B	_	
VDD5V VD23 VD21 VD19 VD15 VD13 VD11 VD7 VD5 VD3 VDEN VSYNC VCLK VBUS OTGID OTGDM OTGDP TSXP TSYP AIN0 WiFi_IO SD1_CLK SD1_nCD	A1 A3 A5 A7 A9 A11 A13 A15 A17 A19 A21 A23 A25 A27 A29 A31 A33 A35 A37 A39 A41 A43 A45	Tiny6410A Tiny6410 P1	A2 A4 A6 A8 A10 A12 A14 A16 A18 A20 A22 A24 A26 A28 A30 A32 A34 A36 A38 A40 A42 A44 A46	GND VD22 VD20 VD18 VD14 VD12 VD10 VD6 VD4 VD2 PWM1 HSYNC GPE0 OTGDRV_VBUS EINT8 USBDN USBDP TSXM TSYM AIN1 WiFi_PD SD1_CMD SD1_NWP	OM 3 M_nRESET RTSn1 TXD0 TXD1 TXD2 TXD3 SPIMOSI SPICLK I2CSCL SD0_CLK SD0_nCD SD0_DAT0 SD0_DAT0 SD0_DAT2 AC97_BITCLK AC97_SVNC AC97_SDI LADDR0 LADDR2 nCS1 nWAIT LnWE LDATA0	B1 B3 B5 B7 B9 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B35 B37 B39 B41 B43 B43	Tiny6410B Tiny6410 P2	B2 B4 B6 B8 B10 B12 B14 B16 B18 B20 B22 B24 B26 B28 B30 B32 B34 B36 B38 B40 B42 B44 B46	OM4 VDDRTC CTSn1 RXD0 RXD1 RXD2 RXD3 SPIMISO SPICS 12 CSDA SD0_CMD SD0_DAT1 SD0_DAT1 SD0_DAT3 AC97_RSTn AC97_SD0 EINT12 LADDR1 LADDR3 EINT7 nRESET LnOE LDATA1
VBUS OTGID OTGDM OTGDP TSXP TSYP AIN0 WiFi_IO SD1_CLK SD1_nCD SD1_DAT0 SD1_DAT2	A27 A29 A31 A33 A35 A37 A39 A41 A43 A45 A47		A30 A32 A34 A36 A38 A40 A42 A44 A46 A48	USBDN USBDP TSXM TSYM AIN1 WiFi_PD SD1_CMD SD1_nWP SD1_DAT1 SD1_DAT3	SD0_DAT2 AC97_BITCLK AC97_SYNC AC97_SDI LADDR0 LADDR2 nCS1 nWAIT LnWE LDATA0 LDATA2 LDATA4	B29 B31 B33 B35 B37 B39 B41 B43 B45 B47		B30 B32 B34 B36 B38 B40 B42 B44 B46 B48 B50	SD0_DAT3 AC97_RSTn AC97_SD0 EINT12 LADDR1 LADDR3 EINT7 nRESET LnOE LDATA1 LDATA3 LDATA5
DACOUTO EINTO EINT2 EINT4 EINT19	A51 A53 A55 A57 A59		A52 A54 A56 A58 A60 TINY641	PWM0 EINT1 EINT3 EINT5 EINT20	LDATA6 LDATA10 LDATA12 LDATA14	B51 B53 B55 B57 B59		B52 B54 B56 B58 B60 TINY641	LDATA7 LDATA9 LDATA11 LDATA13 LDATA15