# Feb-25-2019 Compensation Function for ADC

$f(x) + g(x) = ax + b$ … (1)

Where ax + b is the ideal linear characteristics of the ADC, f(x) is the actual ADC function (piece wise linear), and g(x) is the compensation function to be designed. Note b = 0, and a is a slop for the ADC, for 10 bits ADC, a = 1024/3.3, f(x) is from the ADC data characteristic curve and g(x) is the compensation function to be designed.

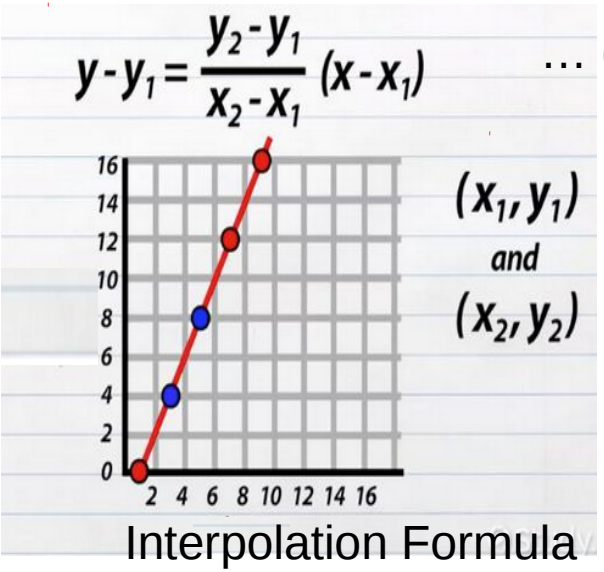
So f(x) + g(x) = ax and

Based on equation (2), we can write f(x) as

$f(x) = px + q$ … (3)

p and q can be found from the actual experiment. Substitute eqn(3) back to (1),

$$y - y_1 = \frac{y_2 - y_1}{x_2 - x_1}(x - x_1)$$ … (2)



Interpolation Formula

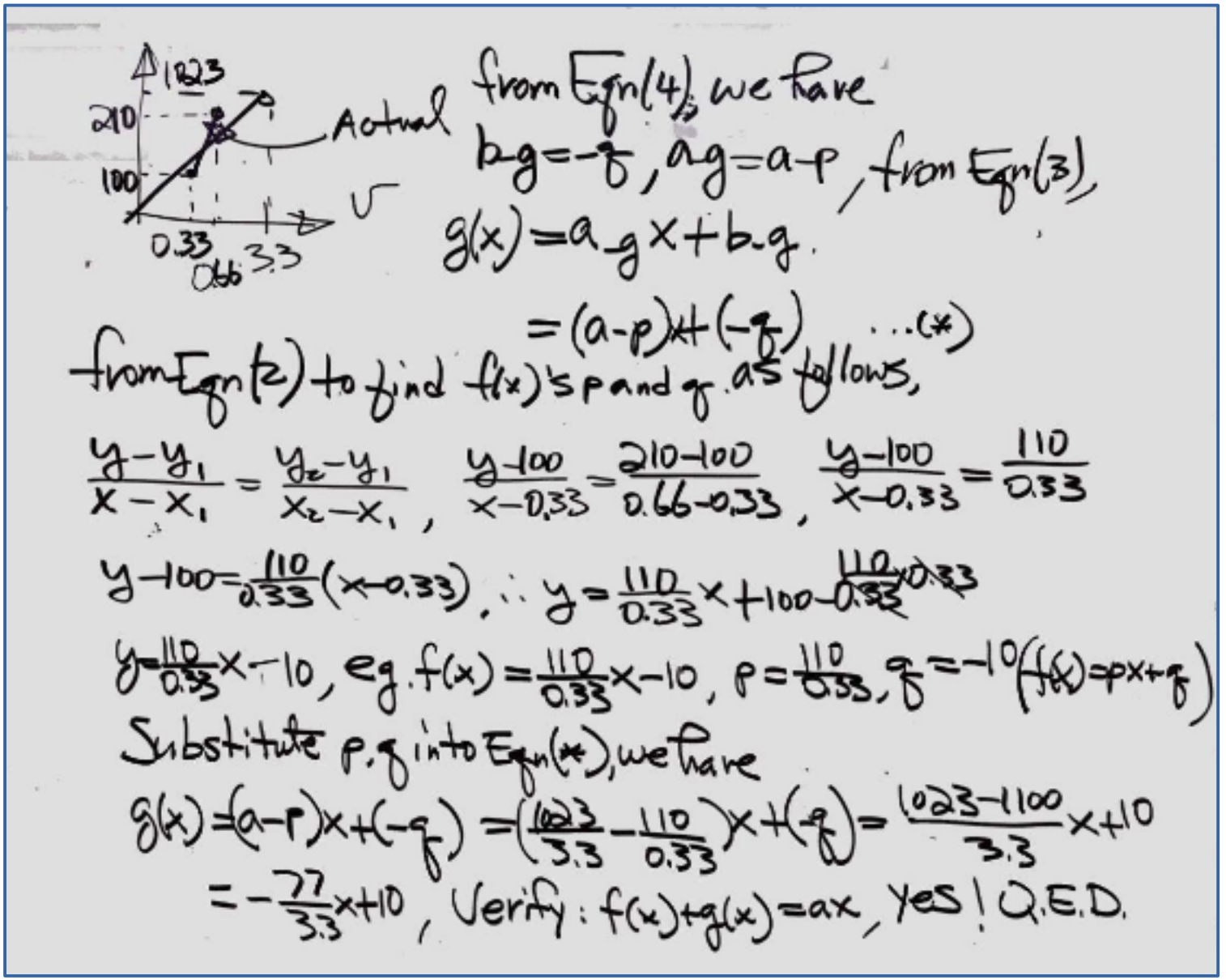
we have

$px + q + g(x) = ax$
$px + q + a_g\, x + b_g = ax$

Therefore:

$b_g = -q;\ a_g = (a - p)$ … (4)

# Feb-25-2019 ADC Compensation Example




from Eqn(4), we have

$b_g = -q$, $a_g = a - p$, from Eqn(3),

$g(x) = a_g x + b_g$.

$= (a-p)x + (-q)$ ...(*)

from Eqn(2) to find $f(x)$'s $p$ and $q$ as follows,

$\frac{y-y_1}{x-x_1} = \frac{y_2-y_1}{x_2-x_1}$, $\frac{y-100}{x-0.33} = \frac{210-100}{0.66-0.33}$, $\frac{y-100}{x-0.33} = \frac{110}{0.33}$

$y - 100 = \frac{110}{0.33}(x-0.33)$, $\therefore y = \frac{110}{0.33}x + 100 - \frac{110}{0.33}0.33$

$y = \frac{110}{0.33}x - 10$, eg. $f(x) = \frac{110}{0.33}x - 10$, $p = \frac{110}{0.33}$, $q = -10$ ($f(x) = px + q$)

Substitute $p, q$ into Eqn(*), we have

$g(x) = (a-p)x + (-q) = \left(\frac{1023}{3.3} - \frac{110}{0.33}\right)x + (q) = \frac{1023-1100}{3.3}x + 10$

$= -\frac{77}{3.3}x + 10$, Verify: $f(x) + g(x) = ax$, Yes! Q.E.D.

# A/D Converter

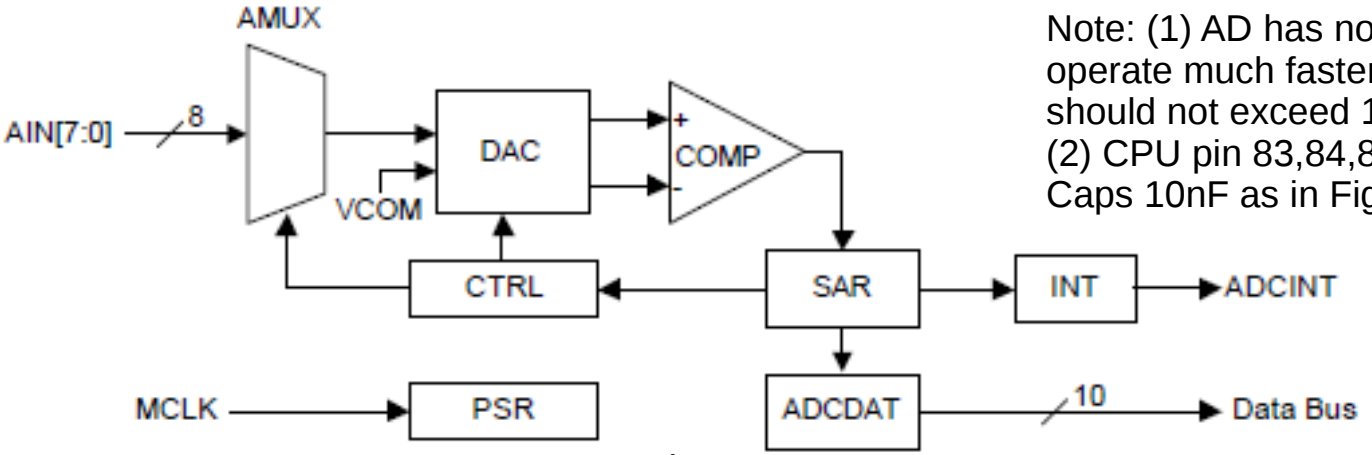



Fig 1

Note: (1) AD has no built-in S/H circuit. Even it can operate much faster, but without S/H, the sampling speed should not exceed 100 Hz;
(2) CPU pin 83,84,85 must have external compensation Caps 10nF as in Fig 2;

(3) Problem 1 of the ADC: ADCCON's ADC state flag off by 1 right after the conversion starts and right before the conversion ends;

| | | |
|---|---|---|
| PSR | Prescaler register: define sample speed | |
| ADCCON | ADC control register | |
| ADCDAT | ADC data register | |
| SAR | Successive approximation register | |

$$f_{Conv} = \frac{CLK_{CPU}}{2 * (N_{PSR} + 1)} \quad \ldots(1) \qquad T_{Conv} = 1/f_{Conv} \quad \ldots(2)$$

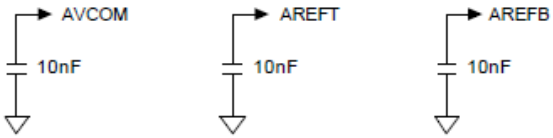



Fig 2

(4) Problem 2 of the ADC: No S/H therefore ADC error can be large, need to reduce the output impedance of the analog signal source.

*Example: For a given signal, we have $f_{Sampling}$ = 98.2 KHz, find $N_{PSR}$ to realize this AD design requirement. Ans: $N_{PSR}$ = 20*

# ADC Theoretical Background

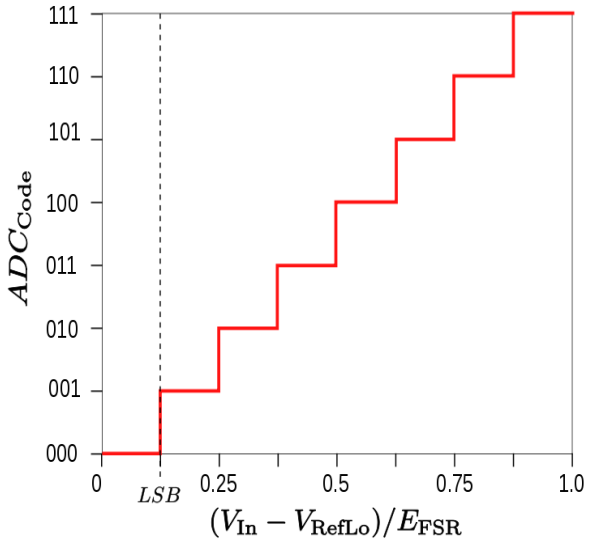
ADC voltage resolution *Q* calculation

$$Q = \frac{E_{FSR}}{N}$$

Where $E_{FSR} = V_{R,High} - V_{R,Low}$

and

$N = 2^X$




*http://en.wikipedia.org/wiki/File:ADC_voltage_resolution.svg*

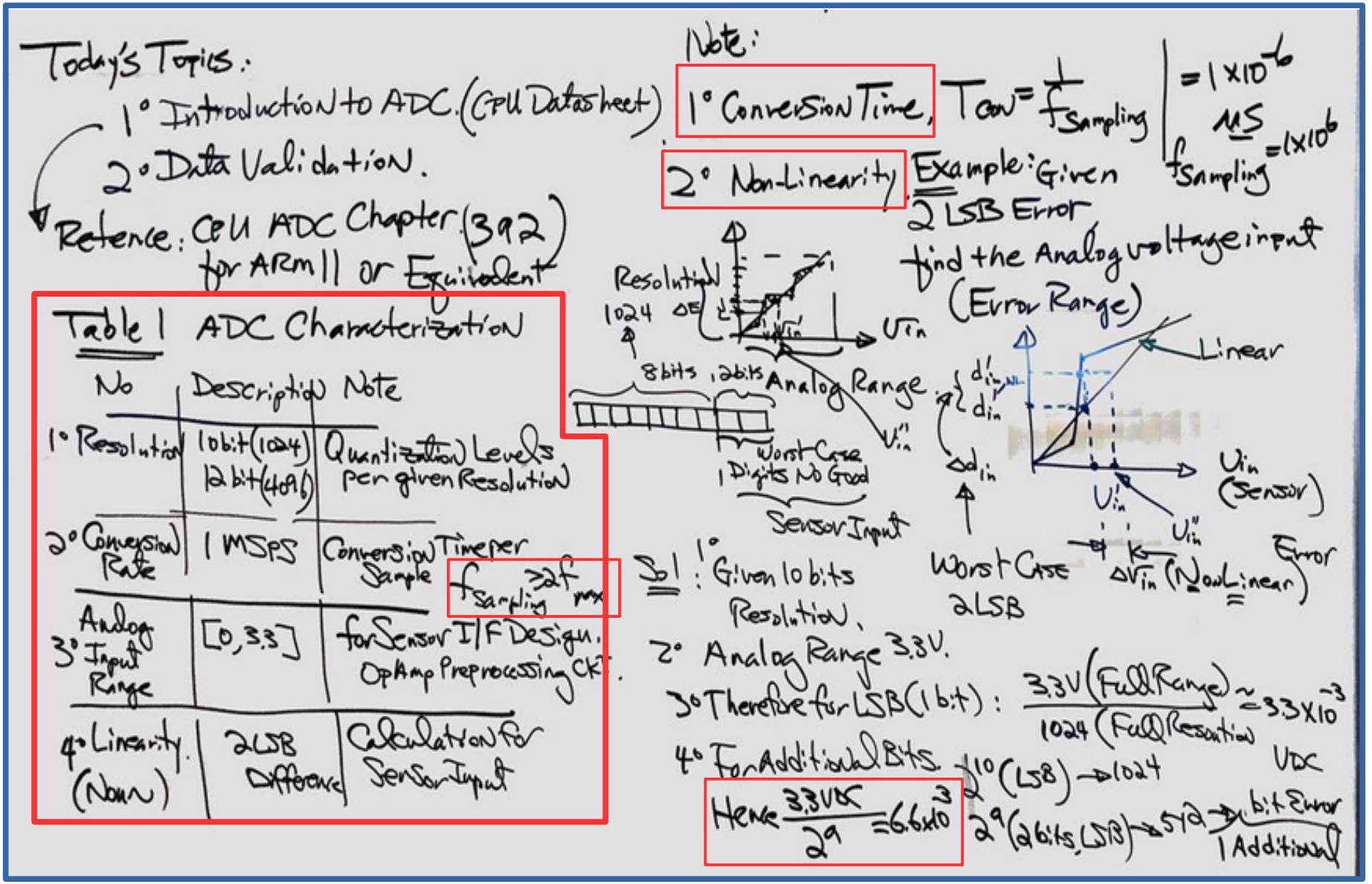
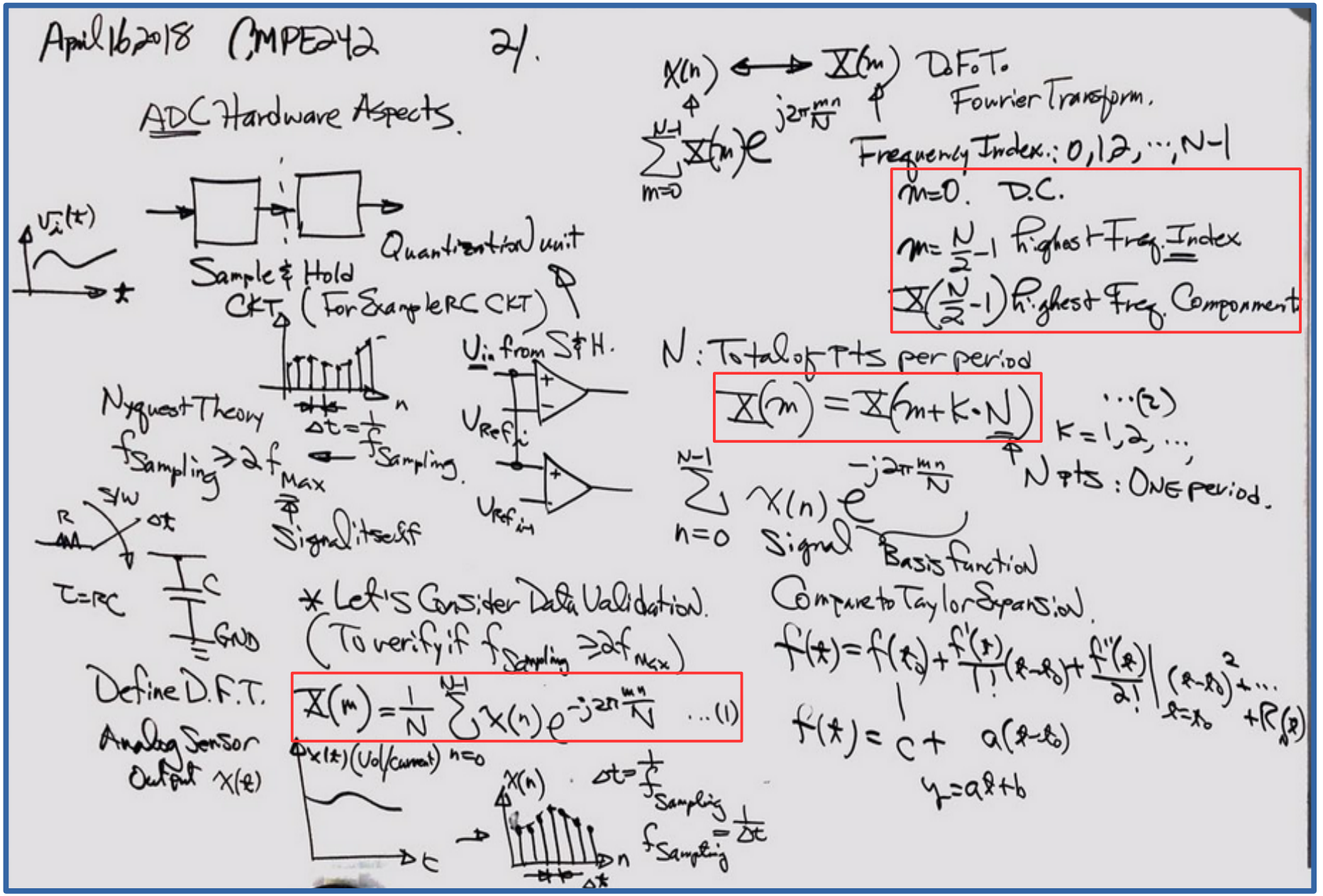
Fig 3

Example 1

* Coding scheme as in figure 3
* Full scale measurement range = 0 to 10 volts
* ADC resolution is 12 bits: 212 = 4096 quantization levels (codes)
* ADC voltage resolution, Q = (10V - 0V) / 4096 = 10V / 4096 \approx 0.00244 V \approx 2.44 mV.

DFT (FFT: fast Fourier Transform) based AD conversion validation.

# ADC Characterization



# Introduction To DFT For Data Validation