A/D Converter

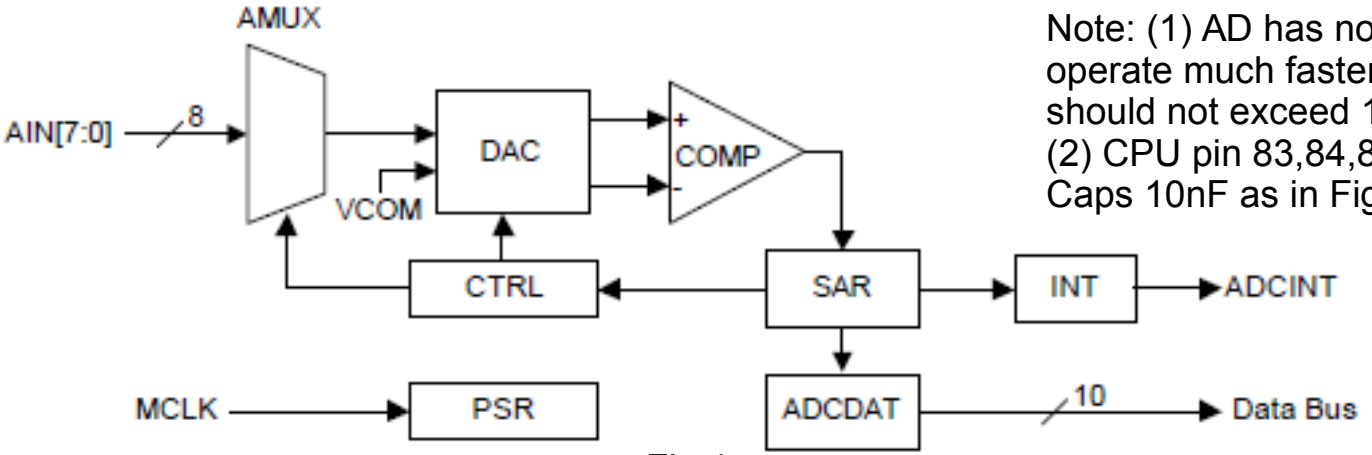


Fig 1

Note: (1) AD has no built-in S/H circuit. Even it can operate much faster, but without S/H, the sampling speed should not exceed 100 Hz;
(2) CPU pin 83,84,85 must have external compensation Caps 10nF as in Fig 2;

(3) Problem 1 of the ADC: ADCCON's ADC state flag off by 1 right after the conversion starts and right before the conversion ends;

PSR	Prescaler register: define sample speed	
ADCCON	ADC control register	
ADCDAT	ADC data register	
SAR	Successive approximation register	

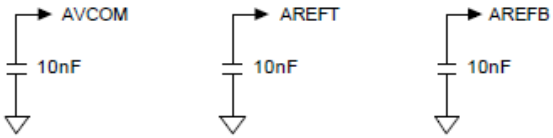


Fig 2

(4) Problem 2 of the ADC: No S/H therefore ADC error can be large, need to reduce the output impedance of the analog signal source.

$$f_{Conv} = \frac{CLK_{CPU}}{2 * (N_{PSR} + 1)} \quad \ldots(1) \qquad T_{Conv} = 1/f_{Conv} \quad \ldots(2)$$

Example: For a given signal, we have $f_{Sampling}$ = 98.2 KHz, find N_{PSR} to realize this AD design requirement. Ans: N_{PSR} = 20

ADC Theoretical Background

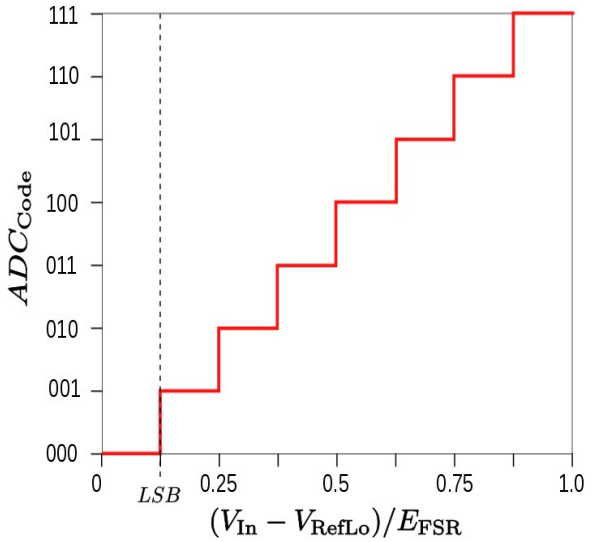
ADC voltage resolution *Q* calculation

$$Q = \frac{E_{FSR}}{N}$$

Where $E_{FSR} = V_{R,High} - V_{R,Low}$

and

$N = 2^X$



http://en.wikipedia.org/wiki/File:ADC_voltage_resolution.svg

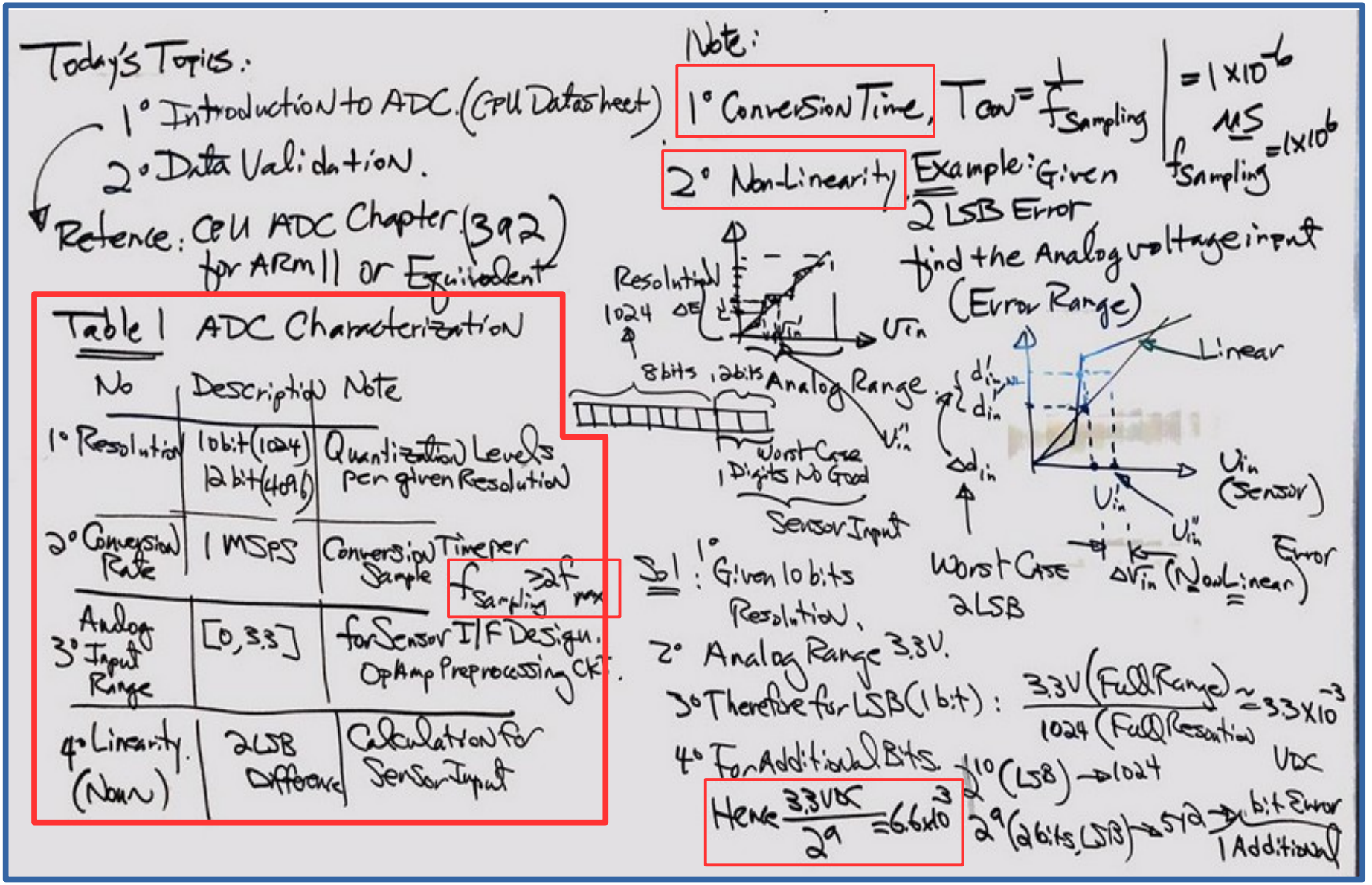
Fig 3

Example 1

* Coding scheme as in figure 3
* Full scale measurement range = 0 to 10 volts
* ADC resolution is 12 bits: 212 = 4096 quantization levels (codes)
* ADC voltage resolution, Q = (10V - 0V) / 4096 = 10V / 4096 \approx 0.00244 V \approx 2.44 mV.

DFT (FFT: fast Fourier Transform) based AD conversion validation.

ADC Characterization



Introduction To DFT For Data Validation