Review 2

Stepper Motor Control and PWM Timing Calculation

CMPE242

S2018

1. The following table is given to describe a typical stepper motor characteristics, based on the table information complete the blanks.

Table 1. Typical stepper motor characteristics

Configuration of the steps	Description	Note
Full step	1.8 degree	Per step
A half step		
A quarter step		
A 1/8 of a step	0.225 degree	

2. Typical stepper motor driving board, such as the one shown in Figure 1, can be utilized to drive a stepper motor (4 input pins, A+, A-, B+, B-). The minimum inputs to the motor driver board are 2 pins (sometimes you may need to provide one additional enable pin): 1 PWM output from ARM board, tom drive control the speed of the motor and 1 GPP output to control the direction of the motor. Typical pwm frequency is 500 – 2000 Hz, duty cycle can be 10% to 50% for example. Suppose the stepper motor is equipped with gearbox, which provides motor spin reduction ratio, typically 10:1 to 50:1. Suppose:

(2.1) gear box with 28:1 reduction ratio;

(2.2) PWM frequency is 1000 Hz;

(2.3) the motor with gear box drives wheel with OD (outer diameter) equal to 16 inch;

(2.4) motor drive is configured for ¼ micro step;

Find:

(2.5) km per hour for this design, what is miles per hour for this design?

(2.6) how much distance can the wheel travel for 10 mSec?

(2.7) in order to control the wheel motion to 10 mm, how many pulses does PWM has to produce? How much time does it need when PWM frequency is set to 1000 Hz?

3. Given below is the PWM timing diagram from ARM11 CPU data sheet, read Chapter 32, based on the timing diagram, complete a design by answering the following questions.

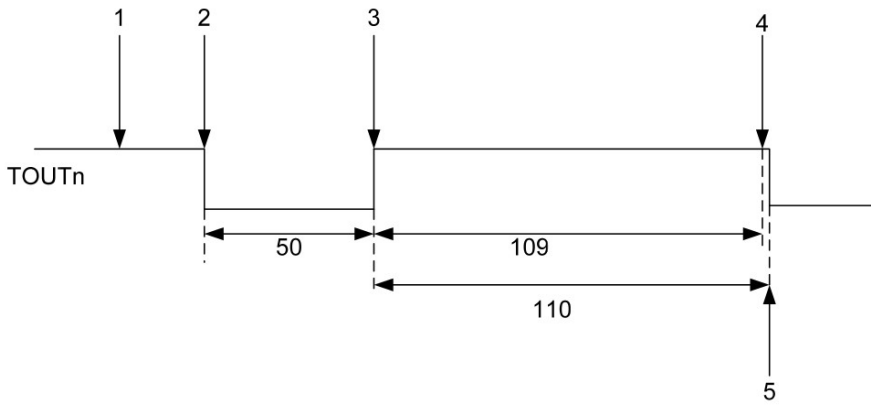

Figure 1. PWM timing diagram.

1. Initialize the TCNTBn with 159(50+109) and the TCMPBn with 109.
2. Start Timer by setting the start bit and manual update bit off.
   The TCNTBn value of 159 is loaded into the down-counter, the output is driven low.
3. When down-counter counts down to the value in the TCMPBn register 109,
   the output is changed from low to high
4. When the down-counter reaches 0, the interrupt request is generated.
5. The down-counter is automatically reloaded with TCNTBn, which restarts the cycle.

Figure 2. From CPU data sheet, Chapter 32, the PWM timing principle is described.

(3.1) suppose PCLK is 50 MHz, and we would like to realize a PWM clock design to achieve PWM frequency of 2 Khz, and 30% duty cycle;

(3.2) Find the counts number N for TCNTBn register; Find the counts number M for TCMPBn register; (see Figures below from lecture notes for the example)

(3.3) Read TCFGn from CPU data-sheet Chapter 32, pp. 1118, set pre-scaler value, so the timer input clock frequency is equal to ¼ of the PCLK, assume divider = 1 (see formula below at 1st table)

32.4.1.1 TCFG0 (Timer Configuration Register)

Register	Offset	R/W	Description	Reset Value
TCFG0	0x7F006000	R/W	Timer Configuration Register 0 that configures the two 8-bit Prescaler and DeadZone Length	0x0000_0101

Timer input clock Frequency = PCLK / ({prescaler value + 1}) / {divider value}
{prescaler value} = 1~255
{divider value} = 1, 2, 4, 8, 16, TCLK

TCFG0	Bit	R/W	Description	Initial State
Reserved	[31:24]	R	Reserved Bits	0x00
Dead zone length	[23:16]	R/W	Dead zone length	0x00
Prescaler 1	[15:8]	R/W	Prescaler 1 value for Timer 2, 3 and 4	0x01
Prescaler 0	[7:0]	R/W	Prescaler 0 value for timer 0 & 1	0x01

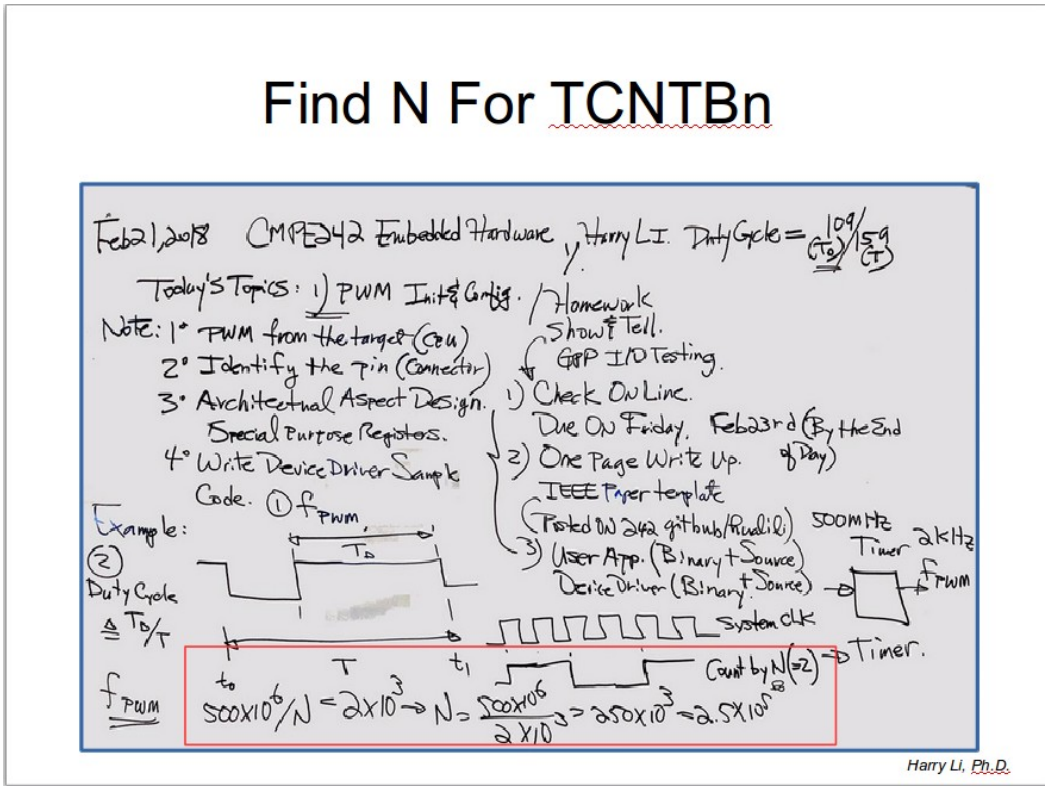

Figure 3. PWM Timing Calculation, counts N for TCNTBn.

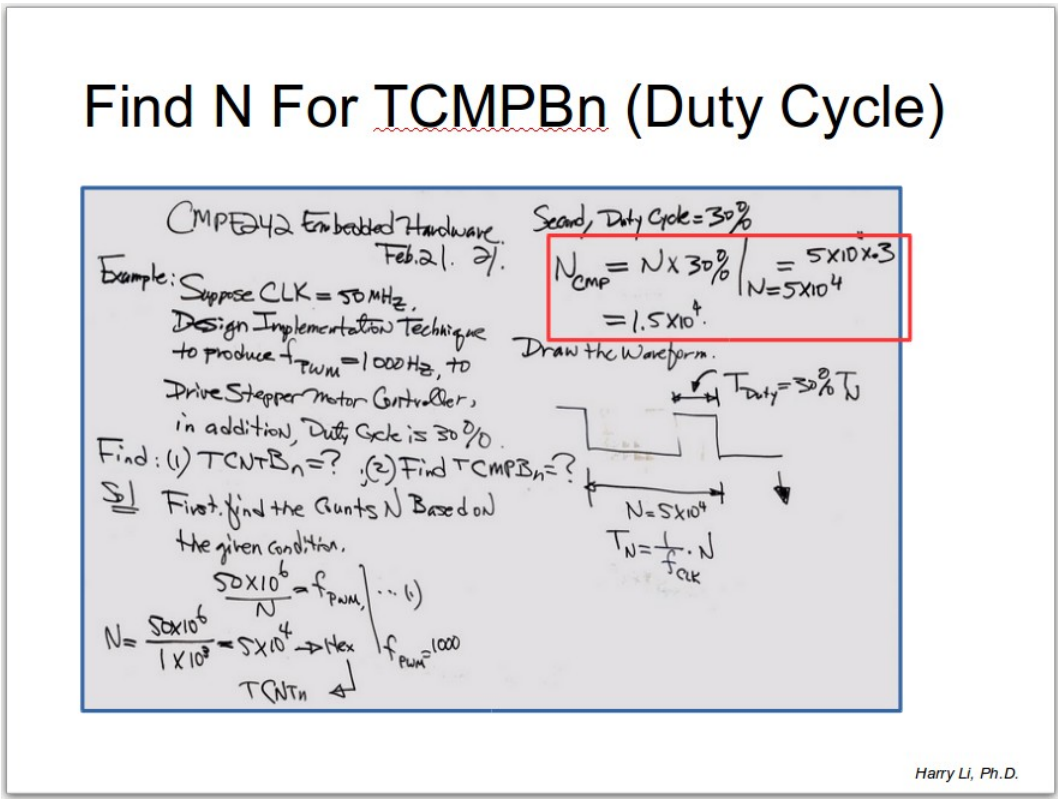

Figure 4. Calculate N for TCMPBn from lecture notes.

(End)