Handout
On Hardware of the ARM11 Development Board
HL
S12

I. Introduction

This handout is written for ARM11 hardware development kit brief description. The kit is given in Figure 1, note the CPU board is plugged into the main board and it is located on the top left of the main board. Figure 2 is the CPU board.

Figure 1. ARM11 development board.

The brief technical specification of the board is given in Table 1 below. The CPU board is shown in Figure 2 with connector information.

Table 1. Technical specification of the ARM11 board.

Item	Description
CPU	Samsung S3C6410A, run at 533Mhz ARM1176JZF-S, up to 667Mhz
RAM	256 DDR RAM(128M is option), default: 256M
Flash	128/256M/512M/1GB/2GB Nand Flash, default: 2GB MLC Nand Flash
Interface	4 x User Leds 10 pin 2.0mm space Jtag connector Reset button on board
Connector	- 2 x 60 pin 2.0mm space DIP connector - 2 x 30 pin 2.0mm space GPIO connector
Power Supply	Supply Voltage from 2.0V to 6V
Size	64 x 50 x 12mm (L x W x H)

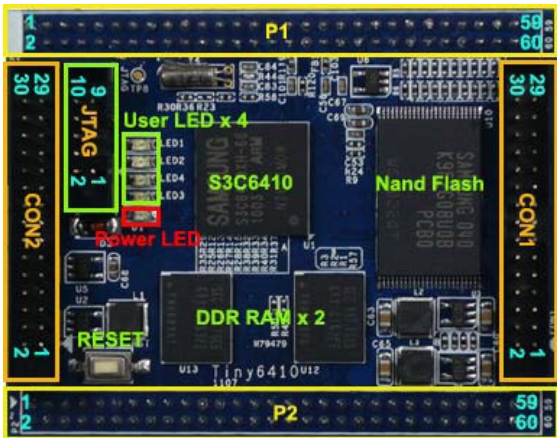


Figure 2. The CPU board.

Table 2. The CPU board connector information.

Connector	Description	Note
P1	LCD，AD，SDIO2, INT，USB，TVOUT0.	
P2	SPI1，I2C，SD Card，AC97 (I2S) etc.	
CON1	GPIO，AD，SPI0，TAVOUT1，same as those in CON6 of the main board.	
CON2	CMOS camera (same as 2440 ARM9)，GPIO.	
J-tag	Support J-link for step through operations.	

In the following 4 tables, we give detailed pin assignment for each connector.

Table 3. J tag connector.

1	VDD_IO	3.3V	2	VDD_IO	3.3V
3	TRSTn	TRSTn	4	nRESET	nRESET
5	TDI	TDI	6	TDO	TDO
7	TMS	TMS	8	GND	
9	TCK	TCK	10	GND	

Table 4. CON1 connector.

CON1.1	VDD_IO(3.3V)		CON1.2	GND	
CON1.3	GPE1		CON1.4	GPE2	
CON1.5	GPE3		CON1.6	GPE4	
CON1.7	GPM0		CON1.8	GPM1	
CON1.9	GPM2		CON1.10	GPM3	
CON1.11	GPM4		CON1.12	GPM5	
CON1.13	GPQ1		CON1.14	GPQ2	
CON1.15	GPQ3		CON1.16	GPQ4	
CON1.17	GPQ5		CON1.18	GPQ6	
CON1.19	SPICLK0		CON1.20	SPIMISO0	
CON1.21	SPICS0		CON1.22	SPIMOSI0	
CON1.23	EINT6		CON1.24	EINT9	
CON1.25	EINT11		CON1.26	EINT16	

CON1.27	EINT17		CON1.28	AIN2	
CON1.29	AIN3		CON1.30	DACOUT1	

Table 5. CON2 connector.

CON2.1	CAMSDA	I2CSDA	CON2.2	CAMSCL	I2CSCL
CON2.3	GPK2		CON2.4	CAMRSTn	
CON2.5	CAMCLK		CON2.6	CAMHREF	
CON2.7	CAMVSYNC		CON2.8	CAMPCLK	
CON2.9	CAMDATA7		CON2.10	CAMDATA6	
CON2.11	CAMDATA5		CON2.12	CAMDATA4	
CON2.13	CAMDATA3		CON2.14	CAMDATA2	
CON2.15	CAMDATA1		CON2.16	CAMDATA0	
CON2.17	VDD_IO(3.3V)		CON2.18	VDDCAM	2.4-2.8V, CMOS
CON2.19	1.8V	CMOS	CON2.20	GND	
CON2.21	GPK8		CON2.22	GPK12	
CON2.23	GPK13		CON2.24	EINT18	
CON2.25	VD0		CON2.26	VD1	
CON2.27	VD8		CON2.28	VD9	
CON2.29	VD16		CON2.30	VD17	

Table 6. P1 connector.

P1			P1		
P1.1	VDD_5V	DC-5V	P1.2	GND	
P1.3	VD23	LCD_R5/GPJ7	P1.4	VD22	LCD_R4/GPJ6
P1.5	VD21	LCD_R3/GPJ5	P1.6	VD20	LCD_R2/GPJ4
P1.7	VD19	LCD_R1/GPJ3	P1.8	VD18	LCD_R0/GPJ2
P1.9	VD15	LCD_G5/GPI15	P1.10	VD14	LCD_G4/GPI14
P1.11	VD13	LCD_G3/GPI13	P1.12	VD12	LCD_G2/GPI12
P1.13	VD11	LCD_G1/GPI11	P1.14	VD10	LCD_G0/GPI10
P1.15	VD7	LCD_B5/GPI7	P1.16	VD6	LCD_B4/GPI6
P1.17	VD5	LCD_B3/GPI5	P1.18	VD4	LCD_B2/GPI4
P1.19	VD3	LCD_B1/GPI3	P1.20	VD2	LCD_B0/GPI2
P1.21	VDEN	VDEN/GPJ10	P1.22	PWM1	PWM1/GPF15
P1.23	VSYNC	LCD /GPJ9	P1.24	HSYNC	LCD /GPJ8
P1.25	VCLK	LCD /GPJ11	P1.26	GPE0	GPE0
P1.27	VBUS	VBUS	P1.28	OTGDRV_VBUS	OTGDRV_VBUS
P1.29	OTGID	OTGID	P1.30	XEINT8	EINT8/GPN8
P1.31	OTGDM	USB Slave D-	P1.32	USBDN	USB Host D-
P1.33	OTGDP	USB Slave D+	P1.34	USBDP	USB Host D+
P1.35	TSXP	TSXP/AIN7	P1.36	TSXM	TSXM/AIN6
P1.37	TSYP	TSYP/AIN5	P1.38	TSYM	TSYM/AIN4
P1.39	AIN0	AIN0	P1.40	AIN1	AIN1
P1.41	WiFi_IO	WiFi_IO/GPP10	P1.42	WiFi_PD	WiFi_PD/GPP11
P1.43	SD1_CLK	SD1_CLK/GPH0	P1.44	SD1_CMD	SD1_CMD/GPH1
P1.45	SD1_nCD	SD1_nCD/GPN10	P1.46	SD1_nWP	SD1_nWP/GPL14
P1.47	SD_DAT0	SD1_DAT0/GPH2	P1.48	SD1_DAT1	SD1_DAT1/GPH3
P1.49	SD1_DAT2	SD1_DAT2/GPH4	P1.50	SD1_DAT3	SD1_DAT3/GPH5
P1.51	DACOUT0	H	P1.52	PWM0	PWM0/GPF14
P1.53	XEINT0	XEINT0/GPN0	P1.54	XEINT1	XEINT1/GPN1
P1.55	XEINT2	XEINT2/GPN2	P1.56	XEINT3	XEINT3/GPN3
P1.57	XEINT4	XEINT4/GPN4	P1.58	XEINT5	XEINT5/GPN5
P1.59	XEINT19	XEINT19/GPL11	P1.60	XEINT20	XEINT20/GPL12

Table 7. CON2 connector.

P2.1	OM3	SD/NAND	P2.2	OM4	SD/NAND
P2.3	M_nRESET		P2.4	VDD_RTC	RTC
P2.5	RTSn1	RTSn1/GPA7	P2.6	CTSn1	CTSn1/GPA6
P2.7	TXD0	TXD0/GPA1	P2.8	RXD0	RXD0/GPA0
P2.9	TXD1	TXD1/GPA5	P2.10	RXD1	RXD1/GPA4

P2.11	TXD2	TXD2/GPB1	P2.12	RXD2	RXD2/GPB0
P2.13	TXD3	TXD3/GPB3	P2.14	RXD3	RXD3/GPB2
P2.15	SPIMOSI	SPIMOSI/GPC6	P2.16	SPIMISO	SPIMISO/GPC4
P2.17	SPICLK	SPICLK/GPC5	P2.18	SPICS	SPICS/GPC7
P2.19	I2CSCL	I2CSCL/GPB5	P2.20	I2CSDA	I2CSDA/GPB6
P2.21	SD0_CLK	SD0_CLK/GPG0	P2.22	SD0_CMD	SD0_CMD/GPG1
P2.23	SD0_nCD	SD0_nCD/GPG6	P2.24	SD0_nWP	SD0_nWP/GPL13
P2.25	SD0_DAT0	SD0_DAT0/GPG2	P2.26	SD0_DAT1	SD0_DAT1/GPG3
P2.27	SD0_DAT2	SD0_DAT2/GPG4	P2.28	SD0_DAT3	SD0_DAT3/GPG5
P2.29	AC97_BITCLK	AC97_BITCLK/GPD0	P2.30	AC97_RSTn	AC97_RSTn/GPD1
P2.31	AC97_SYNC	AC97_SYNC/GPD2	P2.32	AC97_SDO	AC97_SDO/GPD4
P2.33	AC97_SDI	AC97_SDI/GPD3	P2.34	XEINT12	XEINT12/GPN12
P2.35	ADDR0	ADDR0	P2.36	ADDR1	ADDR1
P2.37	ADDR2	ADDR2	P2.38	ADDR3	ADDR3
P2.39	nCS1	nCS1	P2.40	XEINT7	XEINT7/GPN7
P2.41	nWAIT	nWAIT	P2.42	nESET	出)
P2.43	LnWE	LnWE	P2.44	LnOE	LnOE
P2.45	DATA0	DATA0	P2.46	DATA1	DATA1
P2.47	DATA2	DATA2	P2.48	DATA3	DATA3
P2.49	DATA4	DATA4	P2.50	DATA5	DATA5
P2.51	DATA6	DATA6	P2.52	DATA7	DATA7
P2.53	DATA8	DATA8	P2.54	DATA9	DATA9
P2.55	DATA10	DATA10	P2.56	DATA11	DATA11
P2.57	DATA12	DATA12	P2.58	DATA13	DATA13
P2.59	DATA14	DATA14	P2.60	DATA15	DATA15

II. Main Board Description

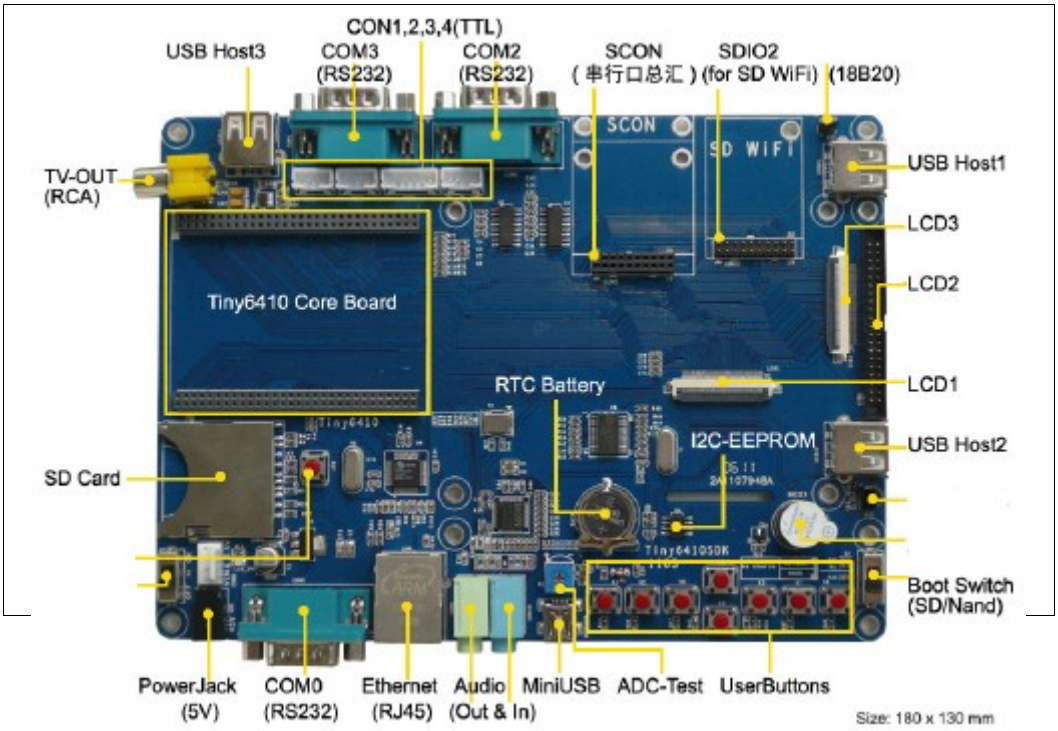


Figure 3. Main board.

Figure 4. CON0-2 on the main board.

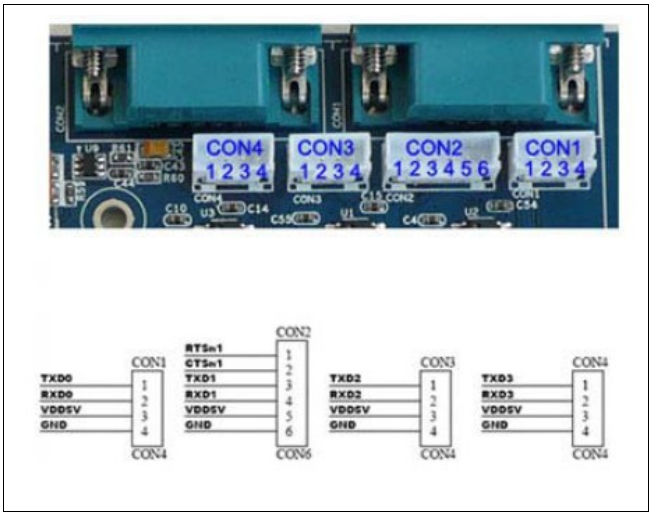


Figure 5. CON1-4 connectors.

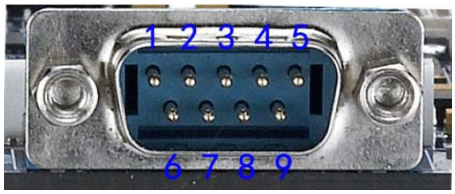


Figure 6. DB-9 Connector pin assignment.

Table 8. DB-9 connector pin assignment.

COM0		COM1		COM2		COM3	
1	NC	1	NC	1	NC	1	NC
2	RSRXD0	2	RSRXD1	2	RSRXD2	2	RSRXD3
3	RSTXD0	3	RSTXD1	3	RSTXD2	3	RSTXD3
4	NC	4	NC	4	NC	4	NC
5	GND	5	NC	5	GND	5	GND
6	NC	6	NC	6	NC	6	NC
7	NC	7	RSRTS1	7	NC	7	NC
8	NC	8	RSCTS1	8	NC	8	NC
9	NC	9	NC	9	NC	9	NC

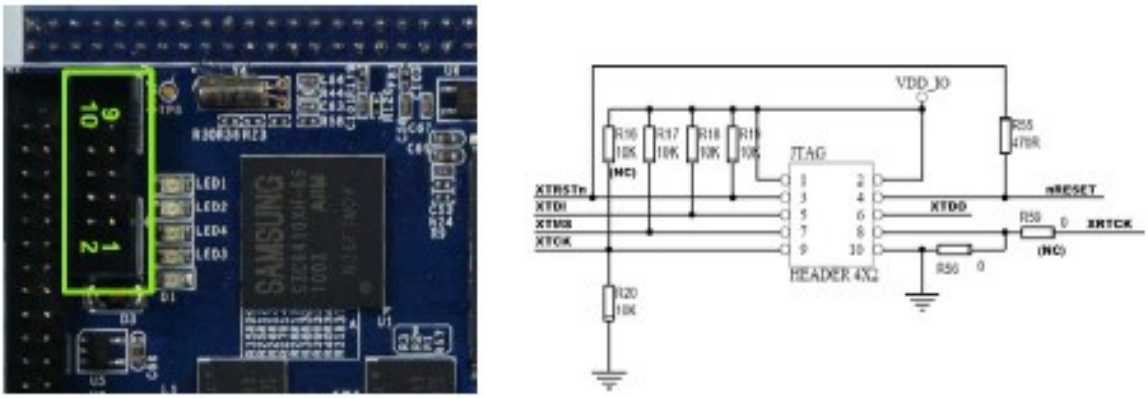


Figure 7. J tag connector.

Figure 8. ADC and external Pot.

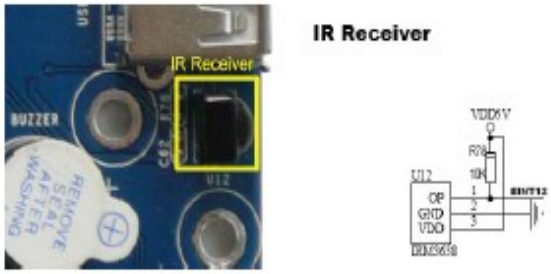
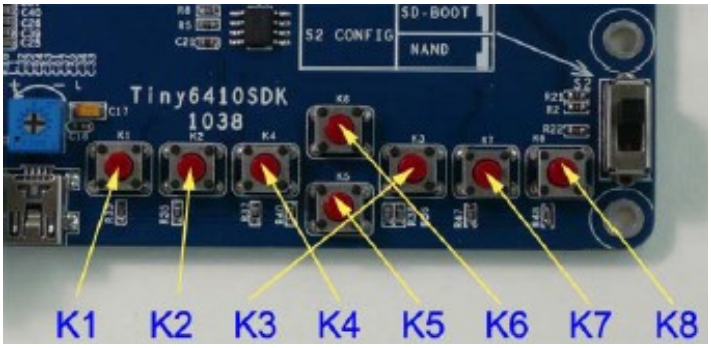


Figure 9. IrDA receiver (EINT12).



K1	K2	K4	K4	K5	K6	K7	K8
EINT0	EINT1	EINT2	EINT3	EINT4	EINT5	EINT19	EINT20
GPN0	GPN1	GPN2	GPN3	GPN4	GPN5	GPL11	GPL12

Figure 10. Push button switch and their pin configuration.

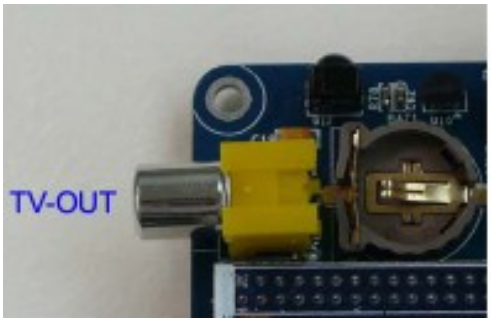


Figure 11. TV output, note TV set has to be set to CVBS mode.

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