

A Sub-60- μ A Multimodal Smart Biosensing SoC With >80-dB SNR, 35- μ A Photoplethysmography Signal Chain

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Abstract—A sub-60- μ A multimodal analog front-end and ultralow energy biosensing CMOS SoC is presented. A 35- μ A photoplethysmography (PPG) signal chain that consumes five times lower power than state of the art has been demonstrated. An SNR of >80 dBFS was achieved using circuit and system techniques that enable sub-1% analog duty cycling. Input signal-aware, on-the-fly, real-time data path adaptation algorithms implemented on an external microcontroller and synchronized by an ultralow power on-chip FSM along with a 1.3- μ W, 14-b, 1-kSPS SAR ADC further lower system energy. A programmable, asynchronous reset capacitive amplifier (PARCA) with noise efficiency factor (NEF) of 4.8 and dx/dt analog feature extractor demonstrates energy efficient electrocardiogram (ECG) capture. A wearable platform using this SoC that simultaneously captures ECG plus PPG and wirelessly transmits the heart rate using Bluetooth low energy every 2 s to a smartphone lasts for greater than five days from a 250-mAh battery.

Index Terms—Adaptive feedback, analog front end (AFE), biosensing, Bluetooth low energy (BLE), duty-cycling, electrocardiogram (ECG), energy-efficiency, multimodal, photoplethysmography (PPG).

I. INTRODUCTION

C MOS scaling and advances in microfabrication have made sensors to provide contextual awareness ubiquitous in our homes, cars, and physical selves. However, powering this sensor swarm remains a challenge. Wearable fitness devices must subsist on batteries with capacities limited to the 10–100-mAh range. Multimodal sensing of elementary quantities and subsequent fusing of data streams is often more energy efficient than directly measuring certain phenomena especially in mobile use cases. For example, in the context of health and fitness, simultaneously measuring the photoplethysmography (PPG) [1] and electrocardiogram (ECG) is a good way to measure pulse transit time, a key correlational factor in cuffless blood pressure measurement [2].

Once the sensor data are processed locally, the resulting information must be communicated either to other devices or to the cloud. Next-generation energy constrained sensor systems need to locally extract relevant information from raw data streams in order to reduce communication overhead. Integrated

Manuscript received August 14, 2016; revised October 14, 2016; accepted December 7, 2016. This paper was approved by Guest Editor Makoto Ikeda.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2016.2642205

codesign of the digital architecture along with the analog front end (AFE) is required to achieve seamless operation across domains while preserving data integrity and saving energy. While low-power microprocessors [3] and SoCs that support new energy efficient wireless protocols such as Bluetooth low energy (BLE) [4] have improved the back-end energy efficiency, the AFE often is the bottleneck to achieving overall sensor-node energy optimization. The challenge in designing mobile biosensing AFEs is the accurate, synchronous sensing of multiple biological parameters (e.g., PPG, ECG, neural potentials, and temperature) spanning multiple modalities (voltage, current, impedance, and charge) over diverse subject types and use-cases [5]–[8]—while operating from a very limited energy budget (e.g., coin cell/paper battery).

The 130-nm biosensing-integrated signal conditioner presented here demonstrates power-optimal system design that achieves approximately five times lower power than what is possible using current state-of-the-art biosensing front ends and enabling battery life in the order of a week to ten days. The SoC leverages three key techniques—aggressive duty cycling, algorithmically assisted on-the-fly signal chain adaptation, and input signal-aware adaptive sampling. Efficacies of the proposed techniques are demonstrated in the context of heart-rate monitoring (HRM) using both pulse oximetry and ECG, while consuming less than 100 μ W. Measured results show that the entire PPG signal chain achieves SNR > 80 dB while consuming 35 μ A and sampling at 100 Hz with the duty cycle of 1%.

Section II discusses challenges and tradeoffs in PPG chains. SoC architecture and the key strategies are outlined in Section III. Sections IV and V describe the design of the PPG and ECG chains, respectively. Measurement results from the SoC and platform are presented in Section VI.

II. CHALLENGES IN PHOTOPLETHYSMOGRAPHY AND CHANNEL MODEL

Pulse oximetry [1] has become the clinical standard for measuring oxygen saturation (SpO_2) in biological tissue as it is safe, convenient, and noninvasive. A reference platform [9] using a clinical grade pulse-oximeter AFE was used to collect data from human subjects from which an empirical electro-optical model of the reflective PPG system was developed (Fig. 1). An LED is pulsed at a fixed frequency—known as pulse repetition frequency (PRF)—onto the wrist. Beer–Lambert’s law [10] models the attenuation of the optical

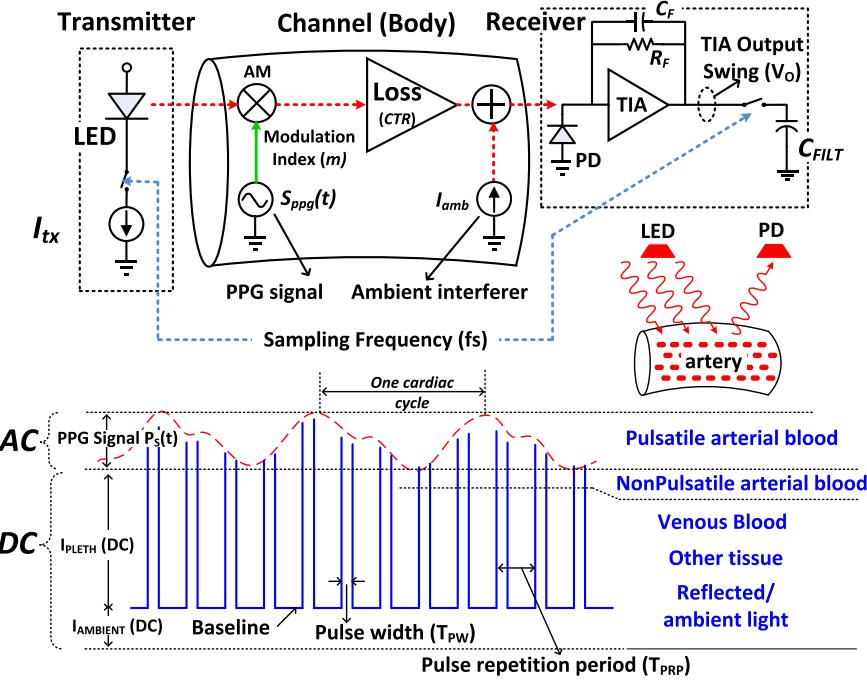


Fig. 1. Electro-optical model for PPG signal chain and PPG signal showing various components that make up the ac and dc signals.

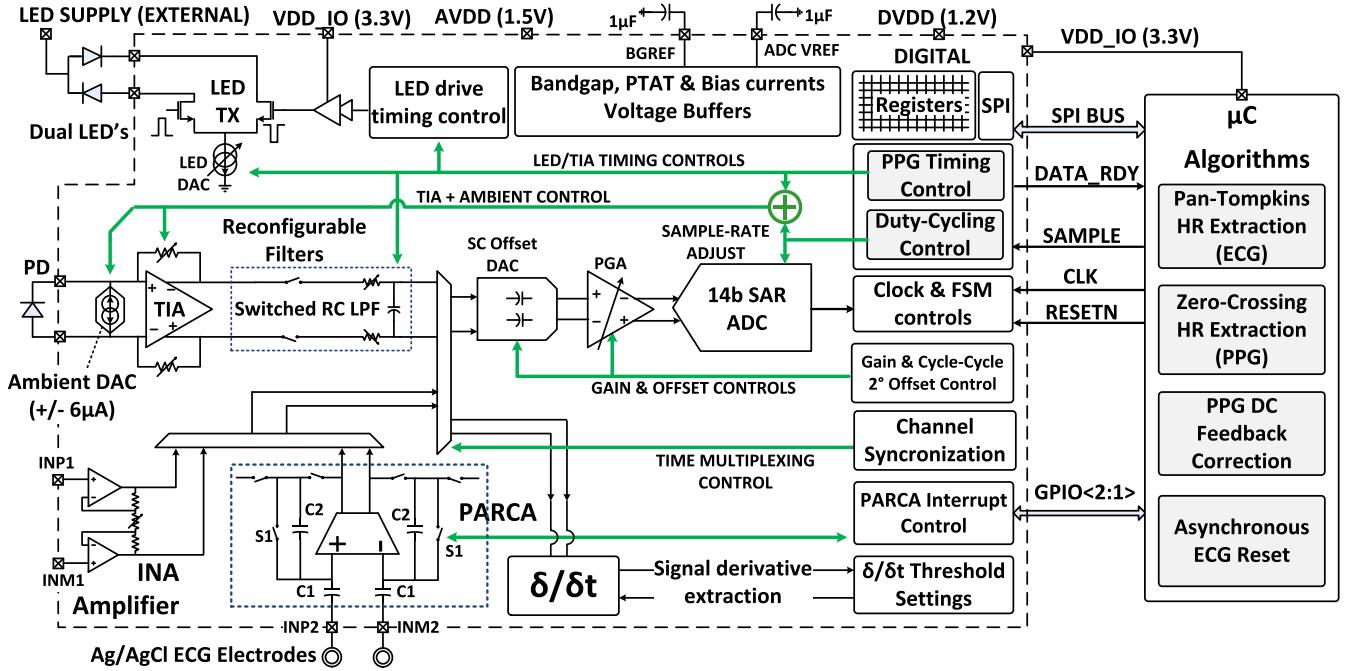


Fig. 2. SoC block diagram.

pulses as they reflect off the body and impinge on the photodiode (PD). Analogous to a pulse amplitude-modulated (PAM) wireless communication system [11], here the LED is the transmitter (TX), the body/tissue is the channel, and the PD + transimpedance amplifier (TIA) is the receiver (RX). Due to heart pulsation, the detected PPG signal exhibits a small pulsatile (i.e., ac) component riding atop a much larger nonpulsatile, fixed (i.e., dc) component. The photocurrent pulses from the PD are converted to voltage, $V_o(t)$, by a TIA and demodulated using the switched capacitor (SC) filter.

The frequency of the pulsatile (ac) component, $P_S(t)$, gives HR. The system sampling frequency, f_{PRF} , is chosen much higher than the PPG signal bandwidth, Δf , to avoid aliasing of motion-related and other artifacts that fall close to the signal band. The magnitude of the ac component, $P_S(t)$, is typically the orders of magnitude smaller than the dc component atop which it rides. The dc component includes ambient light contribution—i.e., from illumination present even when the LED is OFF and modeled as an additive current source, I_{amb} , at the PD—as well as other fixed components of biological

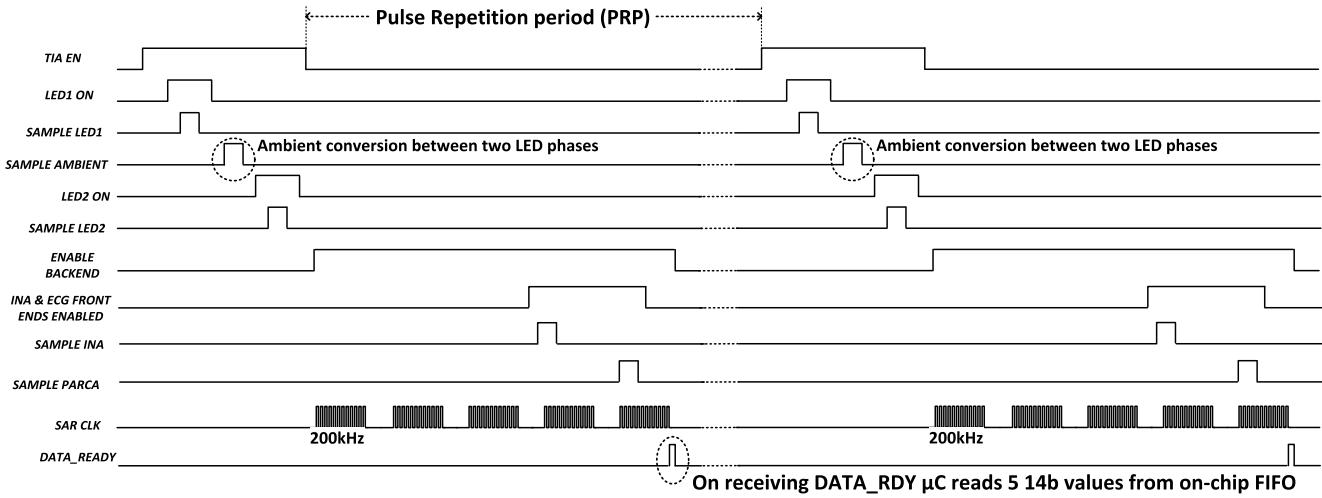


Fig. 3. Timing diagram used on the SoC.

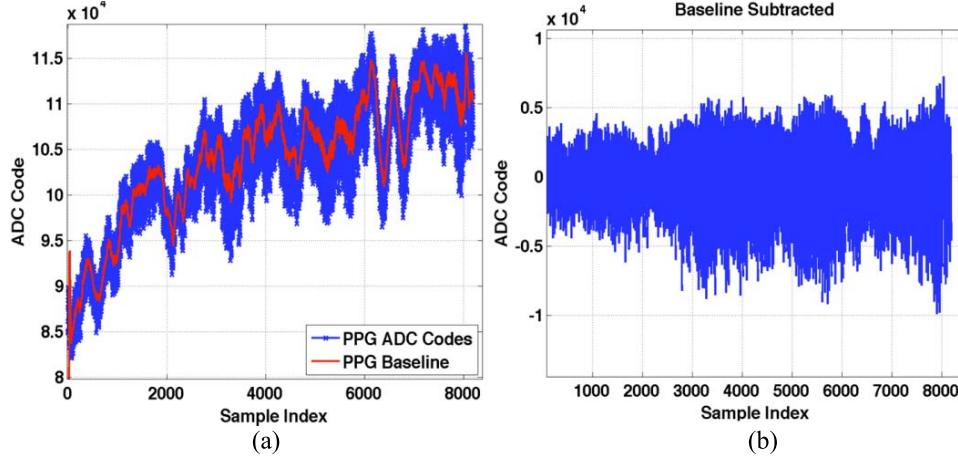


Fig. 4. (a) Raw PPG signal from subject at rest showing baseline wander. (b) PPG signal after baseline wander has been removed.

and mechanical origin, I_{PLETH} (Fig. 1). Ratio of the ac to dc component gives the *perfusion index* (PI) [12], which is correlated with the modulation index, m . The attenuation encountered by the optical pulses is modeled as the ratio of received dc photocurrent to drive current of the LED, I_{tx} , and is referred to as the current transfer ratio (*CTR*).

In-band electrical noise from the TX directly appears as injected noise in the PD photocurrent, and limits the overall PPG SNR. In the PPG system presented here, by design, the noise injected by the TX and transmit SNR (SNR_{TX}) over the PPG signal band limits the overall (TX + RX) SNR. Equation (1) gives the overall SNR of the PPG signal (SNR_{PPG}) in the transmit noise dominated system

$$\text{SNR}_{\text{PPG}} = \text{SNR}_{\text{TX}} + 20 \log_{10}(\text{PI}). \quad (1)$$

The maximum achievable receive SNR ($\text{SNR}_{\text{RX-MAX}}$) of the PPG signal at the output of the TIA with transimpedance gain R_F and sampling capacitor C_{FILT} can then be expressed as

$$\text{SNR}_{\text{RX-MAX}} \approx P_s m^2 V_o^2 \frac{D}{N} \frac{\pi}{8kT R_F \Delta f} \quad (2)$$

TABLE I
EMPIRICAL PPG MODEL PARAMETERS OBTAINED FROM
30 HUMAN SUBJECTS

Model Parameter	Value
Perfusion index related to m : ratio of AC/DC	5e-4
PPG signal bandwidth (equiv. to 30 – 300 bpm)	0.5–5 Hz
DC Responsivity/ Current Transfer Ratio (CTR)	100 nA/mA
Minimum SNR for +/- 1BPM accuracy	25dB
Minimum sampling frequency	30 Hz
Sampling in presence of motion	~ 670 Hz

where, P_s is the power of the PPG signal, $P_s(t)$, D is the duty cycle of the LED pulses, N is the excess noise factor to account for noise aliasing on the sampling capacitor, Δf is the bandwidth of interest (0.5–5 Hz), and V_o is the output swing of the TIA. The Appendix derives (2).

As $m(t) \ll 1$, for best performance, $V_o = (I_{\text{TX}} \text{CTR}) \times R_F$. Therefore, for a given channel loss (i.e., *CTR*), the maximum I_{TX} is constrained by TIA parameters R_F and V_o . Both ac ($P_s(t)$) and dc components (I_{PLETH}) are proportional to the LED intensity through the CTR—thus increasing I_{TX} to improve SNR is limited by the output swing of the TIA. Furthermore, (2) shows that increasing either LED current (I_{TX}) or duty cycle will increase RX SNR—albeit at a higher power consumption.

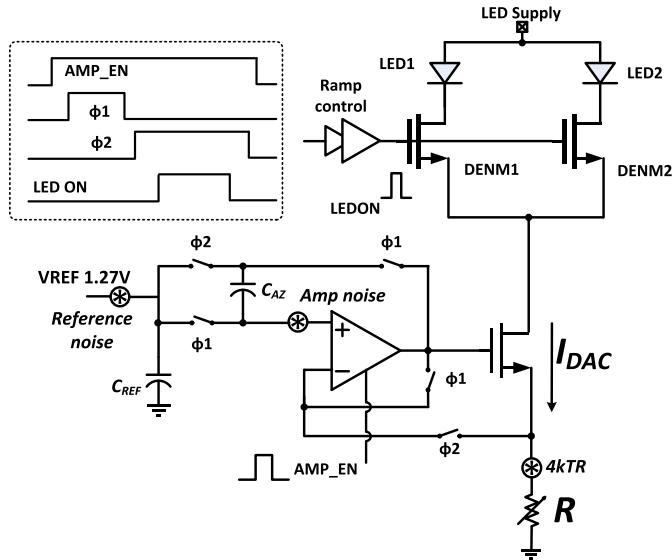


Fig. 5. Schematic of LED driver and primary noise contributors.

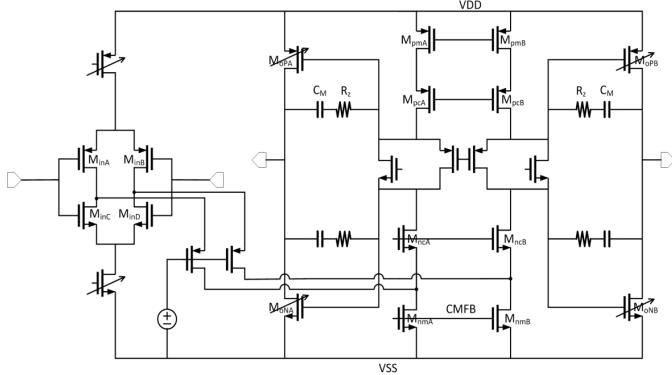


Fig. 6. Schematic of core op-amp used in TIA.

Key parameters of the empirical electro-optical model are shown in Table I. The PI can be as low as 0.05% (empirically obtained from the ~ 30 human subjects) and varies widely across subjects. A typical PI is 0.5%, and varies for a given subject based on numerous environmental factors, such as hydration, blood pressure, and so on. By adding white noise to an ideal PPG signal chain, in simulation, it was determined that an SNR of ≥ 25 dB at the input of the zero-crossing HR estimation engine [13] is necessary to achieve an HR accuracy of ± 1 beat per minute (BPM). Using a CTR of ~ 100 nA/mA, an LED current of 5 mA yields an I_{PLETH} of 500 nA. For a typical PI of 0.5% and moderate indoor ambient illumination, in order to meet the 25-dB minimum SNR for an HR accuracy of ± 1 BPM, the dynamic range (DR) of the entire PPG RX + TX chain must be > 80 dB—which must be achieved while operating from an energy budget of $< 100 \mu\text{W}$.

III. SYSTEM ARCHITECTURE AND DESIGN METHODOLOGY

Fig. 2 shows the block diagram of the 130-nm CMOS AFE, which communicates via SPI to an external μC [3] that runs multiple HR extraction algorithms and dedicated subroutines to adapt analog parameters on the fly. A 50-mA,

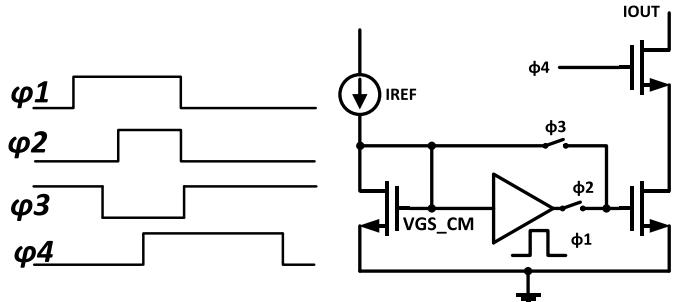


Fig. 7. Modified current mirror for fast duty cycling and control signals.

8-b LED driver capable of driving dual LEDs enables both optical HRM and SpO₂ measurement. Multimodal sensing is achieved using three separate signal-specific front ends: 1) a TIA plus SC filter for PPG; 2) a capacitive amplifier for ECG acquisition; and 3) an instrumentation amplifier (INA) for other voltage acquisition. The three separate front ends are time multiplexed into a DAC, PGA, and ADC. Fig. 3 shows the timing sequence used on the SoC for multimodal acquisition. The ambient light measurement phase (i.e., measurement of baseline, when LED is OFF) is inserted between LED phases to enable system-level-correlated double sampling (CDS). A 1.3- μW , 14-b, 75-dB SNDR at 1-kSPS segmented capacitive SAR ADC with on-chip reference buffer and mismatch calibration is chosen for its energy efficiency, memoryless nature, and ease of time multiplexing without excessive crosstalk between time-interleaved measurements.

A. Aggressive Analog Duty-Cycling for Low Energy

After initial power-up, the analog blocks, such as amplifiers, DACs, and ADC, are kept in a low quiescent current state. The bias currents are raised to their normal desired value only when that particular block is processing a signal. Controlling block-level bias current predictably enables duty-cycle-based scaling of the dc current consumption of the signal chain. For the case of the PPG chain with a PRF of 100 Hz, the time between samples is 10 ms. The LED ON time is typically in the order of 40–50 μs . The TIA is kept biased at full power (i.e., active mode) for only about 100–150 μs —thereby resulting in a significantly reduced time-averaged current consumption. Such a technique has been applied across the entire analog portion of the SoC.

B. On-the-Fly Feedback to Increase Effective Analog DR

In traditional sensor signal conditioners, a significant portion of the DR is used to accommodate interferers that do not contain relevant information. This leads to energy inefficient designs, since the DR is typically proportional to current consumption. In this paper, energy efficiency of the overall signal chain is improved by on-the-fly cancellation of those portions of the signal that do not contain relevant information. For example, Fig. 4(a) shows the measured output of the PPG chain [10] taken when a subject is at rest in a dark environment. A clear baseline drift can be observed in the dc–0.5-Hz frequency band, attributed to physiological and/or

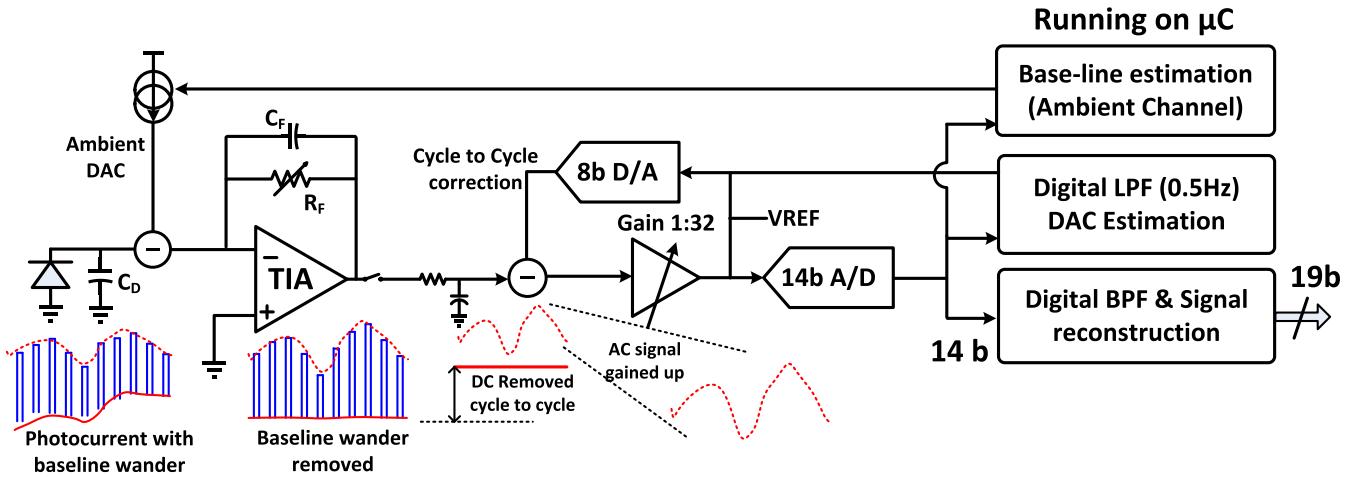
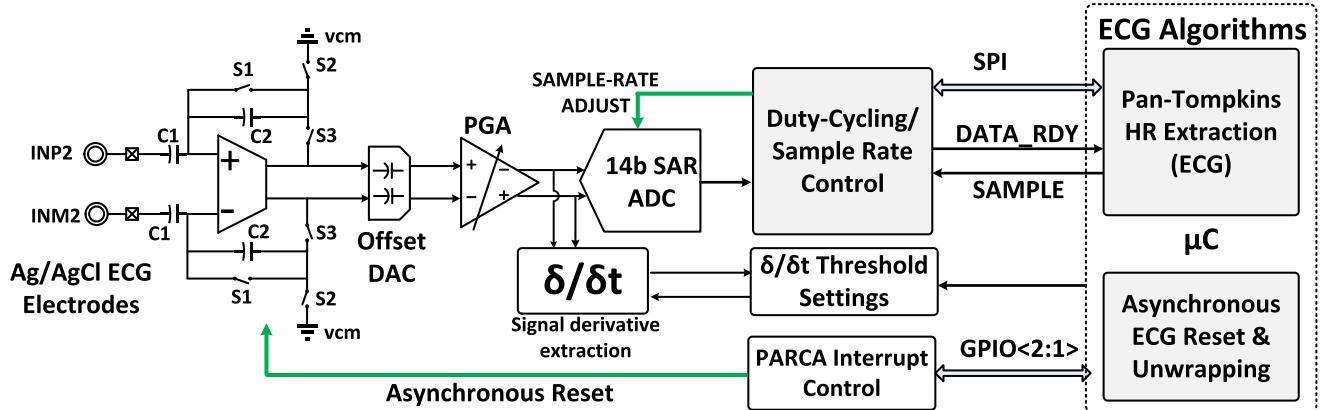


Fig. 8. PPG chain showing dc correction loops and PPG signal as it moves along the chain.

Fig. 9. ECG signal chain showing PARCA and dx/dt feature extractor.

environmental factors. The HR-containing ac message signal rides atop this baseline wander, dictating the requirement of a signal chain with >16 -b DR. In a traditional PPG system [14], wide DR ADCs (>20 b) digitize both the baseline wander as well as the message signal. Fig. 4(b) shows the same signal with baseline wander component (dc—0.5-Hz band) removed. Only a 13-b DR signal chain suffices to digitize the signal.

C. Adaptive Sampling

For most sensor signals, the *information rate* is actually much smaller than that suggested by the bandwidth [15]—i.e., the signals are *sparse* in a particular domain. The key concept is to leverage signal sparsity and design sensing or sampling schemes that allow the useful information content to be extracted in a condensed and hence energy-efficient manner. Such an example is the typical ECG signal with periodic QRS-peaks separated by long period of inactivity. For HR measurement, only the detection of the R-peaks is sufficient as described in [7]. Instead of sampling at the fixed highest Nyquist rate (f_s), accurate HR information can also be extracted if we were to sample the ECG waveform at different rates as in [7]—higher f_s during the QRS-peak and lower f_s during the interim, longer periods of inactivity. The amount of data that needs to be stored, processed, and transmitted

to the cloud (if necessary) is significantly reduced using this method—thereby improving energy efficiency.

IV. PPG SIGNAL CHAIN

A. LED Driver

Fig. 5 shows the schematic of the open drain LED driver. The LED current (I_{DAC}) is set by the 8-b code applied to the R-DAC and is given by $I_{DAC} = V_{REF}/R$, where V_{REF} is the reference voltage from the on-chip bandgap reference circuit and R is the variable R-DAC value. The primary noise contributors to the LED current noise, I_n^2 , are: 1) thermal noise from the DAC resistor; 2) voltage noise of V_{REF} ; and 3) voltage noise of the amplifier used to set the DAC current. For simplicity, assuming only thermal noise from the resistor, the SNR_{TX} is derived to be

$$\text{SNR}_{\text{TX}} = \frac{I_{\text{DAC}}}{I_n} = \sqrt{\frac{V_{\text{REF}} I_{\text{DAC}}}{4kT}} \quad (3)$$

which shows that the SNR of the TX is proportional to the reference voltage, V_{REF} . In actual practice, the voltage noise of the amplifier limits the overall SNR_{TX}. Here, the amplifier is duty cycled to reduce standby power and improve energy efficiency. This duty-cycling allows a higher peak current to be used in the amplifier, thereby reducing its flicker and thermal

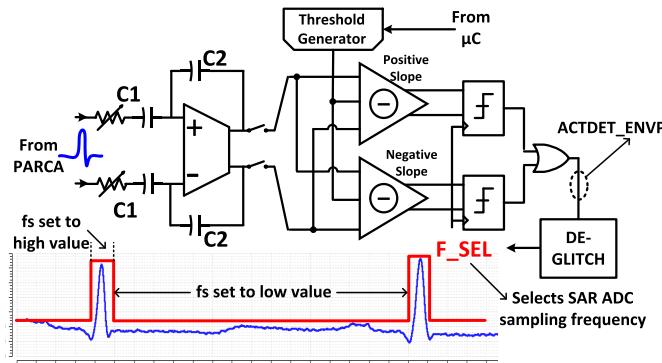
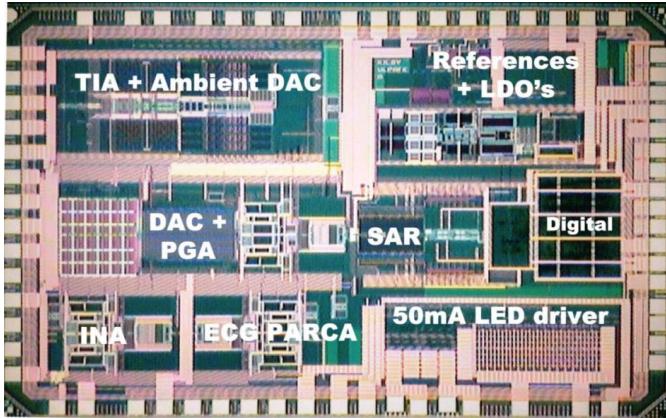
Fig. 10. dx/dt feature extractor.

Fig. 11. Die micrograph.

noise. An autozeroing scheme [16] (Fig. 5) reduces the amplifier flicker noise in the 0.5–5-Hz band, which ultimately limits SNR_{TX}. This autozeroing configuration offers the additional benefit of short LED current rise time, which is critical to sub-1% duty cycles.

B. Duty-Cycled TIA With Ambient Current Cancellation

From (2), the SNR of the RX (SNR_{RX}) is maximized when the TIA output swing is maximized. Here, as the supply voltage is 1.5 V, the full scale TIA swing is set to ± 1 V. Reduced LED ON times of $\sim 40 \mu s$ /sample to improve energy efficiency places stringent restrictions on settling time of the front-end TIA. The bandwidth (TIA_{BW}) must be large enough to accommodate the narrow pulselength T_{PW} , which is much greater than either the PPG signal bandwidth (~ 5 Hz) or the PRF (typically 100 Hz–1 kHz). The bandwidth needs to be large enough such that the output voltage settles to its final value during the LED ON time. To avoid signal-dependent, settling-induced distortion, the output must settle to a 14-b level—i.e., the TIA output rise time must be at least ten times smaller (i.e., faster) than the LED ON time. This translates to a high bandwidth and slew rate requirement on the core TIA amplifier. However, increasing bandwidth beyond the optimal amount will cause out-of-band noise to alias over at the subsequent switched-RC sampling stage. These two constraints imply that the TIA bandwidth must be carefully optimized so that the signal is not distorted and any excess noise is filtered.

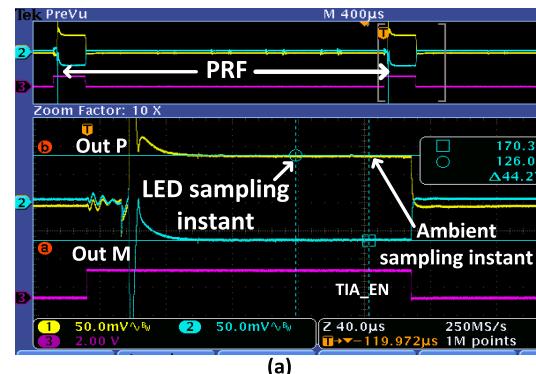


Fig. 12. (a) Waveforms showing duty-cycled TIA operation. (b) Measured average dc current consumption plotted as a function of duty cycle.

To handle the range of LED currents and operating conditions, the TIA has a 3-b on-the-fly reconfigurable gain, R_F between $10 \text{ k}\Omega$ and $2 \text{ M}\Omega$. However, changing the R_F directly impacts TIA stability and bandwidth. The transfer function for a TIA with input capacitance C_D , feedback capacitance, C_F , and op-amp with a single pole response [17] is shown in

$$Z(s) = \frac{R_F \left(\frac{A_0}{A_0+1} \right)}{s^2 \left(\frac{R_F C_F + R_F C_D}{(A_0+1)\omega_0} \right) + s \left(R_F C_F + \frac{R_F C_D + 1/\omega_0}{(1+A_0)} \right) + 1}. \quad (4)$$

Here, C_F is 8-b reconfigurable with an LSB of 0.25 pF to serve two purposes. First, fine adjustment of C_F (Figs. 1 and 8) can optimize rise time and noise performance based on duty cycle or LED ON time. Second, C_F can be optimally adjusted for a range of input capacitances to account for various PDs, cables, and so on. For a given PD, C_{PD} is fixed and C_F is varied based on selected R_F . Applying the correct C_F damps any second-order response, thereby preventing any gain peaking and ensuring stability. At low frequencies, the op-amp flicker noise is dominant and is addressed by chopping. The thermal noise from the feedback resistor, R_F , and op-amp is amplified by the noise gain ($\sim 1 + C_{PD}/C_F$) of the TIA [17] and increase at higher frequencies. The smallest ac photocurrent signal that can be seen at the TIA input is about 5 pArms, which sets the TIA noise floor.

Based on the above constraints, the core TIA amplifier must have the ability to be duty-cycled, needs to have a low input thermal and flicker noise, a large output swing

and consume as low power as possible. Fig. 6 shows a schematic of the fully differential amplifier used in the TIA. The use of pMOS and nMOS input pairs maximizes g_m , while maintaining energy efficiency through duty-cycled tail current reuse. Since the PD is connected across the TIA inputs, common-mode variations are minimal. The input transistors are biased in near-subthreshold operation to maximize their g_m/I_D and reduce thermal noise contribution. The Class-AB output maximizes output swing and is capable of driving a large output capacitance.

Duty-cycling requirements led to the use of a two-step switching scheme to transition from bias-on to active via an intermediate low-power mode. During the intermediate low-power mode, settling of the amplifier internal nodes and CMFB loop is achieved, allowing a much faster transition to the full power/active mode. This scheme allows higher peak bias currents in the core amplifier whilst active, precluding the higher noise, low BW, and PVT variations associated with sub-VT designs [18]—ensuring reliable operation across lots for volume manufacturing.

Current mirrors are very challenging to duty cycle. When reference currents are on the order of 10–100 nA, C_{GS} of the current mirror transistors limits turn-on time. Switching techniques can reduce turn-on time, but charge injected at the high impedance gate node is still the limiting factor—especially for current mirror ratios >100 . To avoid the switching induced charge injection, a switchable buffer (Fig. 7) is activated to protect the reference node (V_{GSCM}). This duty-cycled buffer replenishes the injected charge when the amplifier tail current is switching.

To address baseline wander, a $\pm 6\text{-}\mu\text{A}$, bidirectional 6-b current DAC controlled by the microcontroller (μC) is placed at the TIA input. The amount of dc correction at the TIA input is restricted by design, to limit the amount of noise injected. The TIA voltage outputs are sampled on respective switched- RC filters. The sw- RC filter shown in Fig. 2 synchronously demodulates the PAM PPG signal. The -3-dB frequency of the sw- RC filter is given by (5), where D is the duty cycle of the sampling pulse. The filter cutoff can be controlled by varying the width of the sampling pulse, in addition to R and C , to further reduce any noise aliasing that occurs at the output of the TIA

$$f_{-3\text{ dB}} = \frac{D}{2\pi \times R \times C}. \quad (5)$$

Recall that the ambient light measurement phase is inserted between LED phases to enable system-level CDS, as explained in Section III.

C. Bang-Bang DC Correction

To address PI of 0.05%–0.5%, conventional solutions [14], [19] use $\Sigma\Delta$ ADCs with DR > 20 b to digitize both the dc and ac components stored on the sw- RC filter, subsequently extracting the ac component by digital postprocessing. These wide DR ADCs are energy consuming, and being $\Sigma\Delta$ -based topologies, they cannot be very easily duty-cycled or used in a one-shot manner. In contrast, here, a 14-b low-power SAR ADC is used in a one-shot fashion

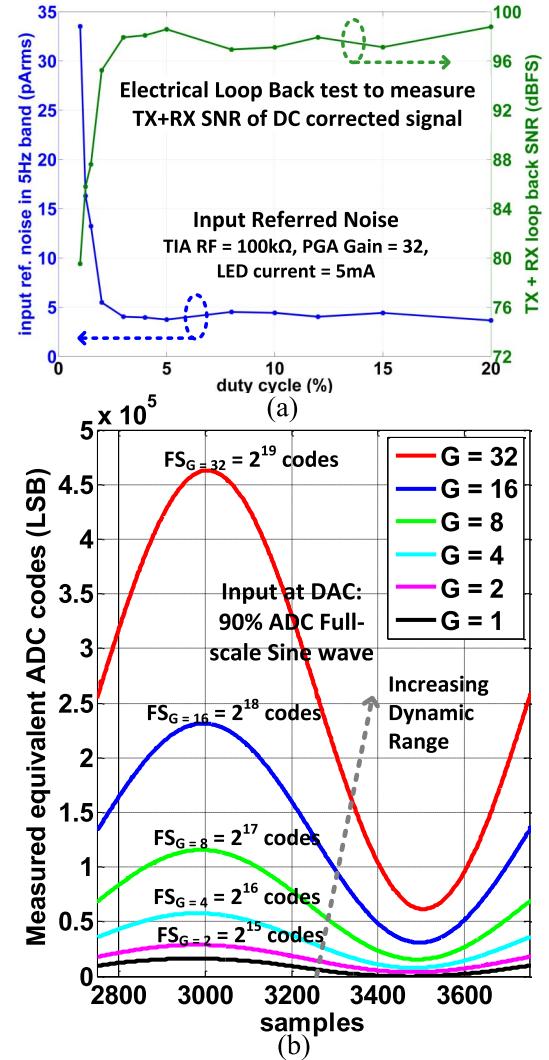


Fig. 13. (a) Loop-back SNR and noise measurements of PPG TX + RX chain. (b) Measured full-scale signal after dc correction showing effective DR of 19 b.

for cycle-to-cycle conversion. In addition to the front-end current DAC for static (or slowly varying) ambient interferer rejection [14], [20], a second 8-b SC DAC reduces the dynamic (i.e., variable from cycle to cycle) dc component (I_{PLETH}) without impacting the HR-bearing ac component. Recall that I_{PLETH} is the dc component of the photocurrent that is present only when the LED is ON (Fig. 1). The ambient interferer (or baseline wander) is the signal output from the PD—and sampled during the ambient sampling phase, Fig. 3—even in the absence of the LED light, i.e., due to environmental illumination. A digital 0.5-Hz LPF and bang-bang DAC estimation control algorithm running on the μC sets the DAC value sample by sample (Fig. 8) to ensure that the A/D output remains within programmed thresholds. Only when the ADC output crosses the

preprogrammed thresholds at a given conversion, the DAC value will be changed to bring the signal back to midrail, at the next cycle. The SC DAC has a ± 1 V correction range—therefore by choosing appropriate thresholds, the ADC inputs

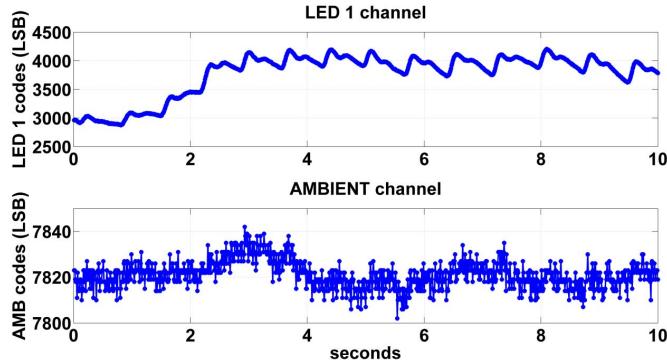


Fig. 14. Measured biological PPG and ambient channel data.

will never saturate. Since the DAC correction is only applied at sporadic instants and does not represent a periodic update, it does not present interference in the signal band of interest (0.5–5 Hz) [21]. The PGA between the DAC and the ADC further amplifies the residual ac component prior to A/D conversion. Fig. 8 shows the PPG signal as it moves through the signal chain. Due to the presence of the variable gain PGA (G_{PGA}), the overall equivalent system DR is given by

$$\text{Equivalent DR} = 14 \text{ bit} + \log_2(G_{\text{PGA}}). \quad (6)$$

This bang–bang dc correction followed by a PGA allows the PPG signal chain to achieve an effective DR of 19 b (at the PGA gain of 32) with a 14-b ADC at the core. The key is to gain effective DR in the relevant signal domain (i.e., ac component) by removing unwanted portions (i.e., dc component) that dictated a high DR to begin with.

V. ASYNCHRONOUS RESET CAPACITIVE AMPLIFIER FOR ECG WITH FEATURE EXTRACTION

Capacitive ECG amplifiers have been shown to achieve much smaller noise efficiency factors (NEFs) than INA-based front ends [6], [8] while inherently providing a high input impedance. However, all capacitive ECG amplifiers require a dc path to set the bias of the amplifier inputs, which often takes the form of a large resistance. Pseudoresistors [22] and SC techniques [6] are commonly used to set the dc bias, and any noise introduced is mitigated by design. However, there is the continuous dc leakage at the high-impedance node of the amplifier that cannot be compensated. Mismatch in leakage between the positive and negative paths degrades the common mode rejection (CMR) of the front end and contributes to offset. Therefore, eliminating the dc biasing path from a capacitive amplifier would provide the lowest noise and the best CMR possible.

In this paper, a fully differential programmable asynchronous capacitive reset amplifier (PARCA) [23] has been designed for ECG detection (Fig. 9). The PARCA solves the leakage of the dc bias path by eliminating the dc bias path altogether. The fully differential PARCA with maximum capacitive gain of 200 ($=C_1/C_2$) senses ECG directly from electrodes without any off-chip dc block. The gain stage and Class-AB output stage are separated so that the amplifier can drive the large capacitance presented by the back-end SC offset

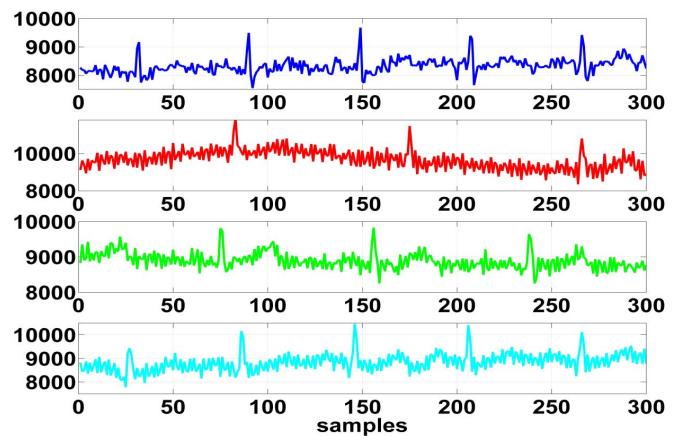


Fig. 15. ECG data from four human subjects acquired using the PARCA (y-axes units: codes).

DAC. During amplification phase, switches S1 and S2 are open while S3 remains closed. Once the A/D output crosses programmed thresholds, the μ C closes switches S1 and S2 asynchronously, setting the dc bias at the summing node and ensuring linear operation. The reset pulsewidth is significantly smaller than typical sampling durations (~ 1 kHz) so as not to have any noticeable effect on the acquired signal. The absence of sampling precludes kT/C noise associated with traditional SC AFEs. In contrast to analog dc servo loops [8], the reset instance can be algorithmically modified by the μ C to prevent switching-induced charge injection at the high-Z nodes. Compensation of PVT variations present in pseudoresistor schemes is avoided here by varying reset thresholds.

An analog feature extractor (Fig. 10) computes the slope of the ECG signal by differentiation, and adapts the ADC sampling frequency on-the-fly for accurate R-peak detection. The goal is to reduce system energy overhead in the back-end data processing and wireless transmission, as described in [7]. The dx/dt analog feature extractor is similar to [7] but with few key differences. Unlike [7] where a fully analog loop is used to generate the adaptive threshold, here the thresholds are digital. Due to the slow tracking nature of the dx/dt loop, updates to the digital threshold are relatively infrequent, which makes the digital implementation more energy efficient. A digital threshold control method also gives more flexibility and robustness for volume manufacturing.

It was empirically determined that in order to reliably determine the onset of the QRS complex, the minimum detectable slope of the ECG signal is ~ 25 mV/s. The clock frequency of the SC differentiator [24] is 2 kHz, which yields a maximum latency of 500 μ s—insignificant compared with a typical QRS-pulse of width 20–30 ms. Since the dx/dt feature extractor is not duty-cycled, most transistors in its core amplifiers and comparators are operated in the subthreshold region to lower power. A deglitch filter smooths the outputs from the positive and negative comparators and provides a frequency select signal (F_SEL) to the ADC sampling engine. Another key difference compared with [7] is that here, the deglitcher attack/release windows are digitally programmable, making it more amenable for application across subject populations.

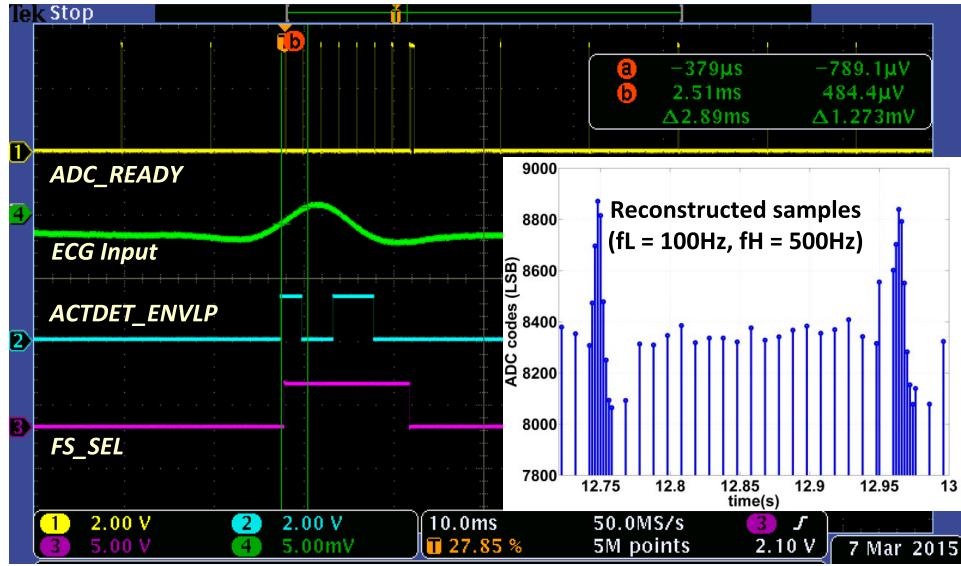


Fig. 16. Adaptive sampling and reconstructed samples in time domain.

TABLE II
MEASURED CURRENT BREAKDOWN OF ASIC

Block (PRF = 100Hz, Duty Cycle= 1%, LED on-time = 100 μ s)	Supply Voltage (V)	Current (μ A)	Power (μ W)
TIA + Ambient DAC	1.5	3	4.5
Instrumentation Amplifier		10.19	15.3
PARCA		2.5	3.75
SC Filter , Offset/ Pleth DAC, PGA		12.19	18.3
ADC (analog + digital logic)		1.09	1.3
References, dx/dt		7	10.5
Digital	1.2	12.5	15
3.3V supply for LED driver	3.3	10	33
Total current/ power consumption of PPG RX Chain Only		35.78 μ A	$\sim 50\mu$ W
ASIC current/ power during HRM using PPG only (TX + full RX chain with 1 LED + 1 ambient)		45.81 μ A	$\sim 83\mu$ W
Full Chip current/ power with 5 channels enabled (2 LED channels + 1 ambient + ECG + 1 voltage)		59 μ A	$\sim 102\mu$ W

VI. MEASUREMENT RESULTS

Fig. 11 shows the micrograph of the AFE SoC that was fabricated in a 130-nm CMOS process.

A. PPG Chain

Fig. 12(a) shows the internal TIA_EN control signal and the fully differential outputs of the PPG TIA for a test input. Only a single LED cycle and the ambient cycle are included for HRM measurement. The TIA_EN signal repeats every pulse repetition period and turns on the TIA to full active mode. No duty-cycling-induced settling artifacts are observed on the TIA outputs at the LED and ambient sampling instants [Fig. 12(a)]. Fig. 12(b) plots the measured average dc current of the TIA as a function of duty cycle, for a fixed PRF of 100 Hz.

The combined (TX + RX) SNR is obtained by performing an electrical loop-back test. The LED current is 5 mA at a PRF of 100 Hz. Gain (R_F) of the TIA is 100 k Ω and the PGA gain is 32 V/V. Fig. 13(a) plots the loop back SNR (dBFS) and the

0.5–5-Hz integrated noise of the entire PPG chain referred back to the TIA input in pArms. At duty cycles >2%, the entire PPG chain (TX + RX) SNR is >95 dBFS—sufficient to resolve HR in the cases where PI \sim 0.05%. Fig. 13(b) plots the PPG chain output with the bang–bang cycle to cycle dc correction loop running when a full scale (± 1 VPP) signal is seen at the output of the TIA. This shows the increase of effective DR from 14 to 19 b.

Finally, Fig. 14 shows the recorded raw 14-b biological PPG signal from the LED and ambient channels at the output of the SoC, recoded from a human subject. No postprocessing by the μ C has been performed, though active cycle-to-cycle dc correction (at the SC offset DAC) as well as ambient/baseline wander cancellation using the input current DAC are being applied. The LED channel signal has a peak to peak of ~ 350 ADC codes, while the ambient signal shows a variation of ± 5 A/D codes—more than 25 dB needed for a variation of ± 1 -BPM accuracy.

B. ECG Chain

Fig. 15 shows a snapshot of the raw 14-b ECG records obtained from four different human subjects captured using Ag/AgCl electrodes at the wrist and using the PARCA. The sampling frequency is 100 Hz and PARCA gain is 200. The PARCA consumes 2.5 μ A with an NEF of 4.8.

Fig. 16 shows the waveform capture when an emulated ECG signal was input to the dx/dt feature extractor. The ACTDET_ENVLP toggles at both the rising part and falling part of the QRS waveform, when the derivative exceeds the set thresholds. By appropriately adjusting the attack and release windows digitally to account for the QRS inflection point, FS_SEL selects one of two frequencies to the ADC. When FS_SEL goes high, the ADC switches to a higher sampling rate—500 Hz—and when it goes back low, the ADC switches to the lower sampling rate—i.e., 100 Hz (Fig. 16). Fig. 16 also plots the reconstructed digital ECG record at the μ C output.

TABLE III
COMPARISON OF THIS PAPER AGAINST OTHER REPORTED PPG RX CHAINS

	This Work	Winokur et al. 2015 [26]	TI AFE4404 2015 [14]	Glaros et al. 2013 [25]	Tavakoli et al., 2010 [18]
IC-only current for optical HRM (μ A)	45.81	216.6	210	-	-
# of LED channels	2	2	3	2	2
Static/Ambient Removal (μ A)	12	100	6	Yes, not spec.	
Power for FOM calculation (μ W)	83	425	440	528	200
Effective Max DR (dBFS)	97	91*	99	68	90**
PPG FOM (pJ/sample)	14	140	60	2572	77
Multi-parameter sensing capability	Yes	No	No	No	No
NEF of ECG front-end	4.8	N/A	N/A	N/A	N/A
Process (μ m)	0.13	0.18	-	0.35	1.5
Supply Voltage (V)	1.5	1.8	2	3.3	5
* 52dB + 39(IR channel), **60dB based on claim 0.1% PI + 30dB for HR detection					

C. ASIC Current Consumption and Comparison

Table II gives the measured current breakdown of the various blocks in the ASIC with a PRF of 100 Hz and duty cycle of 1%. Table II also tabulates the AFE current and power consumption in various operation modes. For optical HRM, only a single LED measurement and ambient measurement are necessary. The PPG RX chain consumes only about 35 μ A, while still providing overall SNR > 80 dB for duty-cycles of >1%. A figure-of-merit (FOM) is derived based on the Walden-FOM commonly used for ADCs [25]. The ENOB of the PPG chain is calculated from the loop-back SNR that includes both TX + RX components and the f_s is set as the PRF. Table III summarizes the key parameters and the FOM for PPG chains (normalized to a 100-Hz PRF) found in the literature [14], [18], [26], [27]. This paper shows the lowest reported FOM till date—more than five times lower than prior work.

D. Multimodal Measurements in a Wireless, Wearable Form Factor

Fig. 17 shows the 3.4 cm \times 4 cm wireless multimodal acquisition platform built using the AFE and powered by a 3.7 V, 250-mAHr, Li-Polymer rechargeable battery. Multichannel PPG and ECG data acquired from the AFE by the μ C [3] are wirelessly transmitted via BLE [4] to a smartphone every 2 s for postprocessing.

Fig. 18(a) shows the concurrently captured PPG and ECG signals using the wireless platform. An optimized version

of the Pan–Tompkins algorithm [28] is used to extract HR from the ECG data stream. HR is extracted from the PPG data stream using a zero-crossing detection algorithm. The wirelessly transmitted HR value from the ECG and PPG channels recorded on the smartphone [Fig. 18(b)] tracks to within ± 5 BPM.

The platform lasts approximately five days on a single charge of the 250-mAHr battery with simultaneous concurrent ECG and PPG acquisition (100 Hz), adaptive μ C algorithms enabled, and BLE transmission every 2 s, but without peripherals, such as display, real-time clock, and so on enabled. The platform lasts greater than ten days when used for a period of 4 h/day and streaming HR every 2 s (to emulate an exercise scenario).

VII. CONCLUSION

In conclusion, this paper has demonstrated that by using novel circuit and system techniques, it is possible to reduce the energy consumption needed for accurate signal acquisition, such that the AFE is no longer the bottleneck in achieving overall energy efficiency in wireless sensor nodes. Circuit techniques that enable aggressive analog duty cycling without performance degradation are presented, and cycle-to-cycle feedback to extend overall DR has been demonstrated. In the context of biosensing for health and fitness applications, these circuit and algorithmic techniques, have resulted in the lowest FOM—14.3 pJ/sample—PPG signal chain reported.

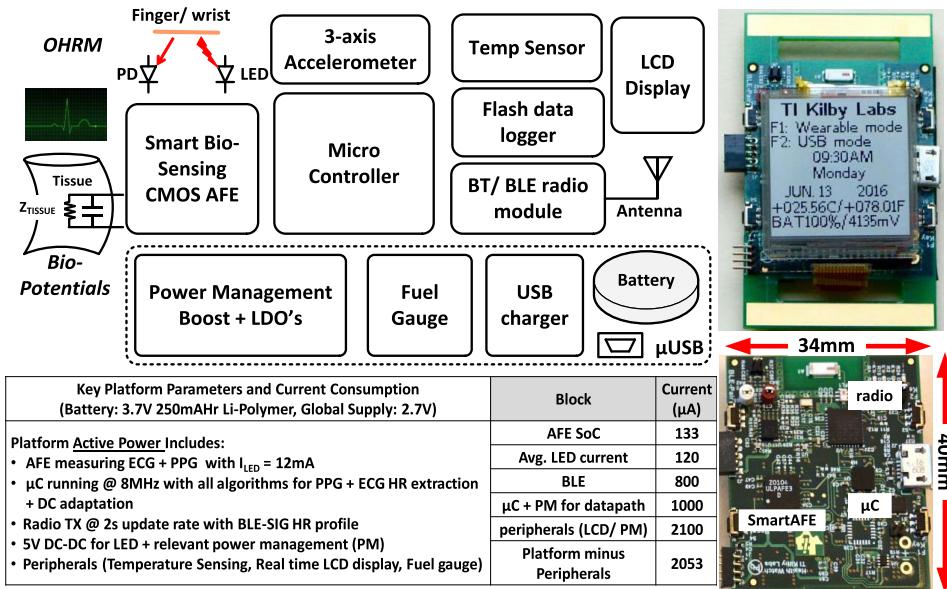
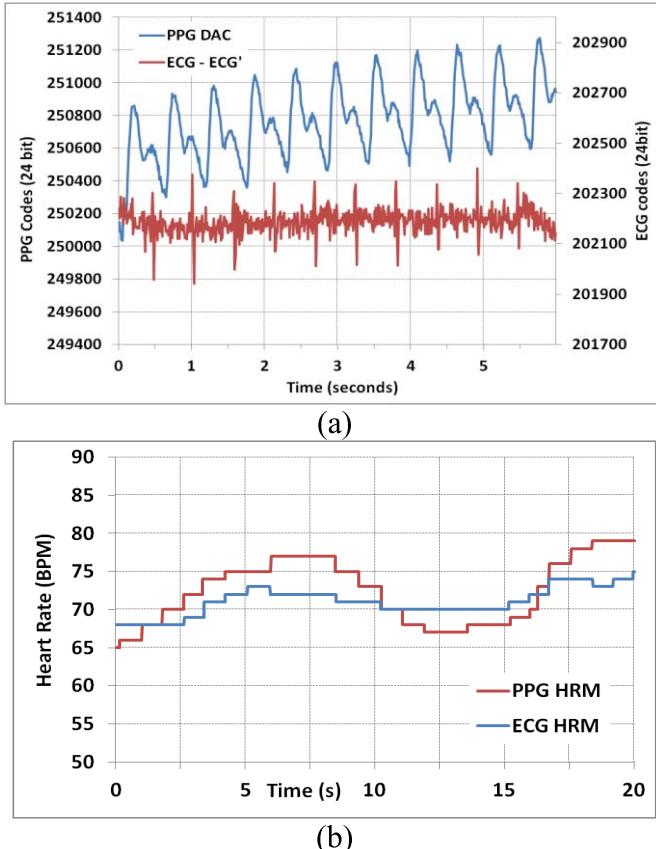


Fig. 17. Wireless multimodal platform.

Fig. 18. (a) Concurrently captured ECG and PPG signals using the platform.
(b) Transmitted HR from PPG and ECG chains.

APPENDIX

In this appendix, (2) is derived for the PPG system shown in Fig. 1.

- f_{PRF} is the sampling frequency of the PPG system (set by PRF).
- D is the duty cycle.
- Δf is the PPG signal bandwidth (normally 0.5–5 Hz for humans).

This gives the available settling time for the TIA output (on sampling capacitor C_{FILT}) = D/f_{PRF} .

N is the number of time constants of settling required. f_{TIA} is the –3-dB bandwidth of the TIA.

Normally the TIA –3-dB bandwidth is set such that the settling period corresponds to an integer multiple (N) time constants. This implies

$$\frac{N}{2\pi f_{\text{TIA}}} = \frac{D}{f_{\text{PRF}}}. \quad (7)$$

For the purposes of this derivation, the TIA output noise power spectral density (PSD) is assumed to be $4kT R_F$ (units: V^2/Hz).

The effects of C_F and C_D on the TIA transfer function (4) and TIA noise have been ignored in this qualitative analysis of the factors that limit SNR of a PPG chain.

For a TIA with –3-dB bandwidth f_{TIA} , the number of folding/aliasing zones due to the sampling operation is given by

$$\frac{f_{\text{TIA}}}{f_{\text{PRF}}/2} = \frac{N}{\pi D}.$$

Therefore, the PSD of the sampled noise on the sampling capacitor is given by

$$\sigma^2 \sim 8kTR \frac{N}{\pi D} \quad (\text{Units: } \text{V}^2/\text{Hz}). \quad (8)$$

The total integrated in-band noise in the PPG signal bandwidth (Δf) is therefore

$$\sigma_{\Delta f}^2 = 8kTR \frac{N}{\pi D} \Delta f \quad (\text{Units: } \text{V}^2). \quad (9)$$

- P_S is the normalized signal power in the transmitted PPG signal.
- V_O is the maximum output voltage swing of the TIA.
- m is the PPG PI.

The maximum received PPG signal power can therefore be given by

$$S_{\text{PPG_RX}(\text{MAX})} \approx P_S m^2 V_0^2 \text{ (Units: V}^2\text{).} \quad (10)$$

Hence, the maximum limit of the SNR of the received PPG signal is proportional to

$$\text{SNR}_{\text{PPG_RX}(\text{MAX})} \propto \frac{P_S m^2 V_0^2 \pi}{8kT R_F \left(\frac{N}{D}\right) \Delta f}. \quad (11)$$

ACKNOWLEDGMENT

The authors would like to thank Dr. R. Aggarwal, A. Rappoport, H. Shah, C. Rush, Dr. K. Nagaraj, A. Das, Dr. J. Park, N. Elahi, U. Shirsalkar, S. V. V Prasad, M. Koosha, W. Culpepper, R. Chatterjee, B. Sharma, and Dr. P. Aroul for help at various stages in the project. They would also like to thank Dr. G. Burra for insightful discussions and P. Emerson and K. Soundarapandian for supporting the project.

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