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A Low-Power CMOS Front-End for Photoplethysmographic Signal Acquisition With Robust DC Photocurrent Rejection

Alex K. Y. Wong, Kong-Pang Pun, *Member, IEEE*, Yuan-Ting Zhang, *Fellow, IEEE*, and Ka Nang Leung, *Senior Member, IEEE*

***Abstract*—A micro-power CMOS front-end, consisting of a transimpedance amplifier (TIA) and an ultralow cutoff frequency lowpass filter for the acquisition of photoplethysmographic signal (PPG) is presented. Robust dc photocurrent rejection for the pulsed signal source is achieved through a sample-and-hold stage in the feed-forward signal path and an error amplifier in the feedback path. Ultra-low cutoff frequency of the filter is achieved with a proposed technique that incorporates a pair of current-steering transistors that increases the effective filter capacitance. The design was realized in a 0.35-μm CMOS technology. It consumes 600 μW at 2.5 V, rejects dc photocurrent ranged from 100 nA to 53.6 μA, and achieves lower-band and upper-band − 3-dB cutoff frequencies of 0.46 and 2.8 Hz, respectively.**

***Index Terms*—Current-steering, dc photocurrent rejection, photoplethysmogram, pulsed light source, ultralow cutoff frequency filter.**

I. Introduction

NEAR-INFRARED (NIR) sensing has been used widely in the acquisition of biomedical signals. It is typically performed by detecting a current that is proportional to the amount of transmitted or reflected photons being sensed by the photodiode. This current is then converted to a voltage signal by a transimpedance amplifier (TIA) for further signal processing. The signal being acquired by this method is termed photoplethysmogram (PPG), which can be used together with electrocardiogram (ECG) to estimate blood pressure (BP) [1]. Generally, PPG alone is used for heart rate measurement.

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This acquired current signal consists of an ac signal of interest (i_d) and a dc component (I_D) related to the following: 1) physiological condition of individual, which varies from person to person; 2) duty cycle of the light-emitted diode (LED), when it is pulsed to reduce power consumption; and 3) the power consumption of the LED in continuous-time operation. The ratio of i_d/I_D is given by the following equation:

$$\left(\frac{i_d}{I_D}\right)_{R,IR} \approx \log\left(\frac{\Gamma_{\rm sys}}{\Gamma_{\rm dias}}\right)_{R,IR} \quad (1)$$

where R and IR stands for red and infrared, and $\Gamma_{\rm sys}$ and $\Gamma_{\rm dias}$ represent the systolic and diastolic values for the bulk tissue absorption coefficient, respectively. i_d/I_D is typically in the range of 0.001 to 0.015 [2]. Since i_d is in the range of 50 nA to few hundred nanoamperes, I_D is in the range of 1 μA to 120 μA. Therefore, the TIA in the PPG analog front-end (AFE) must reject this dc component to avoid degradation of the dynamic range (DR).

The dc rejection problem is further complicated when the light source (i.e., the NIR LED) is pulsed for reducing power consumption [3], [4]. As shown in Fig. 1, the average level of a pulsed signal is not the same as its continuous-time version, and depends on the duty cycle of the pulsating scheme. A proper dc rejection should reject the latter rather than the former for maximizing the DR of the system. In the past, ac coupling circuit using diode connected transistor (pseudo-resistor) [4], [5], dc current rejection for cochlea implant [6], correlated double sampling (CDS) [7], [8], and capacitance multiplication [9] have been implemented to address this issue. Nonetheless, each technique has its own strengths and drawbacks, such as poor linearity and process dependency in pseudo resistor due to inadequate headroom and variation in saturation current ($I_{\rm S}$) [5], inappropriate operating frequency for slow varying physiological signal [6], susceptibility to aliasing and folding in CDS [10], and severe loading problem in the feedback source follower when ultralow frequency operation is desired [9], [11].

Another challenge for the monolithic integration of PPG front-end is the realization of lowpass filter with very low cutoff frequency due to the slow varying physiological signals (0.5–4 beats per second), and the removal of motion artifact and charge leakage from sample-and-hold, which are in the range of 10–100 Hz. However realization of filter with very low cutoff frequency requires a very large *RC* time constant, which implies that bulky passive components are to be integrated in silicon. Alternatively, low power consumption stems from the

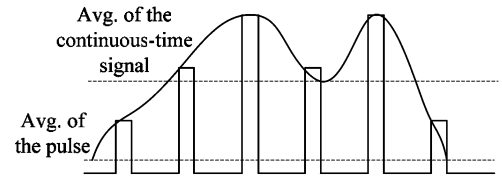

Fig. 1. Difference between the average levels of a continuous signal and its pulsed version.

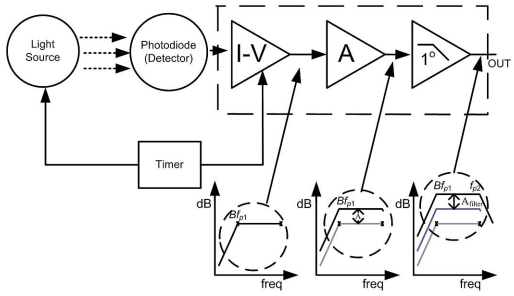

Fig. 2. Proposed sensor architecture, which consists of a closed-loop TIA, amplifier and current-steering lowpass filter (CS-LPF).

portable nature of the sensor system and the constraints of the power source. This is especially crucial for future design when integrated wireless transmitters are used.

Consequently, this paper presents a robust mixed-signal system that addresses the aforementioned issues, which includes a new dc photocurrent rejection TIA [12] and fully-integrated ultralow cutoff frequency filter using current-steering technique (CS-LPF). In Section II, the system architecture is presented. A review on dc photocurrent rejection circuit [13] is included in Section III. The proposed circuit structure, the CS-LPF and the measurement results are presented in Sections IV–VII, respectively.

II. System Architecture

The system that performs PPG signal processing, together with its frequency response, is implemented in Fig. 2. It consists of a light source, a detector (photodiode), a TIA, which is based on [13], a post amplifier, a current-steering lowpass filter (CS-LPF) [14] and a timing circuit. The system being realized is enclosed within the dotted line. The transfer function is

$$A(s) = A_{\text{stopband}} \cdot A_{\text{amp}} \cdot A_{\text{filter}} \cdot \frac{1 + \frac{s}{\omega_{p1}}}{\left(1 + \frac{s}{B\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{2}$$

Equation (2) exhibits a bandpass filter response, where B is the product of component parameters and ω_{p1} is the lower-band $f_{-3\text{ dB}}$ formed by the feedback element within the dc rejection loop of the TIA, both of which will be explained later. On the other hand, ω_{p2} is the upper band $f_{-3\text{ dB}}$ and is controlled by the cutoff frequency of the CS-LPF. The gain of the system is the product of the gains of the post-amplifier, filter and the stopband, which is generated by the TIA as well.

The source is a NIR LED that is pulsed by the timing circuit to emit a train of light pulse of wavelength at 850-nm. All components have been implemented on chip except for the LED, photodiode (PD), timing circuit and the off-chip capacitors. Power saving can be achieved by time-multiplexing the switching of the LED, which is pulsed for 1 ms for every 10 ms. The input signal is a current pulse being acquired through the PD with ac amplitude of 200–300 nA that sits on top of a 50 –60 μA pulse with f_{sample} of 100 Hz and duty cycle of 10%.

The pulse height is set at 50–60 μA since experiments with discrete circuits have shown that dc photocurrent of most subjects spans a range of 60– 80 μA when physiological signal is acquired through the PD, with the LED fully on. Therefore, with a 10% duty cycle, the actual amount of dc current generated by the PD is about 6–8 μA. This signal is then converted to voltage in the TIA. To detect the average of this pulsating signal accurately, this pulsed PPG signal is then sampled and held inside the system, together with the feedback mechanism, which will be elaborated in the next section. Finally, filtering is applied to this quantized signal through the CS-LPF and continuous-time signal can be recovered for further processing.

Various techniques have been adopted to overcome the low cutoff frequency problem mentioned previously. Continuous-time technique such as $G_m - C$ [15] is preferred to discrete-time technique such as switched-opamp switched-capacitor (SO-SC) [16], [17] due to the complex clock circuitry of the SO-SC circuits and the nature of the biomedical signal, which has small amplitude that is susceptible to leakage current. Moreover, the implementation of $G_m - C$ filter involves complex architecture [15] and to compensate for its inaccuracy, capacitance multiplication is also required, which might create loading problem for the transconductor if not designed carefully [15]. Alternatively, the current-steering technique (CST), works by varying the gate voltage of the transistor pair to steer away a certain amount of current to ground from the feedback capacitors in the active-RC filters. As a result, the cutoff frequency of the filter can be adjusted. The advantage is multi-faceted. First, the CST is very simple compared to the SC or $G_m - C$ technique because it does not require the presence of a clock signal or complex biquad/ladder structure. Thus, there is no switching noise problem, which is usually associated with an SC filter, or stability problem, which is associated with the $G_m - C$ structure. Second, the use of large capacitors can be avoided owing to the increasing effective capacitance due to current steering. Third, the process and temperature variations can be compensated by varying the gate voltage. Although the current-steering transistors, which act as linear resistors, might exhibit nonlinear behavior, the problem can be minimized by carefully controlling the aspect ratio of the transistors. Accordingly, the advantages far outweigh the drawbacks. Therefore, the CST technique will be further investigated in later section.

The advantage of the overall system is multi-fold. First, unlike the pseudo-resistor ac coupling circuit, the input signal experiences less distortion with this TIA configuration. Second, the average level of the incoming signal, which is a current pulse, can be computed more accurately through the sample-and-hold in the feedback loop circuitry, and current-to-voltage conversion can also be performed simultaneously. Third, since the NIR LED consumes the most power, it needs to be pulsed to reduce power consumption. Inevitably, the duty cycle and sampling frequency would affect the accuracy of peak detection algorithm later on for BP estimation [3]. Henceforth, this

architecture provides flexibility in the duty cycle and sampling frequency selection to optimize for power consumption and BP computation accuracy because it can reject variable amount of the dc current. Finally, an ultralow cutoff frequency filter is realized with a very simple current-steering transistor pair and active-RC filter. Thus, with proper building block arrangement, the DR of the overall system is not hampered. The off-chip capacitor for compensation in the error amplifier (EA) also provides low enough cutoff frequency required to preserve the original signal, as explained in later section.

III. Optical Preamplifier With DC Photocurrent Rejection

As mentioned in previous section, there is a need for the development of a current-to-voltage converter that can regulate voltage output coming from a pulsed current source [3], [4]. A TIA contained in a feedback loop with error amplifier is necessary, such as the one shown in [13]. This circuit performs the following functions: 1) current-to-voltage conversion through R_f of the TIA, 2) dc photocurrent rejection as the error voltage is sensed by EA to determine the amount of dc current to be sunk from the PD through $M_{\rm ctl}$, 3) highpass filtering through the feedback mechanism, which will be explained here, and 4) regulation of dc output voltage to $V_{\rm ref}$ through the use of feedback loop.

The characteristics of the ambient photocurrent rejection circuit can be characterized by

$$\frac{v_{\rm out}}{i_s}(s) = \frac{R_f}{1+L(s)} \tag{3}$$

where the loop gain $L(s)$ is given by

$$L(s) = R_f \cdot A_{\rm err}(s) \cdot g_{\rm mctl} \approx R_f \frac{A_{\rm dc}}{1+\frac{s}{\omega_{p1}}} g_{\rm mctl} \tag{4}$$

by assuming the gain of the error amplifier $A_{\rm err}(s)$, has a dominant-pole response where $A_{\rm dc} = g_{\rm mEA} R_{02}$ and $g_{\rm mEA}$ is the transconductance and R_{02} is the output impedance of the EA, respectively. $\omega_{p1} = 1/(R_{02}C_m)$ is the dominant-pole frequency, where C_m is the compensation capacitor of the EA. By substituting (4) in (3), the resulting closed-loop response of the preamplifier with ambient photocurrent rejection is

$$\frac{v_{\rm out}}{i_s}(s) = \frac{R_f}{1+L(s)} \approx \frac{1}{A_{\rm dc} g_{\rm mctl}} \times \frac{1+\frac{s}{\omega_{p1}}}{1+\frac{s}{R_f A_{\rm dc} \omega_{p1} g_{\rm mctl}}} \tag{5}$$

where R_f is the passband gain of the TIA, $A_{\rm stopband} = 1/(A_{\rm dc} g_{\rm mctl})$ and $g_{\rm mctl}$ is the transconductance of $M_{\rm ctl}$. Assuming $R_f A_{\rm dc}\, \omega_{p1} \gg 1$, the preamplifier exhibits a highpass response with the following lower-band $f_{-3\ {\rm dB}}$ (ω_{HP}):

$$\omega_{HP} = B\omega_{p1} = R_f A_{\rm dc} \omega_{p1} g_{\rm mctl}. \tag{6}$$

It can be seen that this circuit works fine for high-frequency operation. Yet, two problems emerge if this circuit is used for low-frequency operation with a pulsed input: 1) only very small amount of current can be sunk with a reduced ω_{HP}, as seen in (6) unless very large time constant is implemented in the EA for bandwidth extension to reject moderate amount of dc photocurrent; and 2) incorrect average detection for the pulsating signal. The first point is relevant because the sunk current is in the μA range regardless of the operating frequencies. However, this is not an issue since an external compensation capacitor will be used. Conversely, as illustrated in Fig. 3, for an input current pulse (i_d) whose output is a voltage pulse, as the output is integrated by the EA, the offset of the voltage pulse $(V_{\rm dd}/2)$ becomes the average. Consequently, output from $A_{\rm err}(s)$ is incorrect and the dc current (I_D) generated from $M_{\rm ctl}$ is inaccurate. This is acceptable if signal is not being further processed. Otherwise, reduction of DR occurs due to insufficient output swing.

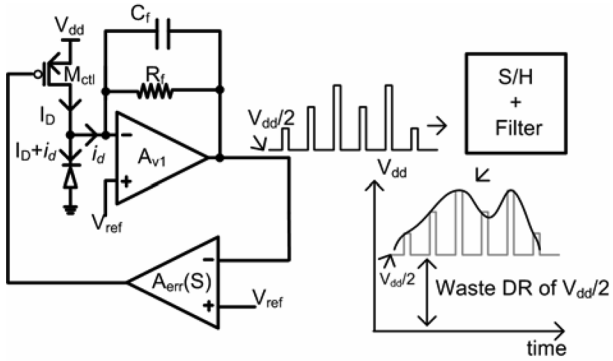

Fig. 3. Illustration of how the circuit in [13] results in DR reduction.

IV. Proposed DC Photocurrent Rejection With Sample-and-Hold in Feedback

To circumvent the incorrect average detection issue, a different topology in the feedback loop is proposed, which is shown in Fig. 4. Since the average of continuous-time signal is desired but not the pulsed signal, a sample-and-hold (S/H) circuit is inserted between the TIA and the EA. As the current pulses are being converted to voltage pulses through the TIA, instead of integrating the pulsated signal to detect its average, the EA integrates the sampled-and-held version of the signal such that the average of the signal can be detected accurately. Thus, robust dc photocurrent rejection for a pulsed light source and accurate detection of dc level of pulsed voltage can be achieved by the addition of an S/H circuit, which is simply a CMOS switch with a holding capacitor $(C_{\rm H})$. To illustrate the point, the system in Fig. 2 is designed and implemented in a 0.35-μm CMOS technology. The supply voltage is 2.5 V. Except for the compensation capacitor (C_m) in the EA, which is 220 nF, and $C_{\rm H}$ in S/H circuit, which is 10 nF, all circuit components have been realized on chip. The EA and the TIA opamps are two-stage amplifiers in [18]. The use of slightly larger capacitor is to reduce the charge injection such that a larger switch can be used to ensure loop stability. The size of these capacitors can be scaled down substantially in future development by using smaller switch size and leakage current cancellation technique [17]. The gain is R_f and a 2-KΩ resistor is used. The circuit achieves a highpass cutoff frequency of 1 Hz and adequate amount of attenuation according to (5) and (6). The main parameters are summarized in Table I.

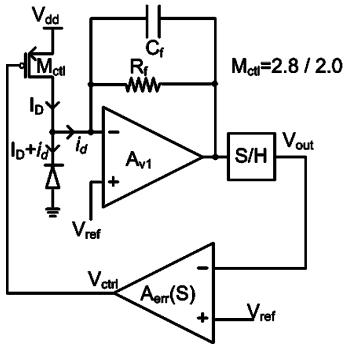

Fig. 4. DC photocurrent rejection TIA with sample-and-hold in feedback loop.

TABLE I
MAIN PARAMETERS FOR PROPOSED TIA

Frequency cutoff	1 Hz (lower) 50 Hz (upper)
(W/L) M_{ctl}	2.8-μm / 2.0-μm
C_H & C_m	10 nF & 220 nF
f_{sample}	100 Hz
TIA gain setting	2KΩ dB
LED duty cycle	10%

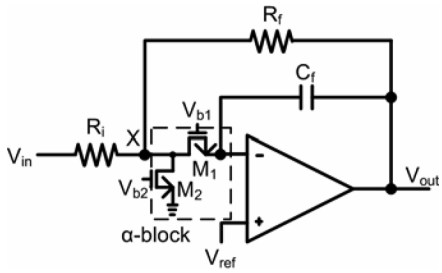

Fig. 5. Schematic of CS-LPF.

V. CURRENT-STEERING LOWPASS FILTER

To achieve a filter architecture with ultralow cutoff frequency, robust performance and compactness, active-RC implementation is preferred. The R-MOSFET-C filter from [19] satisfies this requirement for adaptation. This fully-differential filter structure is part of the 22-KHz fifth-order Bessel filter for audio applications. This filter not only exhibits low distortion due to the current-steering transistor inside the feedback loop, but it also has the potential to be realized as a tunable filter with current division network [20], and evolves to an ultralow cutoff frequency filter [14] based on the pair of current-steering transistors.

The architecture of the first order current-steering lowpass filter (CS-LPF) is given in Fig. 5 and the α-block is enclosed within the dotted line. In here, the virtual ground at the negative input of the opamp has been extended to node X since the α-block is enclosed within a loop. For our application, only single-ended version is sufficient. The new transfer function is given by the following:

$$A(s) = \frac{-R_F/R_i}{1 + \frac{SR_FC}{\alpha}} \tag{7}$$

where $\alpha \leq 1$. Therefore, the $-$3-dB frequency is

TABLE II
MAIN PARAMETERS OF CS-LPF

Frequency cutoff	1.8-Hz – 62-Hz
(W/L) $M_{1,2}$	0.8-μm / 80-μm
C_f	38-pF
R_i and R_f (KΩ)	7 (R_i), 11.2, 73.2, and 184.8
Effective capacitance	48.6-nF - 1.68-μF
Gain setting	3.5, 17.5 and 28.4 dB
Power consumption	95-μW

$$f = \frac{\alpha}{2\pi R_f C}. \tag{8}$$

The α-block consists of two transistors, with M1 operates at the triode region and acts as linear resistor, and M2 in saturation region. Both of them have identical aspect ratios but different gate voltages to steer current (shown in Fig. 5). α is given by:

$$\alpha = \frac{I_{d1}}{I_{d2}} = \frac{K\left[(V_{gs1} - V_t)\cdot V_{ds1} - \frac{V_{ds1}^2}{2}\right]}{0.5K\left(V_{gs2} - V_t\right)^2}$$

since node X is at virtual ground ($V_{ds1} \sim 0$), α becomes:

$$\sqrt{\alpha} = \sqrt{\frac{I_{d1}}{I_{d2}}} = \frac{\sqrt{2V_{ds1}\left(V_{gs1} - V_t\right)}}{V_{gs2} - V_t}. \tag{9}$$

From (9), frequency tuning is achieved by varying the gate voltage, which in turn steers the currents that flow from the capacitors to virtual grounds, and with this adjustment of gate voltage, the compensation for different process and temperature variations is also achieved. By directing less ac current to the feedback capacitor, the effective capacitance seen at the noninverting terminal of the opamp is increased by a factor of α. With this technique, a 38-pF capacitor and 17.5-dB gain is implemented to achieve a cutoff frequency from 62 to 1.8 Hz (and even lower)—an effective capacitive reduction from 500 times to 12 500 times! Nonetheless, for the α-block to work properly, its location must precede a high impedance node such that the ac current would only flow to ground or the feedback capacitor. Again, the opamp is a two-stage configuration in [18].

The performance of this filter is crucial in alleviating the size of the holding capacitor in the TIA and is very robust at different supply voltages, as shown in the experimental section. One shortcoming with this filter is its active-RC configuration, which necessitates a buffer in its opamp to provide proper loading for the next stage. In addition, there is linearity problem as the current-steering transistors exhibit nonlinearity because the voltages vary at the gate and source as cutoff frequency decreases. Nonetheless, care should be taken in choosing V_{b1}, V_{b2}, the cutoff frequency and the aspect ratio of transistors so that the transistors do not operate in the nonlinear region of the $I_{ds} - V_{\rm dsat}$ characteristic curve. The main parameters for CS-LPF are summarized in Table II.

VI. MEASUREMENT RESULTS

In this section, the implementation details, measurement and physiological test results from the CS-LPF and the overall system are presented. To verify the functionality and the performance of the CS-LPF, the filter has been integrated as part

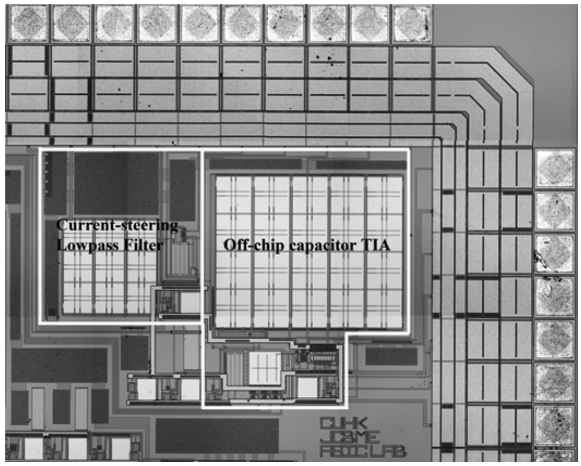

Fig. 6. Micrograph of PPG analog front-end.

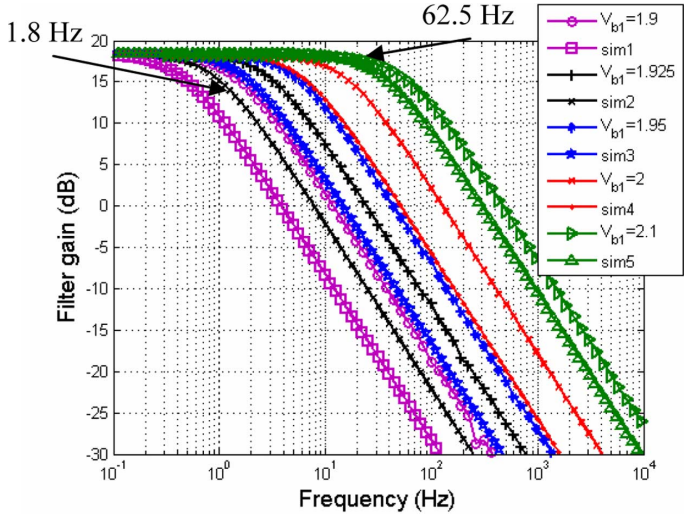

Fig. 7. Simulated and experimental frequency responses of the CS-LPF are plotted together.

of the PPG signal acquisition system. First, the measurement results of the filter are given, and then followed by those of the overall system. The micrograph of the PPG AFE is shown in Fig. 6. The size of the PPG AFE is about 805 μm by 530 μm. It operates from a 2.5-V supply and consumes about 0.6 mW of power. $V_{\rm ref}$ is set at $V_{\rm dd}/2 = 1.25$-V for all measurement settings.

A. Current-steering Lowpass Filter

The measured frequency responses of the CS-LPF with different values of V_{b1} ($V_{b2} = 0.74V$) are plotted together with its simulated frequency response in Fig. 7. The current-steering transistors would work as long as M_2 is in saturation and $f_{-3\ \rm dB}$ can be varied through adjusting V_{b1} of M_1. The $f_{-3\ \rm dB}$ varies from 1.8 Hz to 62 Hz with V_{b1} varies from 1.9 V to 2.1 V. The robustness of the current-steering transistors is clearly seen by the adjustability of $f_{-3\ \rm dB}$. From Fig. 7, the measurement result deviates significantly from the simulated result (from 1.64 times to 3.34 times) as cutoff frequency decreases. Possibly, at lower cutoff frequency, the operation of M_1 of the current-steering transistors is highly nonlinear and might be in cutoff due to very small V_{gs}. Since M_1 is located between the virtual ground and the inverting input of opamp, any small variation in its source voltage can change r_{ds} a lot from simulation.

Fig. 8 shows the total harmonic distortion (THD) of the filter with $f_{-3\ \rm dB}$ of 5.67 Hz and 100 $mV_{\rm in-pp}$ to be -47.1-dB. This is enough for our application.

The distortion as a function of cutoff frequency is plotted in Fig. 9. The THD and spurious-free dynamic range (SFDR) are identical at low cutoff frequency and deviate at higher frequency ($f_{-3\ \rm dB} > 3.1$Hz). This is due to nonlinearity at low cutoff frequency, which results in strong influence of harmonic tone, whereas there are multiple tones of distortion at very low magnitude compared to the fundamental due to less distortion at a higher cutoff frequency. The worst-case distortion is at $f_{-3\ \rm dB}$ of 1.57 Hz, which is about 30.1 dB. Also, Fig. 9 shows the SFDR of the filter with $f_{-3\ \rm dB}$ of 3.1, 5.67, and 16.4 Hz ($100mV_{\rm in-pp}$) to be -33-dB, -47.1-dB, and -50.6-dB, respectively, which are satisfactory for our application.

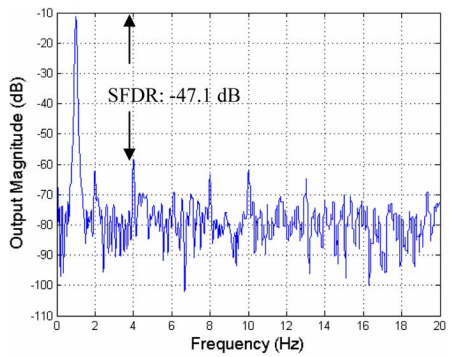

Fig. 8. FFT of a 1 Hz signal with $V_{\rm pp} = 100mV$ and $f_{-3\ \rm dB}$ of 5.67 Hz. SFDR is about -47.1 dB.

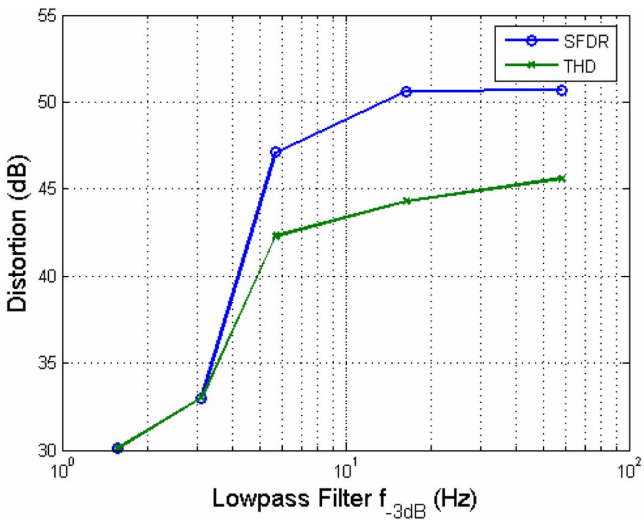

Fig. 9. Distortion versus $f_{-3\ \rm dB}$ of CS-LPF. The distortion is worst at low frequency due to nonlinearity of M_1.

The increase in the integrated input noise corresponds to an increase in bandwidth, which is illustrated in Fig. 10. These figures are reasonable since this filter is located at the back-end and the input signal power to the filter is much larger than the

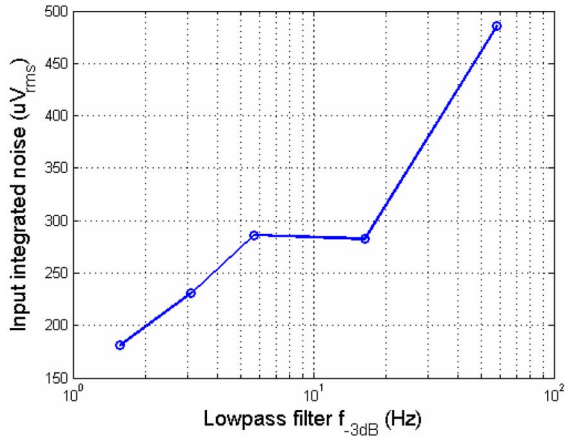

Fig. 10. Input integrated noise of filter versus $f_{-3\ \mathrm{dB}}$. The noise is higher at larger $f_{-3\ \mathrm{dB}}$ due to wide bandwidth.

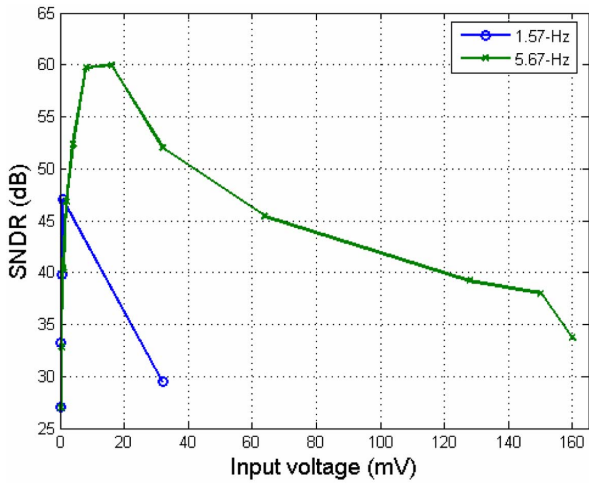

Fig. 11. For a 3% THD, the DRs of the filter are about 54.5 and 46.6 dB for $f_{-3\ \mathrm{dB}}$ of 5.67 and 1.57 Hz, respectively.

integrated noise. From Fig. 10, the values of input integrated noise are 235.9, 285.9, and 282.7 $\mu\mathrm{V_{rms}}$ for $f_{-3\ \mathrm{dB}}$ of 3.1, 5.67, and 16.4 Hz, respectively. Next, the signal-to-noise plus distortion ratio (SNDR) as a function of the input voltage is plotted in Fig. 11 to illustrate DR. With $f_{-3\ \mathrm{dB}}$ of 5.67 and 1.57 Hz, the DRs of the filter are about 54.5 and 46.6 dB, respectively.

B. Overall System

The sinusoidal current source $(I_D + i_d)$ is generated by feeding a voltage source to the circuit in Fig. 12. The frequency response of the entire system with different I_D is shown in Fig. 13. The circuit achieves 47.7-dB attenuation for a photocurrent of 20 μA with an lower-band and upper-band $f_{-3\ \mathrm{dB}}$ of around 0.46 and 2.8 Hz. The range of dc photocurrent that can be sunk effectively while maintaining the desired frequency response is from 0.1 to 53 μA. Theoretically, the larger the amount of dc photocurrent, the higher the attenuation, but practically this might cause transistors in the error amplifier to go into linear region, which leads to reduced attenuation at larger I_D.

The dc attenuation with respect to passband gain as a function of input dc photocurrent is shown in Fig. 14. An in-band

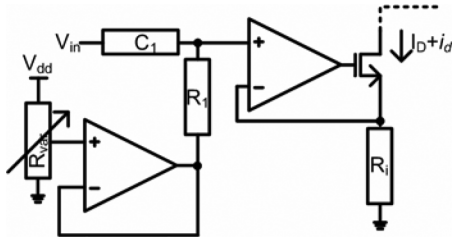

Fig. 12. Schematic for generating $I_D + i_d$.

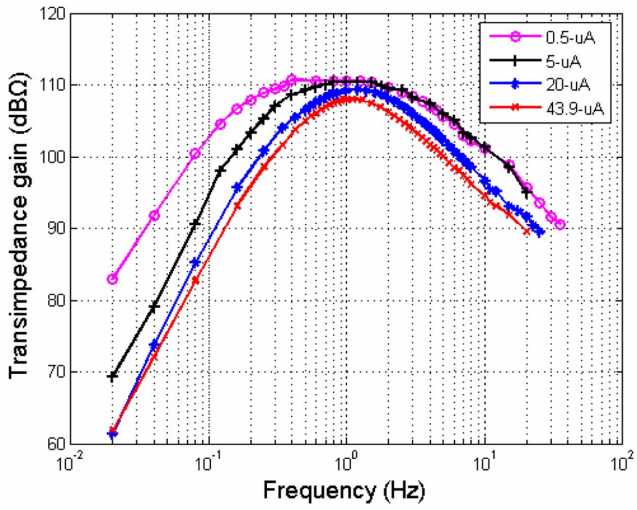

Fig. 13. With $I_D = 6\ \mu$A and $i_d = 1.08\ \mu$A. $f_{-3\ \mathrm{dB}}$ low $= 0.36$ Hz, and $f_{-3\ \mathrm{dB}}$ high $= 6.5$ Hz, respectively.

(maximum) and stopband (minimum) signal tones with small enough amplitude are used for calculating the attenuation. This plot demonstrates the dc rejection capability of the system in the presence of various amount of dc photocurrent. The common-mode dynamic range (CMDR), which is defined as the ratio between the maximum and the minimum dc current that achieves at least 20 dB attenuation at its lower stop-band with respect to its passband in the frequency response, is 54.5 dB (from 0.1 to 53.4 μA). This means that the system can operate with a LED duty cycle from 0.2 percent to 70 percent, which is very robust and sufficient for our application. The CMDR is dictated by the lower frequency pole (ω_{HP}) and is related to the off-chip compensation capacitor (C_m), which can be integrated later in future development [9].Fig. 15 shows the FFT of the overall system with a 0.85 Hz in-band tone with I_D of 5 μA and signal current i_{dpk} of 324 nA. The SNDR is about 37.7 dB, which is acceptable for our application.

In Fig. 16, the inputs to the system are in-band sinusoidal current with various amount of dc current (I_D) from 0.1 to 43.9 μA, to demonstrate the system's ability to reject dc current. The dc level of the output waveforms settles to 1.64 V.

VII. Physiological Test

The LED is operated at 10% duty cycle and its pulsed power consumption is set to 600 μA. I_D is approximately at 6–8 μA, which is in good agreement with the assumption made earlier. The necessary clock waveforms [14] for the LED driver and

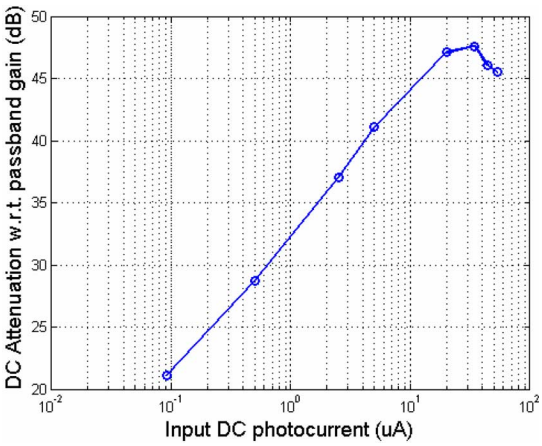

Fig. 14. To illustrate common-mode dynamic range of overall system. For a 20-dB attenuation, the circuit works with I_D from 0.1 to 53 μA, which is about 54.5 dB.

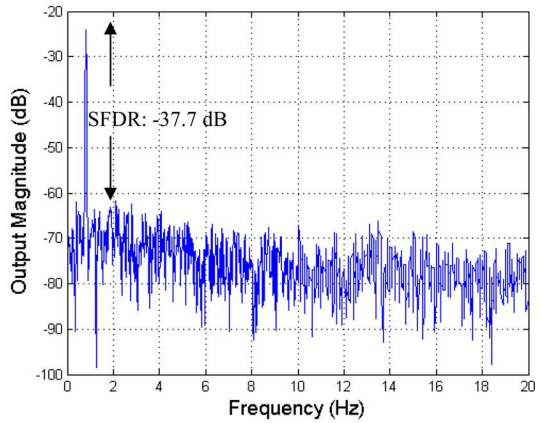

Fig. 15. FFT of output transient waveform at I_D of 5 μA. SFDR and SNDR are both 37.7 dB.

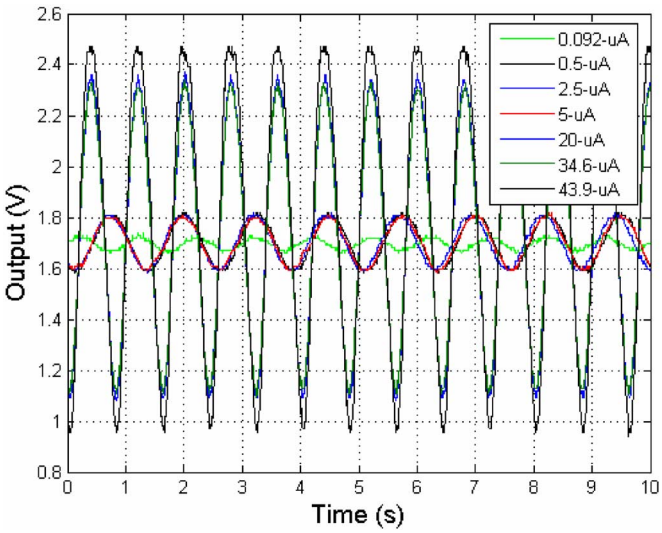

Fig. 16. Transient waveform of overall system with different amount of I_D, to demonstrate the functionality of over all system to reject dc current.

the S/H are implemented using 74HC4538N. The start up transient is shown in Fig. 17, which is taken at the output of the CS-LPF when an index finger is placed onto the sensor unit

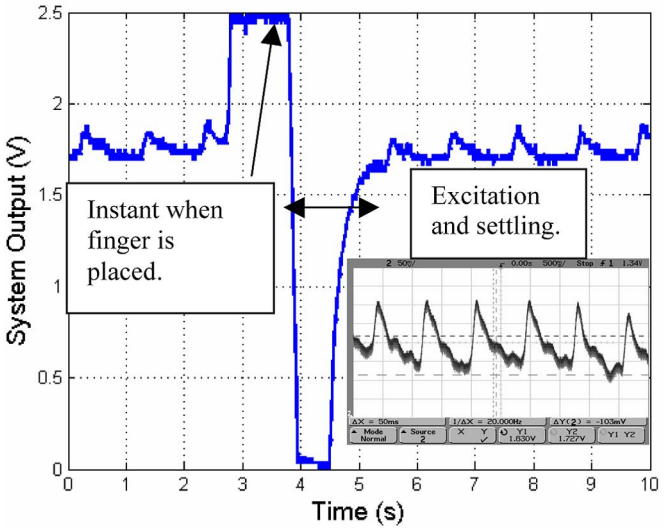

Fig. 17. Transient response of the circuit during start-up; this is taken at the output of CS-LPF. Inset: zoom in waveform of transient figure. It settles at 1.77 V.

(Waitrony RS-05FS). As the tip of the index finger is placed onto the sensor, the system is excited and hence the overshoot, after which the feedback loop activates to perform dc photocurrent rejection. The settling time for the circuit is about 1.68 s and is adequate since the circuit operates at very low frequency. The inset is the zoom-in image, which displays the actual PPG signal when it settles. The overall system (TIA, amplifier and CS-LPF) is clearly working as distinguished features of the PPG signal can be noted (dichromatic notch and peak, etc.) and the signal settles at about 1.77 V. There is a discrepancy between the simulation and experimental results due to an offset of 3–4 mV at the output of the TIA, which causes the output dc level to be about 400 mV higher than expected. Conversely, this is minimal compared to the rise of dc level if no dc rejection mechanism is presented. For instance, a signal with I_D of 34.6 μA gives a 10.96 V rise at its output level $(34.6\ \mu\text{A} \bullet 2000 \bullet 207.5 = 10.96\text{-V})$.

Fig. 18 shows the PPG waveform taken at the output of the system for 12 different subjects to demonstrate consistency and functionality of entire system. Clearly, the circuit is working as all output settles to about 1.77 V and the amplitude of the PPG signal does not change much from person to person. Accordingly, the proposed circuit can remove the dc offset properly and increases DR of the system. The performance of the PPG AFE is recapped in Table III.

From Table III, the slightly higher power consumption is due to the current consumed by the buffer that provides the bias to the noninverting amplifier, which is about 89-μA. Since this circuit will be employed in a wearable system, the current consumption is deemed to be satisfactory. Table IV shows the comparison with other works. Though the current consumption of this PPG AFE is a bit high, this AFE achieves the widest range of dc current rejection by the simple addition of an S/H circuit to reject dc component of the pulsed input.

VIII. Conclusion

A NIR CMOS front-end for PPG with a new dc photocurrent rejection technique for pulsed signal source has been proposed.

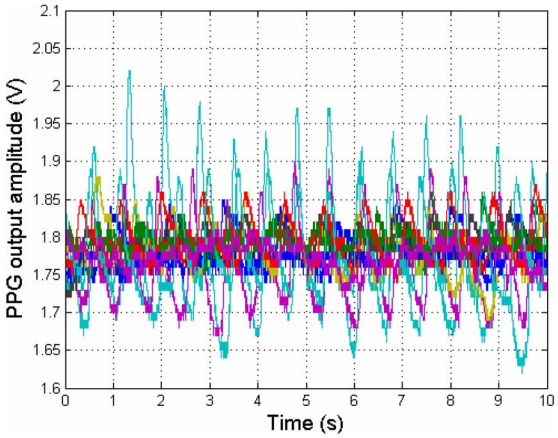

Fig. 18. PPG of 12 subjects to demonstrate consistency and functionality of the entire system. They all settle to about 1.77 V.

TABLE III
PERFORMANCE OF THE PPG SIGNAL PROCESSING CHAIN

Technology	4M/2P 0.35-μm CMOS
Supply voltage	2.5-V
Power consumption	0.6-mW (PPG AFE only)
Frequency cutoff	0.6-Hz (lower band) 1.8-Hz – 62-Hz (upper band)
DC current (I_D) rejected	0.1-μA – 43.9-μA
THD/SNDR	37.7-dB
Dynamic range	29.8-dB
Core area	0.55-mm^2

TABLE IV
COMPARISON WITH OTHER WORKS

Ref	Process (CMOS)	V_{dd}	f_{-3dB} (Hz)	Current (A)	Noise (integrated)	I_D rejected
[4]	0.18-μm	1.8	0.3 – 50K	166μ (TIA)	2.2 nA	N/A
[6]	1.5-μm	2.8	N/A	34.3 μ (TIA)	10 μV	30μA
[16]	0.35-μm	1.0 – 1.8	8 – 30	3 μ	N/A	N/A
This work	0.35-μm	2.5	0.5 – 6.5	240 μ	3.53 nA	0.1 – 43.9 μA

It uses S/H circuit in the feedforward direction, together with the error amplifier in the feedback path of the TIA and the CS-LPF to detect the output dc level accurately so that a correct amount of current can be sunk at the input side. Experimental results verified the functionality of the system and the robustness of the design with various amounts of dc photocurrent.

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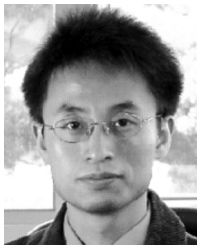

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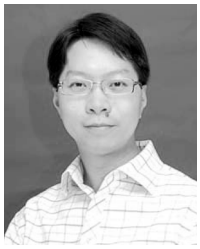

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