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Narra Hemanth Reddy

Electronics and Communication Engineering Undergraduate

Key Skills

- Software Proficiency in MATLAB

Industry Knowledge

PCB Layout, Embedded Systems Design, Flexible Circuits design, FPGA programming

- Tools and Technologies:
  Work Experience of Arduino, PSPICE, Altium PCB Designer, Bolt WIFI Module, ESP8266, Proteus

Coding Languages

- Scripting Language: Python (Libraries: matplotlib, NumPy, cv2).
- Hardware Description Language: Verilog
- Programming Language: C , C++, Verilog HDL, Linux(beginner)
- Data Structures and Algorithms

MOOCs

- Deep Learning, on Coursera.
- NPTEL Course by NIELIT – FPGA Architecture and Programming using Verilog

Education

May 2019 – Present **JNTUH College of Engineering, Hyderabad**
Pursuing B. Tech in Electronics and Communication Engineering and secured 8.5 absolute GPA in aggregate up to fifth semester.

April 2006 – March 2019 **Junior College and Tenth Standard** *Affiliated to TS*
Appeared for TS Board Intermediate Examination in 2019 and scored 959 out of 1000 securing 95.9 percentage in aggregate.Appeared for TS board of Secondary Education Examination in 2017 and secured 9.8 CGPA out of 10 in aggregate.

Projects & Internships

April 2022 – Summer Research Project
Present **Graphite on paper based sensor for the respiration rate monitoring.** *NIT Warangal*

Project Guide: Dr. Md. Farukh Hashmi, Assistant Professor, Department of Electronics and Communication Engineering.
Project Description: Design and Fabrication of Graphite on paper-based sensor for respiration rate monitoring system using ESP8266 WIFI Module. This project is a part of the Summer Research Internship. Patent application is undergoing.

May 2021 – July 2021 During Research Intern at IIT BHU
Design and Implementation of Photoplethysmography Signal-based Heart-Rate Monitoring System. *IIT BHU*
Project Guide: Dr. Priya Ranjan Muduli, Assistant Professor, Department of Electronics and Communication Engineering.
Project Description: An analog-front-end circuit, simulated using PSPICE and PCB designed by Altium, used as the Signal ConditioningUnit to make the PPG signals compatible for Arduino microcontrollerused as the Signal Processing Unit to calculate the heart-rate.

July 2022 – VLSI Project

FPGA Prototyping using Xilinx IP
Project Guide: Shri. Sreejeesh S G (Senior Technical Officer) at NIELIT
Project Description: The project was the part of the NPTEL course. Under the project Xilinx Vivado tool was used to integrate modules like Xilinx counter IP, multiplexer, latch, decoder to implement a digital circuit. The code was dumped in to FPGA board -XC7A50T-1CSG324

June 2022 – Project Intern at IIT Bombay (FOSSEE)
July 2022 **SOC Design tool for SKY130/esim Development**
Project Guide: Mr. Kunal Ghosh and Sumanto Kar
Project Description: I have involved in the SOC Design tool development for esim open-source tool alternative to Pspice simulation tool. My contribution was to design and verification of subcircuits for Analog IP's.

- NPTEL:
  Digital Electronics and Verilog HDL

Hobbies

- Cricket – Cooking – Chess
- Drones

Miscellaneous

2022 **Patents and Publication**

Organizing Institute: NIT Warangal

During the internship at NIT Warangal, a research project was executed. This has been selected for application of patent. The patent will be published within a month.

2022 **Capture the BUG Hackathon**

Organizing Institute: IIT Bombay [FOSSEE], IIT Madras, NIELIT, Vyoma Systems

Under this hackathon I am going to implement Chip 74181 ALU using Verilog. A bug will be inserted into the program. Using the Vyoma tool, the bug will be detected and rectified using python's cocotb library.

2021 **Mixed Signal Circuit Design and Simulation Marathon**

Organizing Institute: IIT Bombay [FOSSEE]

Designed Johnson Counter using Astable Multivibrator which secured a 12th place among 1722 candidates all over India.

2018 **TS EAMCET**

Organizing Institute: JNTU

Secured rank 1296 with Score 96 among 242825 candidates.