TEEDA HEMANTH KUMAR

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EDUCATION

Master of Technology in VLSI Design, IIT Jammu — **Expected 2026**
CGPA: 8.02/10 — J&K, India

Bachelor of Electronics and Communication Engineering, Andhra University — **2019 - 2023**
CGPA: 8.23/10 — AP, India

Intermediate (MPC), Sri Chaitanya Junior College — **2016 - 2018**
CGPA: 95.4% — AP, India

SSC, Ravindra Bharathi School — **2015 - 2016**
CGPA: 9.7/10 — AP, India

PROJECTS

Five-Stage Pipelined RISC-V RV32I Processor - Thesis (GitHub Link) — **July 2025 - May 2026**

- Designed and implemented a **5 stage pipelined RISC-V RV32I processor** in Verilog HDL with full hazard detection and forwarding logic, and validated **100% functional correctness** at **60 MHz** using C based instruction tests, RISC-V toolchain hex generation, and waveform simulation analysis.

RTL-GDSII of 3×3 Systolic Array for Matrix Multiplication(GitHub Link) — **May 2025**

- Designed a **3×3 systolic array** in Verilog HDL for high-throughput matrix multiplication using parallel data flow between processing elements and completed full RTL to GDSII implementation in Cadence Genus & Innovus, achieving timing closure at **100 MHz, 72% utilization**, and **0 ns WNS** on the SCL 180 nm PDK.

Basic FIFO Verification in SystemVerilog (GitHub Link) — **July 2025 - May 2026**

- Created a basic **FIFO** verification environment in SystemVerilog using driver, monitor, and scoreboard components, and achieved **95% functional coverage** with **zero errors** using assertions and randomized test stimulus.

SKILLS

Programming Languages:	C, Python (Basics), Linux Shell (Basics).
Hardware Description & Scripting Languages:	Verilog HDL, SystemVerilog (Basics), TCL.
EDA Tools:	Xilinx Vivado, Cadence Genus, Cadence Innovus, Cadence Virtuoso, and Cadence NCLaunch.
Protocols:	UART.
Soft Skills:	Team Collaboration, Technical Documentation, Time Management, Presentation Skills.

POSITIONS OF RESPONSIBILITY

- Managed and maintained the student branch website, conducted technical workshops and webinars, and coordinated digital outreach and communication as **WebMaster** at **IEEE CASS SBC, IIT Jammu**.
- Represented the NGO initiatives on campus, led awareness drives, organized outreach activities and facilitated volunteer engagement as as **College Ambassador, Humanity Uplifting Mankind NGO**.
- Served as **School Leader** at **Ravindra Bharathi School**, facilitating student participation in school events, organizing extracurricular activities, and maintaining effective communication between students and faculty.

ACHIEVEMENTS

- Represented IIT Jammu at **Inter-IIT Tech Meet 14.0**, securing **7th** place among **23 IITs**, contributing as a **Physical Design** ranked 1st and mentored RTL team ranked 2nd in scoring for the project **ISRO PS-39**.
- As **Webmaster**, facilitated a successful collaboration between **IEEE IISc Bangalore** and **IEEE CASS SBC IIT Jammu** by supervising the technical plans and coordinating all organizational aspects of the joint event.