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By K B Hemanth Raj

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17CS46

Fourth Semester B.E. Degree Examination, Dec.2019/Jan.2020 **Data Communications**

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

Describe data communication and its components. (05 Marks)

Analyze the principle behind protocol layering. Enumerate the functions of different layers of OSI model. (10 Marks)

Differentiate Defacto standard and Dejure standard.

(05 Marks)

OR

Analyze the causes of transmission impairments. 2 (05 Marks)

Define line coding. Enumerates the challenges in line coding. Draw the line code of the sequence 010011110 using polar NRZ - L and NRZ - I schemes. (10 Marks)

In a digital transmission, the receiver clock is 0.3 percent faster than the sender clock. How many extra bits per second does the receiver receive if the data rate is 1Mbps. (05 Marks)

Module-2

Explain the three step procedure of pulse code modulation for analog to digital conversion 3 with example. (10 Marks)

Briefly explain with neat diagrams. Amplitude shift keying and frequency shift keying modulation techniques. Specify bandwidth requirements. (05 Marks)

An analog signal has a bit rate of 8000 bps, and a baud rate of 1000 baud. How many data element are carried by each signal elements? How many signal elements do we need?

(05 Marks)

(05 Marks)

Describe about Frequency Division Multiplexing in brief with neat diagram. (05 Marks)

What is circuit switching? Enumerate the characteristics of circuit, switching. Analyze the three stages of circuit switching. (10 Marks)

Analyze how message can be transmitted from one system to another using datagram network and calculate the total delay in the network. (05 Marks)

Module-3

Describe three types of errors. (05 Marks)

Explain the encoder and decoder logic of Cyclic Redundancy Check (CRC) coding with neat diagram.

Given message = 1011011, k = 7 and generator polynomial $P(X) = X^3 + X^2 + X^0$, n = 3. Find the codeword and design the checker in the receiver using Cyclic Redundancy Codes (CRC).

OR

Explain the working of stop-and-wait protocol for Noiseless channels. (05 Marks)

Explain selective repeat ARQ protocol for noisy channels. (05 Marks)

Explain the frame format of HDLC protocol. (05 Marks)

Describe the transition phases of PPP protocol with Finite State Machines. (05 Marks)

42+8 = 50, will be treated as malpractice. Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Any revealing of identification, appeal to evaluator and /or equations written eg,

Module-4

- a. Analyze the need for access control protocols. Explain the working of CSMA/CD with (10 Marks) suitable diagrams.
 - Describe pure ALOHA and slotted ALOHA protocols.

(05 Marks)

Discuss 802.3 MAC frame format.

(05 Marks)

Analyze Gigabit Ethernet. 8

(05 Marks)

Brief on Bluetooth and explain the architecture of Bluetooth.

(05 Marks)

Analyze channelization. Explain Code Division Multiple Access (CDMA) with an example.

(10 Marks)

Module-5

Explain the operation of cellular telephony.

(05 Marks)

Explain the working of mobile IP.

(05 Marks)

Analyze satellite networks and its different categories.

(10 Marks)

OR

- a. Explain IP datagram header format with neat diagram and given the description of each 10 (10 Marks)
 - Explain the transition from IPV4 to IPV6.

(05 Marks)

Write a short note on fixed WiMax.

(05 Marks)

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