[As ner Choice )		RCHITECTURES		
_ <b>_</b>	•	tem (CBCS) scheme]		
(Effective from the academic year 2017 - 2018)				
0.11 0.1	SEMESTER –		1	40
Subject Code	17CS72	IA Marks		40
Number of Lecture Hours/Week	4	Exam Marks		60
Total Number of Lecture Hours	50	Exam Hours	03	
	CREDITS - 0	)4		
Module – 1				Teaching
				Hours
Theory of Parallelism: Parallel C	-	-	_	10 Hours
Multiprocessors and Multicompute				
and VLSI Models, Program and N	*			
Program Partitioning and Schedu				
Interconnect Architectures, Princi Metrics and Measures, Parallel Pr				
Laws, Scalability Analysis and App	0 11	nons, speedup Perion	mance	
Module – 2	noaches.			
Hardware Technologies: Processors	s and Memory His	erarchy Advanced Pro	cessor	10 Hours
Technology, Superscalar and Vector				TO HOULS
Virtual Memory Technology.	7 110ccs5015, 1vici	nory incrarcity recim	ology,	
Module – 3				
Bus, Cache, and Shared Memory	Bus Systems Ca	ache Memory Organiz	ations	10 Hours
Shared Memory Organizations ,	-	• •		IO IIOUI
Pipelining and Superscalar Techn	•	_		
Pipeline Processors ,Instruction P				
(Upto 6.4).	1 0 /	1	C	
Module – 4				
Parallel and Scalable Architector	ures: Multiproce	ssors and Multicom	nuters	10 Hours
,Multiprocessor System Interconne	_		paters	TO HOURS
	ects, Cache Con	erence and Synchroni	_	10 Hours
		erence and Synchroni mputers ,Message-P	zation	10 Hours
	ns of Multico	mputers ,Message-P	zation assing	10 Hours
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Com	ns of Multico MD Computers ,V npound Vector P	mputers ,Message-Parector Processing Print rocessing ,SIMD Con	zation assing aciples nputer	10 Hours
Mechanisms, Three Generation Mechanisms, Multivector and SIN, Multivector Multiprocessors, Con Organizations (Upto 8.4), Scalable,	ns of Multicon MD Computers ,V npound Vector P , Multithreaded, a	mputers ,Message-Parector Processing Print rocessing ,SIMD Contained Dataflow Architecture	zation assing aciples nputer	TO HOURS
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Com Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P	ns of Multicon MD Computers ,Volume Vector P , Multithreaded, a rinciples of M	mputers ,Message-Parector Processing Print rocessing ,SIMD Contained Dataflow Architecture Multithreading, Fine-	zation assing aciples inputer ctures, Grain	10 Hours
Mechanisms, Three Generation Mechanisms ,Multivector and SIN ,Multivector Multiprocessors ,Con Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi	ns of Multicon MD Computers ,Volume Vector P , Multithreaded, a rinciples of M	mputers ,Message-Parector Processing Print rocessing ,SIMD Contained Dataflow Architecture Multithreading, Fine-	zation assing aciples inputer ctures, Grain	TO HOURS
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Con Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Mult Architectures.	ns of Multicon MD Computers ,Volume Vector P , Multithreaded, a rinciples of M	mputers ,Message-Parector Processing Print rocessing ,SIMD Contained Dataflow Architecture Multithreading, Fine-	zation assing aciples inputer ctures, Grain	TO Hours
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Com Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi-Architectures.  Module – 5	ns of Multicom MD Computers ,Vonpound Vector Post, Multithreaded, a principles of Multithreaded Archite	mputers ,Message-Parector Processing Pringrocessing ,SIMD Contained Dataflow Architectures, Dataflow and Head of the Parectures, Dataflow and Head of the Parec	zation assing aciples	
Mechanisms, Three Generation Mechanisms, Multivector and SIM, Multivector Multiprocessors, Com Organizations (Upto 8.4), Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi-Architectures.  Module – 5  Software for parallel programming	ns of Multicon MD Computers ,V npound Vector P , Multithreaded, a trinciples of M tithreaded Archite	mputers ,Message-Parector Processing Printer rocessing ,SIMD Contant Dataflow Architectures, Dataflow and Futures, Dataflow and Futu	zation assing aciples inputer ctures, Grain Hybrid	
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Com Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi-Architectures.  Module – 5  Software for parallel programming ,Parallel Programming Models, Parallel Programming Models, Parallel Programming Models	ns of Multicom MD Computers, Vanpound Vector Post, Multithreaded, a crinciples of Multithreaded Archite Parallel Models rallel Languages	mputers ,Message-Parector Processing Printer processing ,SIMD Contained Dataflow Architectures, Dataflow and Found Languages, and Comand Compilers ,Dependent of the process of the proces	zation assing aciples inputer ctures, Grain Hybrid	
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Com Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi Architectures.  Module – 5  Software for parallel programming ,Parallel Programming Models, Par Analysis of Data Arrays ,Parallel	ns of Multicom MD Computers ,Volume MD Multithreaded, a Multithreaded, a Multithreaded, a Multithreaded, a Multithreaded, a Multithreaded, a Multitor  MD Multithreaded, a Multitor  MD Multithreaded, a	mputers ,Message-Parector Processing Printer processing ,SIMD Contained Dataflow Architectures, Dataflow and Found Languages, and Compand Compilers ,Dependent and Environment and Environment	zation assing aciples inputer etures, Grain Hybrid inpilers idence ments,	
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Con Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Mult Architectures.  Module – 5  Software for parallel programming ,Parallel Programming Models, Par Analysis of Data Arrays ,Parallel Synchronization and Multiprocess	ns of Multicom MD Computers , Very Multithreaded, a drinciples of Multithreaded Archite described by the Models and the Models and Models and Models and Models. Instance of Models and Mod	mputers ,Message-Parector Processing Printer rocessing ,SIMD Control Dataflow Architectures, Dataflow and Fundament Compand Compilers ,Dependent and Environment and System of the Processing and Compilers and Compilers ,Dependent and System of the Processing Printer Printe	zation assing aciples inputer ctures, Grain Hybrid inpilers adence ments, Level	
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Com Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi-Architectures.  Module – 5  Software for parallel programming ,Parallel Programming Models, Parallel Programming Models, Parallelsm, Instruction Level Parallelism, Instruction Level Parallelism	ns of Multicom MD Computers, Vanpound Vector Post Multithreaded, a crinciples of Multithreaded Archite Extracted Languages of Program Develosing Modes. Instantial Instantial Computation of Multithreaded Archite Extracted Languages of Program Develosing Modes. Instantial Computation of Multicom No.	mputers ,Message-Parector Processing Printrocessing ,SIMD Contend Dataflow Architectures, Dataflow and House and Compilers ,Dependent and Environmental Environment and System atter Architecture ,Contend Tour Contend Tour Conte	zation assing aciples inputer ctures, Grain Hybrid inpilers adence ments, Level intents,	
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Con Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi Architectures.  Module – 5  Software for parallel programming ,Parallel Programming Models, Par Analysis of Data Arrays ,Paralle Synchronization and Multiprocess Parallelism, Instruction Level Par Basic Design Issues ,Problem I	ns of Multicom MD Computers, Vanpound Vector Post Multithreaded, a principles of Multithreaded Archite Models and Languages of Program Develosing Modes. Installelism ,Computer Computer Models (Computer Models), Models (Compute	mputers ,Message-Parector Processing Printer rocessing ,SIMD Contained Dataflow Architectures, Dataflow and Formand Compilers ,Dependent and Environmental Compilers and System and System and Compilers ,Contained of a Typical Processing Printer Prin	zation assing aciples inputer ctures, Grain Hybrid inpilers idence ments, Level intents, cessor	10 Hours
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Con Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi Architectures.  Module – 5  Software for parallel programming ,Parallel Programming Models, Par Analysis of Data Arrays ,Parallel Synchronization and Multiprocess Parallelism, Instruction Level Pa Basic Design Issues ,Problem I ,Compiler-detected Instruction Level	ns of Multicom MD Computers , Very Manager of Multithreaded, a drinciples of Multithreaded Archite of Parallel Models of Program Development of Multithreaded Archite of Multithreaded Archite of Parallel Multithreaded Archite of Parallel Multithreaded Archite of Parallel Multithreaded Archite of Multithreaded, and Multithreade	mputers ,Message-Parector Processing Printrocessing ,SIMD Control Dataflow Architectures, Dataflow and Forward Compand Compilers ,Dependent and Environment and System and System and Forwarding ,Repeated Forwarding ,Repe	zation assing aciples inputer ctures, Grain Hybrid inpilers adence ments, Level intents, cessor eorder	
Mechanisms, Three Generation Mechanisms ,Multivector and SIM ,Multivector Multiprocessors ,Con Organizations (Upto 8.4),Scalable, Latency-Hiding Techniques, P Multicomputers, Scalable and Multi Architectures.  Module – 5  Software for parallel programming ,Parallel Programming Models, Par Analysis of Data Arrays ,Paralle Synchronization and Multiprocess Parallelism, Instruction Level Par Basic Design Issues ,Problem I	ns of Multicom MD Computers, Vanpound Vector Possible Multithreaded, a principle of Multithreaded Archite Mult	mputers ,Message-Parector Processing Printrocessing ,SIMD Control Dataflow Architectures, Dataflow and Formand Compilers ,Dependent and Environmentary and Environmentary and Environmentary and Environmentary (Control Data Typical Proper Perand Forwarding ,Register Architecture ,Control Data Typical Proper Processing ,Register Architecture ,Register Architecture ,Register Architecture ,Register	zation assing aciples inputer ctures, Grain Hybrid inpilers adence ments, Level intents, cessor eorder iction,	

# https://hemanthrajhemu.github.io

## **Course outcomes:** The students should be able to:

- Understand the concepts of parallel computing and hardware technologies
- Illustrate and contrast the parallel architectures
- Recall parallel programming concepts

## **Question paper pattern**

The question paper will have ten questions.

There will be 2 questions from each module.

Each question will have questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

### **Text Books:**

1. Kai Hwang and Naresh Jotwani, Advanced Computer Architecture (SIE): Parallelism, Scalability, Programmability, McGraw Hill Education 3/e. 2015

### **Reference Books:**

1. John L. Hennessy and David A. Patterson, Computer Architecture: A quantitative approach, 5th edition, Morgan Kaufmann Elseveir, 2013