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10CS74

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
Advanced Computer Architectures

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What do you mean by instruction set Architecture (ISA)? Briefly explain the various dimensions of ISA addressed during defining the computer architecture. **(10 Marks)**

b. Assume a disk subsystem with the following components and MTTF.
- 10 disks each rated at 1,000,000 hr MTTF
- 1 SCSI controller, 500,000 – hour MTTF
- 1 Power supply, 200,000 – hour MTTF
- 1 Fan, 200, 000 – hour MTTF.
- 1 SCSI cable, 1,000,000 – hour MTTF.

Using the simplifying assumptions that the lifetimes are exponentially distributed and that failure are independent, compute the MTTF of the system as a whole. **(06 Marks)**

c. Write note on the performance equation of processor. **(04 Marks)**

2 a. Enlist the pipeline hazards. Also explain them. **(10 Marks)**

b. With an aid of a neat functional diagram, discuss the classic 5 – stage pipeline for a Risc processor, that highlight how an instruction flows through the data path. **(10 Marks)**

3 a. What do you mean by loop unrolling? Explain the significance of it. Further, discuss the various types of limits to the gains that can be achieved by loop unrolling. **(10 Marks)**

b. What is dynamic production? Draw the state transition diagram for a 2-bit prediction scheme and explain. **(07 Marks)**

c. Compare and contrast the correlating predictors and Tournament predictors. **(03 Marks)**

4 a. Briefly discuss the different strategies employed to exploit Instruction Level Parallelism (ILP) using multiple issue and static dynamic scheduling. **(10 Marks)**

b. Discuss how the following advanced techniques are useful in enhancing the performance of ILP :
i) Branch target buffers
ii) Speculation
iii) Value prediction. **(10 Marks)**

PART – B

5 a. Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential? **(06 Marks)**

b. Discuss the directory – based cache coherence protocol in a distributed memory multiprocessor, indicating the state transition diagram explicitly. **(07 Marks)**

c. What do you understand by memory consistently? Explain furthermore, discuss how relaxed consistently models allow reads and write to complete out of order. **(07 Marks)**

6 a. Briefly explain the six basic cache optimization employed to improve cache performance. **(09 Marks)**

b. Indicate the distinguish features of the following techniques employed to improve cache behavior.
   i) Compulsory misses
   ii) Capacity misses
   iii) Conflict misses **(06 Marks)**

c. In brief, discuss the four memory hierarchy questions for virtual memory. **(05 Marks)**

7 a. Briefly explain the eleven advanced optimizations of cache performance. **(12 Marks)**

b. Explain how the protection of processes is accomplished via the following :
   i) Virtual memory
   ii) Virtual machines. **(08 Marks)**

8 a. Discuss how software pipelining and trance scheduling techniques are useful in uncovering the parallelism among instructions by creating longer sequences of straight sine code. **(10 Marks)**

b. Explain the five different execution unit types in the IA-64 architecture, that hold the corresponding instruction classes. **(10 Marks)**

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