FUTURE VISION BIE

One Stop for All Study Materials

& Lab Programs

Future Vision

By K B Hemanth Raj

Scan the QR Code to Visit the Web Page

Or

Visit : https://hemanthrajhemu.github.io

Gain Access to All Study Materials according to VTU,
CSE – Computer Science Engineering,
ISE – Information Science Engineering,
ECE - Electronics and Communication Engineering
& MORE...

Join Telegram to get Instant Updates: https://bit.ly/VTU_TELEGRAM

Contact: MAIL: futurevisionbie@gmail.com

INSTAGRAM: www.instagram.com/hemanthraj_hemu/

INSTAGRAM: www.instagram.com/futurevisionbie/

WHATSAPP SHARE: https://bit.ly/FVBIESHARE

DIGITAL SYSTEM DESIGN USING VERILOG

B.E., VI Semester (Open Elective)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code:	**17EC663**	**CIE Marks: 40**
Number of Lecture Hours/Week:	**03**	**SEE Marks: 60**
Total Number of Lecture Hours:	**40 (08 Hrs per module)**	**Exam Hours: 03**

CREDITS – 03

Course Objectives: This course will enable students to

- Understand the concepts of Verilog Language.
- Design the digital systems as an activity in a larger systems design context.
- Study the design and operation of semiconductor memories frequently used in application specific digital system.
- Inspect how effectively IC's are embedded in package and assembled in PCB's for different application.
- Design and diagnosis of processors and I/O controllers used in embedded systems.

Module -1

Introduction and Methodology:
Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology (1.1, 1.3 to 1.5 of Text).

Combinational Basics: Combinational Components and Circuits, Verification of Combinational Circuits.(2.3 and 2.4 of Text)

Sequential Basics: Sequential Datapaths and Control Clocked Synchronous Timing Methodology (4.3 up to 4.3.1,4.4 up to 4.4.1 of Text). **L1, L2, L3**

Module -2

Memories: Concepts, Memory Types, Error Detection and Correction (Chap 5 of Text). **L1, L2, L3**

Module -3

Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity (Chap 6 of Text). **L1, L2, L3**

Module -4

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software (Chap 8 of Text). **L1, L2, L3**

Module -5

Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues (Chap 10 of Text). **L1, L2, L3, L4**

Course outcomes: After studying this course, students will be able to:

- Construct the combinational circuits, using discrete gates and programmable logic devices.
- Describe Verilog model for sequential circuits and test pattern generation.
- Design a semiconductor memory for specific chip design.
- Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
- Synthesize different types of processor and I/O controllers that are used in embedded system.

https://hemanthrajhemu.github.io

Text Book:

Peter J. Ashenden, “Digital Design: An Embedded Systems Approach Using VERILOG”, Elesvier, 2010.

https://hemanthrajhemu.github.io