Design of 4th order bandpass switched capacitor filter with rail to rail swing

Group 4:

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Design of Op-amp:

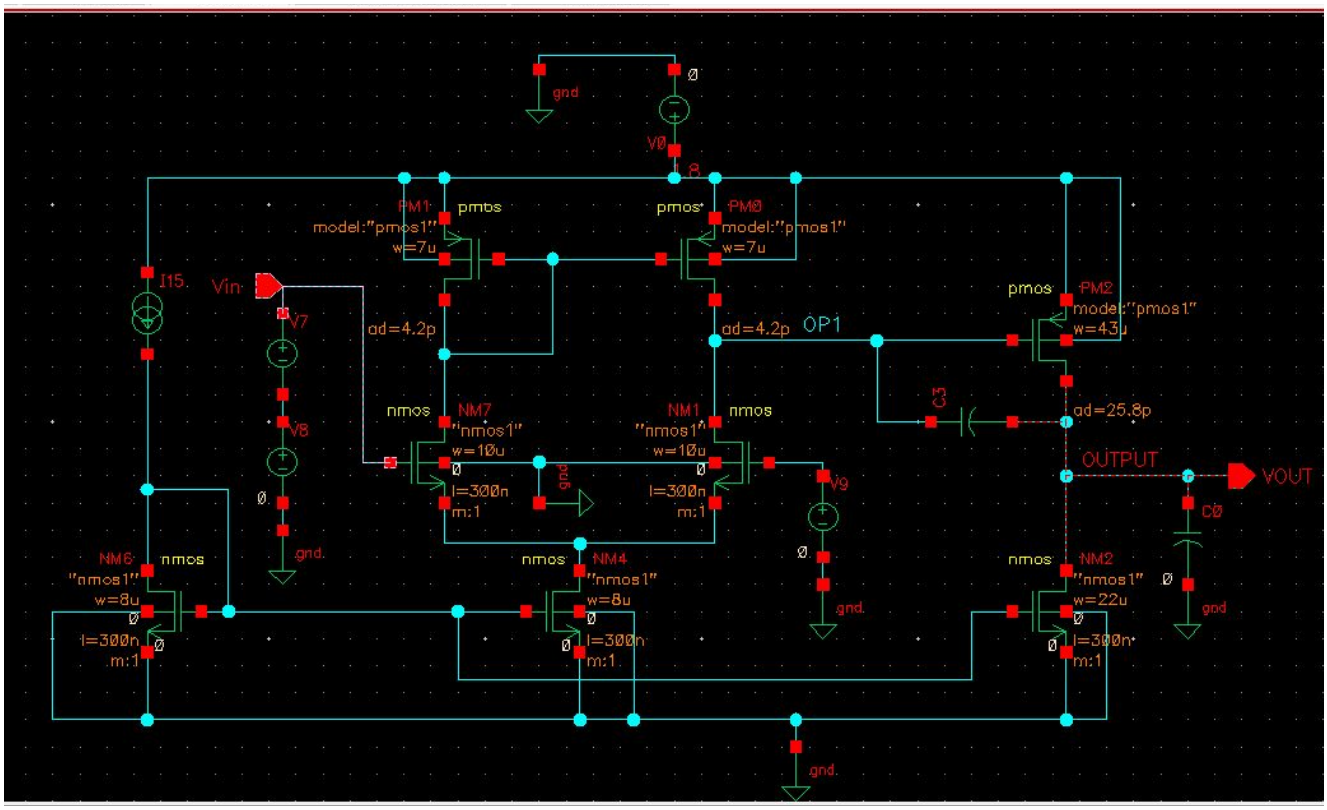
We designed the 4th order filter and simulated in Cadence. In order for better filtering , we require op-amp with gain bandwidth product sufficient to support the desired output. In order to design any active filter we need an Op-amp. The specifications of that Op-amp should be as desired for the filter(based on the topology, filter specifications). The following is the specifications of the Op-amp we would required to design:

Specifications:

- ➢ Av > 40dB
- ➢ GBW = 10 MHz
- ➢ PM > 60 degree
- ➢ Vdd = 1.8V , Vss = 0V
- ➢ O/P Swing = 0.2V – 1.6V
- ➢ SR > 20v/μs
- ➢ ICMR = 0.8V – 1.6V
- ➢ P_{diss} = 0.5mW
- ➢ C_L = 10pF

The above specifications are desired due to the topology that we choose in the earlier stages. The second stage of the Op-amp has the capacitance in the input so we have to aim for an op amp that can drive larger loads hence the C_L is high. The desired gain bandwidth product need not to be so high because of the low frequency range filter that we desire to design. We are targeting a gain of 40 dB gain for op amp

since the closed loop in the topology will reduce the total gain and the two stages of the filter will increase the total gain of the filter hence targeting a filter gain of 40 dB. The architecture that we used to implement the Op-amp is the two stage compensated Op-amp. With it's second stage as common source amplifier to increase the gain. It looks as follows:



Design Outcomes[1]*:*

1. Aspect rations of all transistors in the circuit.
2. Desired gain and bandwidth
3. Components values
4. Biasing Current of each Transistor

[1] The design outcomes are calculated with the same procedure which was taught in the class.

From the theoretical calculation of a two stage OpAmp with compensation capacitor of value equal to the load capacitor the aspect ratios of the transistors are as follows:

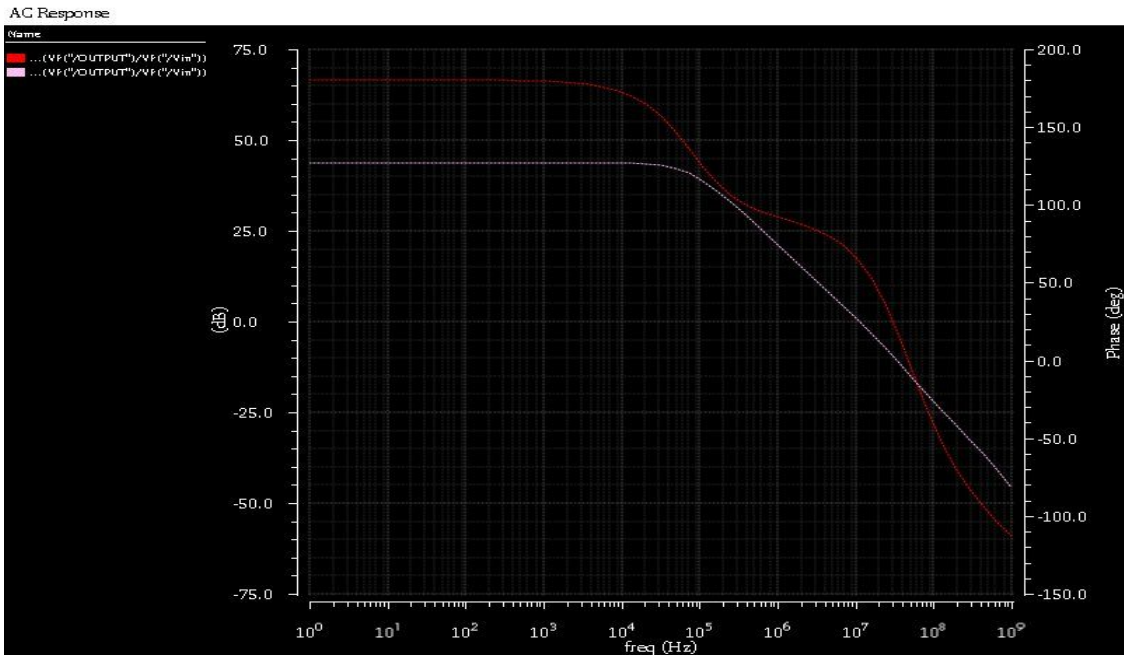
Transistors	Aspect Ratio
M1 , M2	33
M3, M4	23
M5,M8	26
M6	144
M7	73

With the derived aspect ratio the theoretical gain obtained was 40 dB with GBW = 10MHz and Pdiss = 500µWatt

Op-Amp Simulation and Results:
Three specific simulations were performed on the schematic of the OpAmp to verify the results and view its performance in those varied situations.

1. DC Analysis and Static Power consumption. The DC Analysis ensure every transistor remain in saturation. The static power consumption was 500µWatt.

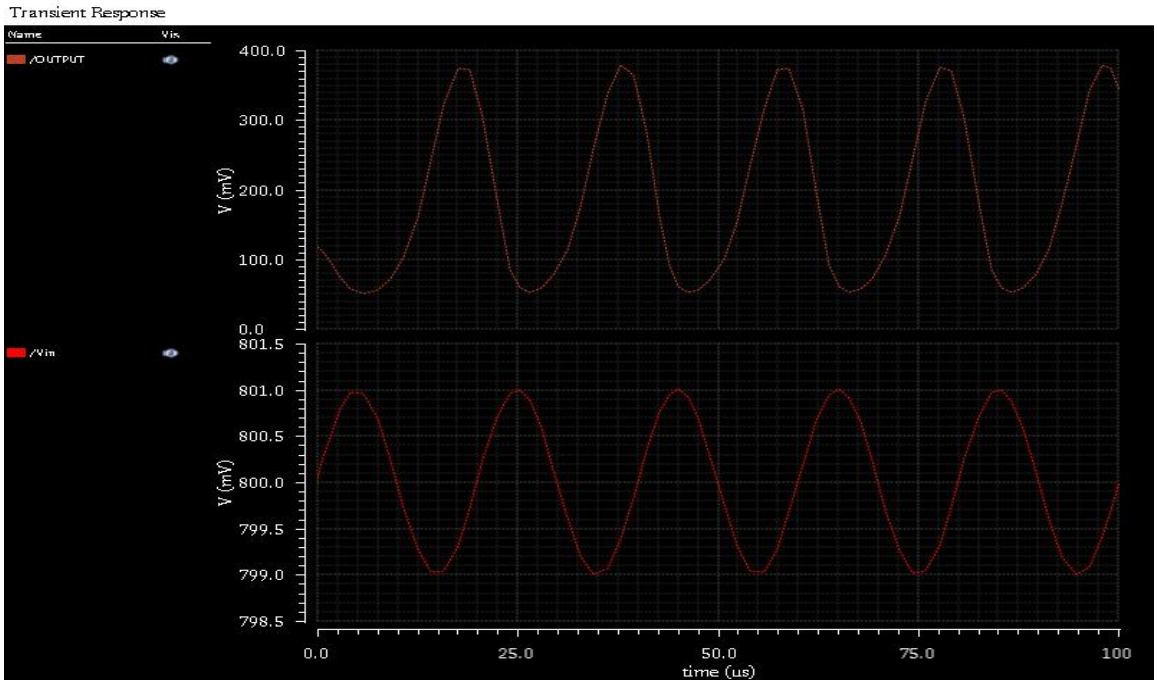
2. AC analysis and Frequency response.



From the frequency response of the schematic, the maximum/DC gain obtained was 43 dB and GBW was 10MHz. The phase margin obtained was at least 60 degree. For the system to be stable when used in the filter circuit, some tuning was performed on the compensation capacitor to improve the phase margin while trading off the gain bandwidth.
when the $C_C = C_L$, the gain bandwidth product is high i.e. 40 Mhz but the PM<60 degrees. The value of C_C is set to the least value(3pF) satisfying the condition of phase margin, then the gain bandwidth product is not as desired. The value of compensating capacitor is set to half of the load capacitance to get the desired results as per specifications.

3. Transient Analysis

The transient response gives a gain of 163.69 or 44.28dB when a



sinusoidal signal of small magnitude is applied. The signal distortion

was seen when the signal amplitude was higher since some transistors would go out of saturation[2].

Active Band pass filter design.

Design of 4th order BPF:

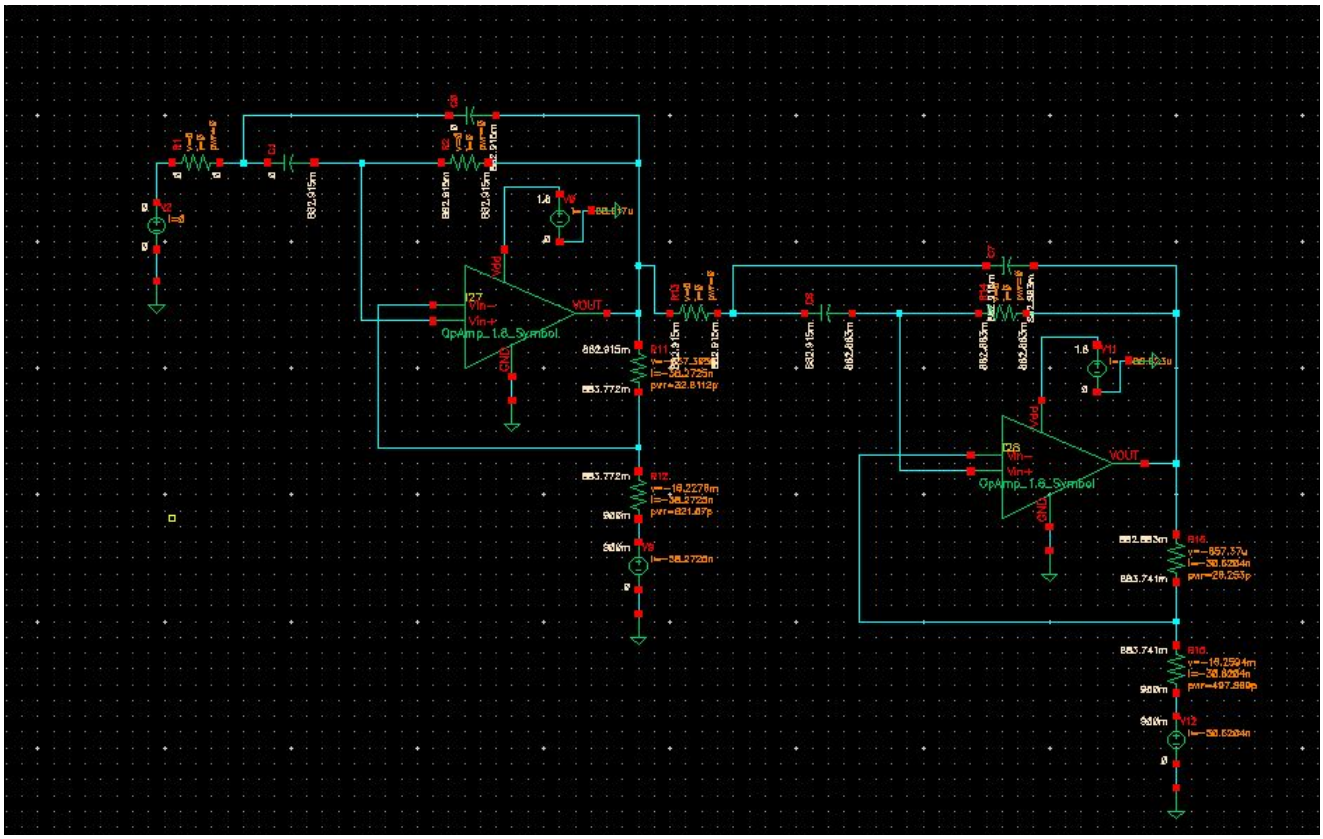
The filter that we desired to design is the 4th order bandpass filter with the band width of 75Hz, a gain of 40 dB and a mid frequency of 40hz. We are aiming for a butterworth filter since it has the low ripple response and given the fact the we are designing a 4th order design which will compensate the transition band. We are using a cascading technique for design of 4th order BPF with two 2nd order BPF multiple feedback topology. Hence it's going to be a two stage filter.

Design steps:

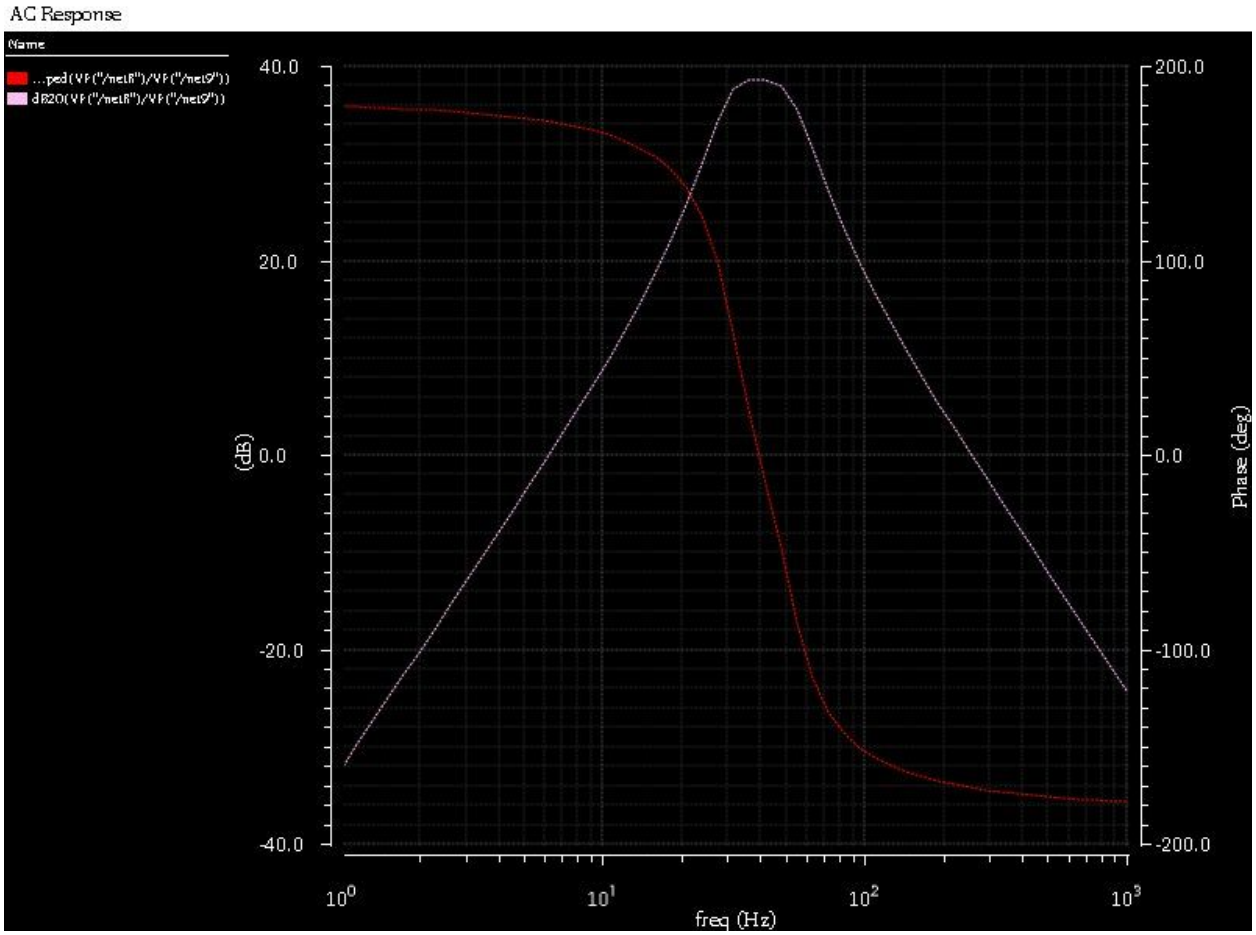
For the design of two stage filter, the required parameters for the individual stages should be calculated i.e individual gain, Q factor of the both filter and the mid frequency of the filters. These parameters is depend on few other parameters like alpha and the different parameter coefficients[3] which decides the nature of the response like butterworth, chebyshev etc c. The desired Q, A_m and f_{m1}, f_{m2} are 0.944, 17.78 and 20Hz, 80Hz. By using the general transfer function comparing with the transfer function of the normal MFB topology[4] when we can get the values of R1,2,3 of each filter for a given C value.

[2] We will try to improve this in the next stage.
[3] Reference 1
[4] Reference 1

The schematic of the design looks as follows:



The above schematic has the biasing at the inverting terminal to give the common mode hence the voltage divider is used to provide it without it the response is not desirable. By adding the same, the circuit passives has to be tuned accordingly. On a good tuning work, the response is as follows:



The drawback of the current circuit biasing is the bandwidth which is coming out to be 30 Hz. The gain and the response is as desired, 39dB which is the gain of the filter and a good no ripple response i.e butterworth response.

Future work:

Optimizing the circuit to increase the bandwidth. We are going to try out the circuit without voltage divider and bias the circuit with some other common mode biasing method and compare the results. Finally, to implement the switch capacitor circuit equivalent of the resistor and replace the resistors with the SC circuits and get the desired response.

References:
1.https://focus.ti.com/lit/ml/sloa088/sloa088.pdf
2.http://www.homeschoolmath.net/worksheets/equation_calculator.php