# Low Power CMOS Comparator Design

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***Abstract*—In this paper, we designed and implemented a Low power CMOS comparator using a 180um technology on cadence. The design has two stages - Differential amplifier which is the preamplifier and a Common source amplifier used to enhance the gain of diff-amp(post amplifier). The power dissipation of the circuit is coming out to be in the range of some micro watt.**

## I. Introduction

A comparator is a circuit with a binary output it gives output as '1' if $V_{in1}$ - $V_{in2} > 0$ else '0'. But this kind of comparator is practically not possible to implement. So we implement a comparator which doesn't have abrupt transition. A range between $V_{high}$ and $V_{low}$ in which difference of inputs is amplified when the difference of input lies in this range and gives an output of '1' or '0' if the difference of input is greater than $V_{high}$ or less than $V_{low}$ respectively. Generally op-amp is used as comparator or a differential amplifier with high gain.

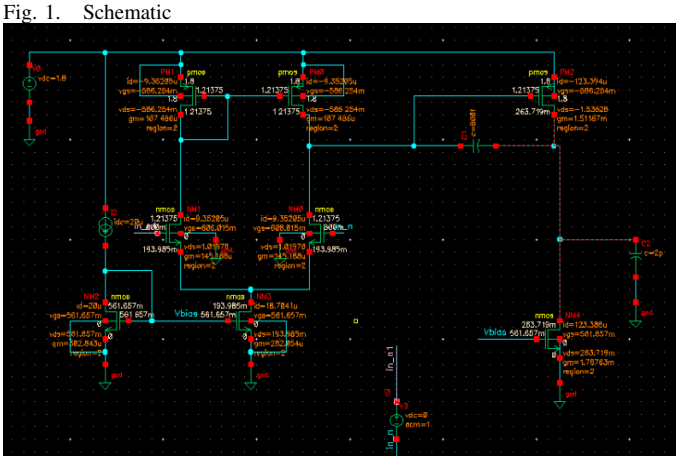
## II. Proposed Design

As stated in the abstract, the design is made using $180nm$ technology on cadence and schematic for the same is given below. Schematic has two stages - differential amplifier and a Common stage amplifier. The output of diff-amp is connected to the input of the CS amplifier to enhance the gain of the diff-amp. So in the small signal model of the circuit we have two RC circuits one at the output of the diff-amp (Drain and source capacitance of NMOS in diff-amp and Gate capacitance of PMOS in CS amplifier) and at the output of CS amplifier due to load capacitance. Hence we have a two pole circuit. But for a two pole system the phase margin is very less, it's nearly equal to zero. If the phase margin is not sufficiently high then the output will have ringings in it which we do not want. We need a phase margin of minimum 45 degrees for a smooth response. So we try to make it a single pole system by moving the first pole or dominant pole to left which throws the second pole after 0dB since there will be a decay of 20db/decade after every pole. We are going to increase the output capacitance of the diff-amp to move the pole leftwards(decrease the value of dominant pole).
We make it a single pole system using a miller theorem(a feedback capacitor is used to split the capacitance into a high input capacitance and low output capacitance) between the input and output node of the CS amplifier. Which increases the output capacitance of the differential amplifier and throws the second pole below 0bB in bode plot. So the transfer function of the circuit has only one pole. Hence we can have a sufficient phase margin in the design.

The design specifications are as follows:

| Specifications | |
|---|---|
| Vdd | 1.8V |
| DC gain | 70dB |
| Gain bandwidth product | 30Mhz |
| Phase margin > | 60degree |
| Slew rate | 20 V/usec |
| ICMR(+) | 1.6V |
| ICMR(-) | 0.8V |
| C(load) | 2pF |
| Power | 0.3nW |

Fig. 1. Schematic



According to the specifications, we biased the transistors. Using Phase margin we derived the relation between the capacitive load and the miller capacitor.
Cc $->$ miller capacitor.
Cl $->$ Load capacitor.

$$Cc \geq 0.22 * Cl$$

Hence we choose a miller capcitor of 800fF. Since at extreme end the current through the MOSFET1 is flowing from miller capacitor hence using slew rate(slew rate is given by rate of change of output voltage), we can calculate the amount of biasing current.

$$SR = I/C$$

I is given by 20uA. All the mosfet are to be saturation in order to work as an amplifier.Hence using the conditions of saturation and the values of ICMR(+) and ICMR(-) we can calculate the W/L ratio of MOSFETs in current mirrors(M3, M4, M5, M8). And M1 and M2(where the inputs are given) is biased using gain bandwidth product. And the CS amplifier is biased using the biasing current and biasing of other components. We implemented the design in cadence and analyzed the circuit to know whether the proposed circuit is meeting it's design specifications or not.

## III. Results

### A. Theoretical Analysis

By theoretical calculation(using the values of DC analysis) we got gain at v(common mode)=0.8 gain = 68.3dB and at 1.6v(common mode) gain = 69dB. We get the DC power dissipation = 0.00028203860 w

| V = 0.8 v | |
|---|---|
| Gain of 1st stage | 38.27dB |
| Gain of 2nd stage | 30.07dB |
| Total | 68.3dB |

| V = 1.6 v | |
|---|---|
| Gain of 1st stage | 35.02dB |
| Gain of 2nd stage | 34.39dB |
| Total | 69dB |

### B. Practical Analysis

We gave a small ac magnitude of 1v to one end of the diff-amp by changing the common mode(v) of both the inputs 0.8 and 1.6.In simulation, first we did DC analysis to check whether all the MOSFETs are in saturation or not and not down the operating point.Then we did AC analysis to check the gain and phase of the circuit and we did a transient analysis just to make sure that the circuit is amplifying the difference of input or not. The results are shown below.By looking at the graph we can see that our theoretical and practical values are almost same. And the phase margin at 0dB gain GBW in the plots we got GBW is 28MHz which almost same as the specifications. The phase margin is around 59 degrees in both the cases. Finally, the gain is around 68 dB in both the cases.

| Power | 0.00028203860 w |
|---|---|

Fig. 2. Power Analysis

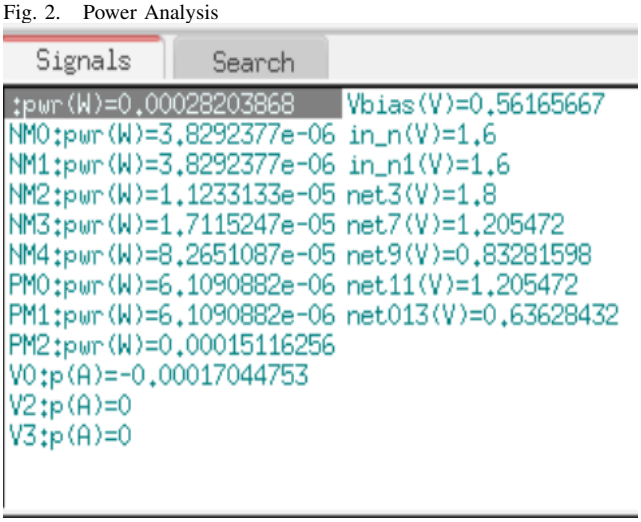



Fig. 3. AC response(Gain and phase) at v=0.8v

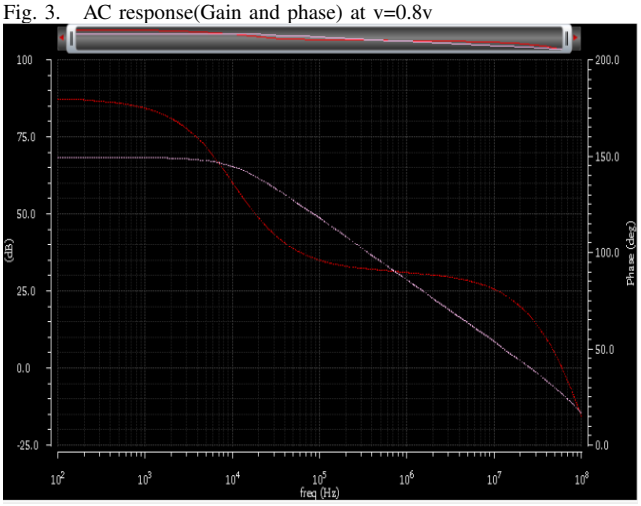



Fig. 4. AC response(Gain and phase) at v=1.6v

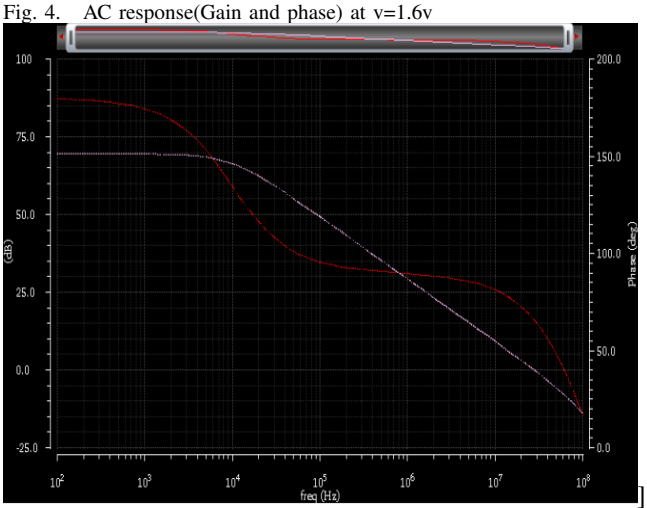
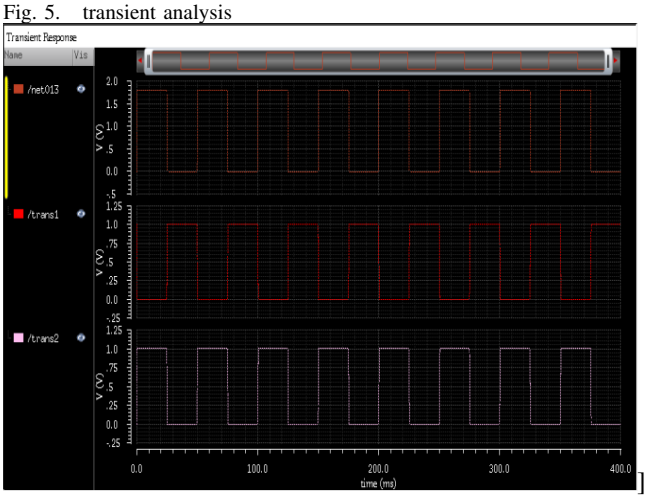


Fig. 5. transient analysis




## IV. Conclusion

As we can see in transient analysis, the output is the amplified signal of the difference in inputs if the input1 $>$ input2 else it's zero and the power consumed by the circuit is 282uWatt.

## References

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[3] S. U. Ay,( 2011) A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS, Int.J. Analog Integr. Circuits Signal Process.