

**Physical Design(PD):** The design software that I used for physical design is '*Cadence encounter*'.

- The design is made for two different floor plans
  - 0.5 - cell utilization - Large die area.
  - 0.8 - cell utilization - Small die area.

### **Cell utilization(0.5)**

- Before Placement:

- Worst timing path - Setup time:

```
=====
-----
          timeDesign Summary
-----
+-----+-----+-----+-----+-----+
|   Setup mode   | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+-----+-----+-----+-----+
|      WNS (ns):| 1.075 | 8.851 | 1.075 | 4.654 | N/A | N/A |
|      TNS (ns):| 0.000 | 0.000 | 0.000 | 0.000 | N/A | N/A |
| Violating Paths:| 0 | 0 | 0 | 0 | N/A | N/A |
| All Paths:| 25 | 16 | 20 | 1 | N/A | N/A |
+-----+-----+-----+-----+-----+
```

Density: 0.000%

```
=====
-----'
```

We can see that the Worst negative slack(WNS) in the pre-placement timing report is positive that implies the pass is not getting failed and the total negative slack(TNS) is 0 which implies that the the design meets timing(if TNS is positive that implies a negative slack in the design since the TNS is the sum of all WNS).

- Area of the design:

```
=====
-----Gate area 2.2707 um^2
-----
```

Level 0 Module SerialParallel

Gates= 183 Cells= 49

Area= 416.3 um^2
-----

As we can see from the report the total number of gates used in the design in pre-placement is 183 Cells and each cell is of  $2.2707 \text{ um}^2$  which implies the total area as  $183 * 2.707 \text{ um}^2 = 416.3 \text{ um}^2$ .

- Power of the design:
- 
- 

Cell	Internal Power	Switching Power	Total Power	Leakage Power
Total ( 49 of 49 )	0.0329	0.002201	0.03739	0.002284

---

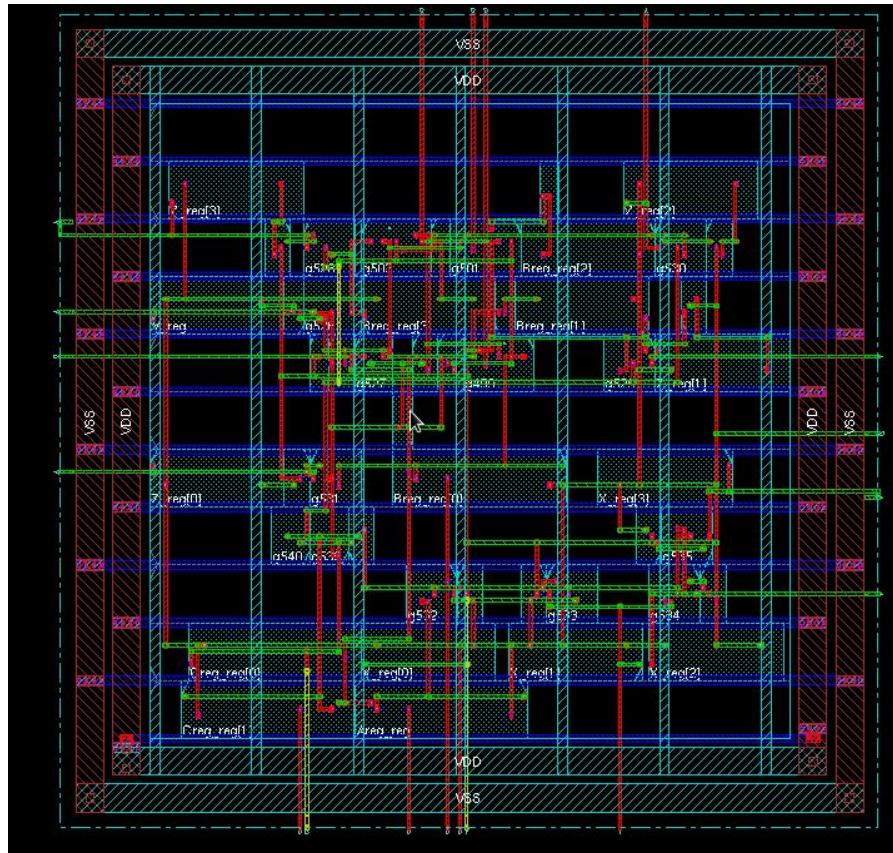


---

The above is the final report of power in pre-placement. We can see the total power is coming out to be 0.03739mW.

- After placement:

- Layout after the placement:



- Timing report:

```
=====
```

```
-----  
timeDesign Summary  
-----
```

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.977	8.758	0.977	4.642	N/A	N/A
TNS (ns):	0.000	0.000	0.000	0.000	N/A	N/A
Violating Paths:	0	0	0	0	N/A	N/A
All Paths:	25	16	20	1	N/A	N/A

DRVs	Real		Total	
	Nr nets(terms)	Worst Vio	Nr nets(terms)	
max_cap	0 (0)	0.000	0 (0)	
max_tran	0 (0)	0.000	0 (0)	
max_fanout	0 (0)	0	0 (0)	
max_length	0 (0)	0	0 (0)	

Density: 50.000%

Routing Overflow: 0.00% H and 0.00% V

```
=====
```

```
-----  
timeDesign Summary  
-----
```

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.296	0.296	7.953	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	24	16	11	N/A	N/A	N/A

Density: 50.000%

Routing Overflow: 0.00% H and 0.00% V

---

We can see that in the setup mode and hold mode the worst case slack is positive and TNS is zero. We can see the density is increased to 50% from the previous reports which is 0% since the the placement is done the density is increased to some extent.

- Area of the design:

---

Gate area 2.2707 um <sup>2</sup>	Gates= 183 Cells=
Level 0 Module SerialParallel	
49 Area= 416.3 um <sup>2</sup>	

---

The area of the design is not changed yet because the number of gates are still the same after placing the cells and no cells/gates are added in the design that are not preexisting. The calculation are the same in the above part.

- Power of the design:

---

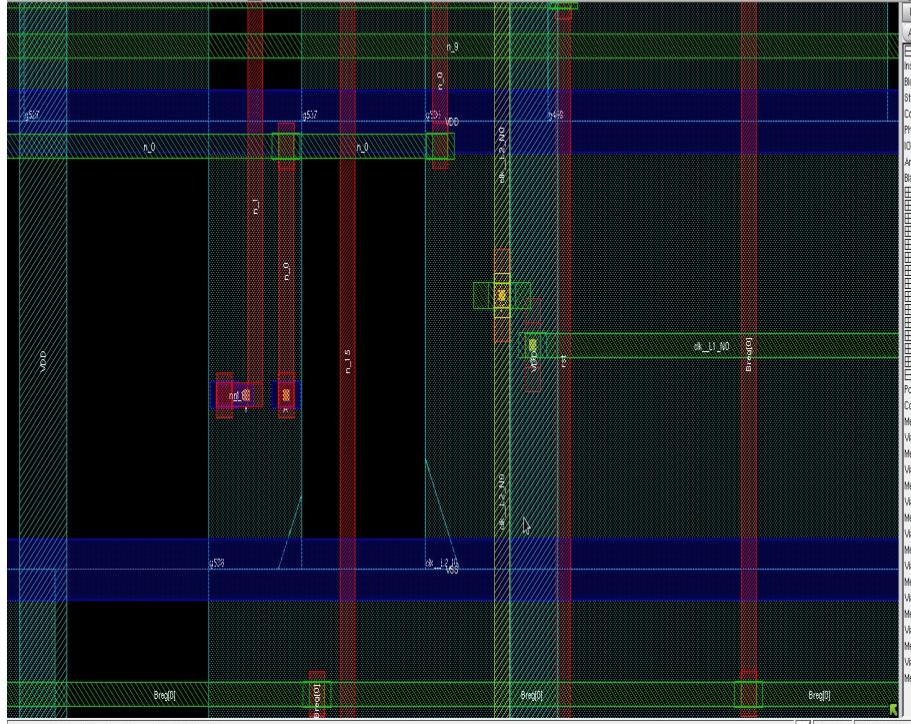
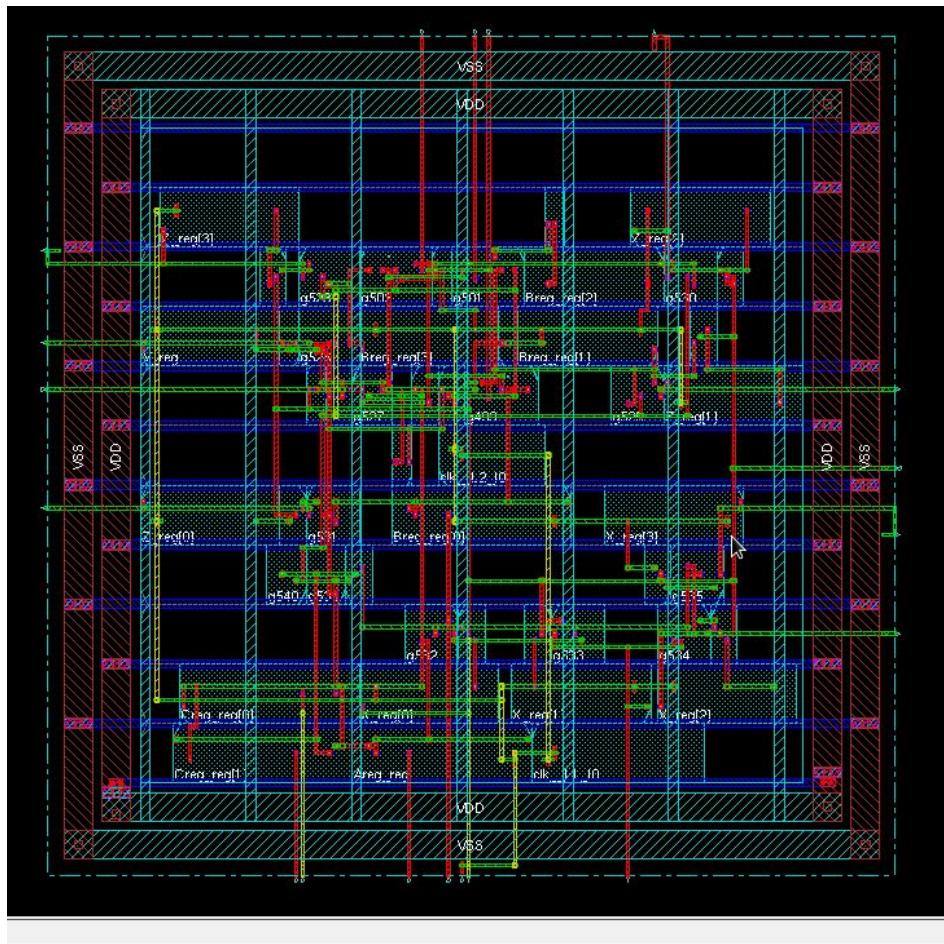
Cell	Internal Power	Switching Power	Total Power	Leakage Power
Total ( 49 of 49 )	0.03294	0.002657	0.03788	0.002284

---

The power of the design is also not changed much except for the switching power, which is increased a bit after placing of cell due to it might be considering the ideal case in the earlier part.

- After CTS:

- Layout:



*Difference:* As we can see from the previous the above layout the yellow colored clock tree is added and visible in the layout above.

- Timing analysis:

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	1.005	8.770	1.005	4.625	N/A	N/A
TNS (ns):	0.000	0.000	0.000	0.000	N/A	N/A
Violating Paths:	0	0	0	0	N/A	N/A
All Paths:	25	16	20	1	N/A	N/A

DRVs	Real		Total	
	Nr nets(terms)	Worst Vio	Nr nets(terms)	
max_cap	0 (0)	0.000	0 (0)	
max_tran	0 (0)	0.000	0 (0)	
max_fanout	0 (0)	0	0 (0)	
max_length	0 (0)	0	0 (0)	

Density: 53.818%

Routing Overflow: 0.00% H and 0.00% V

---

#### timeDesign Summary

---

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.284	0.284	7.924	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	24	16	11	N/A	N/A	N/A

Density: 53.818%

Routing Overflow: 0.00% H and 0.00% V

---

The slack is almost the same same in the above timing report. The density of the design is a bit increased in this case since the clock tree is added to the design.

- Area of the design:
- 

Gate area 2.2707 um<sup>2</sup>  
Level 0 Module SerialParallel  
Area= 448.1 um<sup>2</sup>

---

The number of cells has increased in the clock tree synthesis this is because there might be addition of clock buffers and inverters for clock slew requirements and few gates to in the CTS which increased the area to 448.1um<sup>2</sup>.

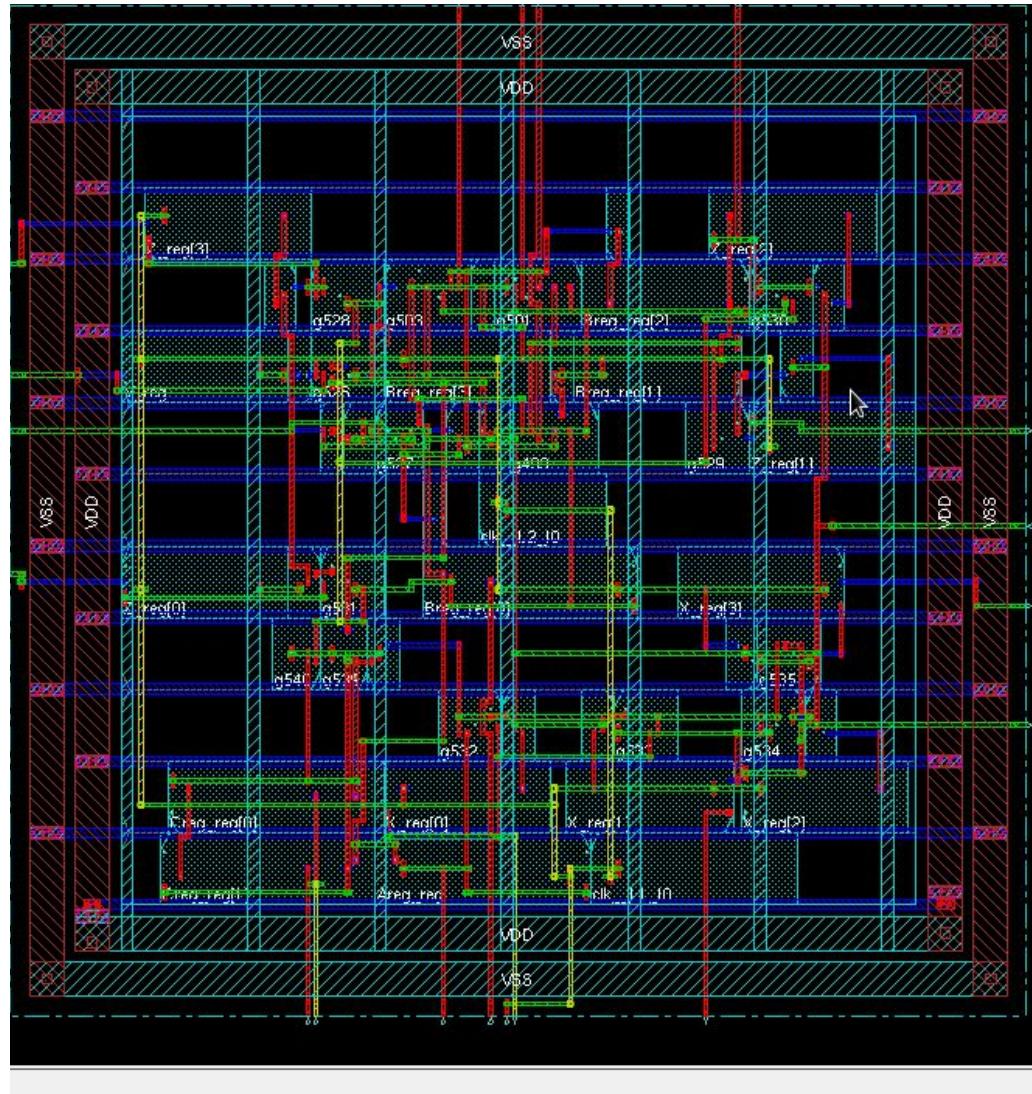
- Power of the design:

Cell	Internal Power	Switching Power	Total Power	Leakage Power
<hr/>				
Total ( 51 of 51 )	0.0457	0.008323	0.05671	0.002686

The total power of the design is obviously increased due the increase in the number of cells(internal power of the design increases due to increase in the number of cell) and hence increasing the total power to 0.0567um<sup>2</sup>.

- Post routing:

- Layout:



If we observe clearly light blue color routing wires is visible in the layout this shows that the routing is done.

- Timing report:

---

#### timeDesign Summary

---

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.958	8.727	0.958	4.630	N/A	N/A
TNS (ns):	0.000	0.000	0.000	0.000	N/A	N/A
Violating Paths:	0	0	0	0	N/A	N/A
All Paths:	25	16	20	1	N/A	N/A

DRVs	Real	Total	
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 53.818%

---



---

#### timeDesign Summary

---

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.283	0.283	7.930	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	24	16	11	N/A	N/A	N/A

Density: 53.818%

---

After the completion of routing the final WNS that is coming out is positive and the design is successfully made. And the density is same as the above step since only wiring is done which is not much dependant of the density.

- Area of the design:

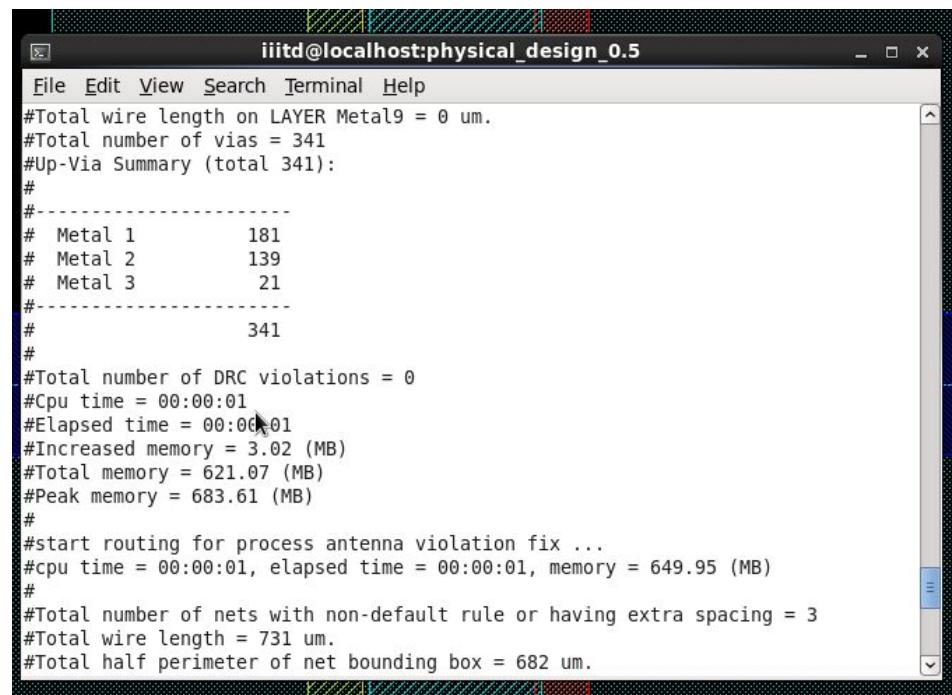
Gate area 2.2707 um<sup>2</sup>

Level 0 Module SerialParallel	Gates= 197 Cells= 51
Area= 448.1 um <sup>2</sup>	

- Power of the design:
-

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
Total ( 51 of 51 ) 0.0457 0.00833 0.05671 0.002686					

Area and power of the design doesn't effect much with the routing since only connection of cells is done no cells are added in the design. During the routing is done the DRC is automatically checked for the design and from the picture below we can see that there are no DRC and antenna violation error in the design.



```

iiitd@localhost:physical_design_0.5
File Edit View Search Terminal Help
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 341
#Up-Via Summary (total 341):
#
#-----
# Metal 1      181
# Metal 2      139
# Metal 3       21
#-----
#                  341
#
#Total number of DRC violations = 0
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 3.02 (MB)
#Total memory = 621.07 (MB)
#Peak memory = 683.61 (MB)
#
#start routing for process antenna violation fix ...
#cpu time = 00:00:01, elapsed time = 00:00:01, memory = 649.95 (MB)
#
#Total number of nets with non-default rule or having extra spacing = 3
#Total wire length = 731 um.
#Total half perimeter of net bounding box = 682 um.

```

### Cell utilization(0.8)

Similarly as explained in the 0.5 utilization steps I evaluated the design in the different stages of the design. The report are coming out to be the following:

- Before placement
  - Timing report:

---



---

timeDesign Summary

---

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	1.075	8.851	1.075	4.654	N/A	N/A
TNS (ns):	0.000	0.000	0.000	0.000	N/A	N/A
Violating Paths:	0	0	0	0	N/A	N/A
All Paths:	25	16	20	1	N/A	N/A

Density: 0.000%

---



---



---

- Area of the design:
- 
- 

Gate area 2.2707 um<sup>2</sup>

Level 0 Module SerialParallel	Gates= 183 Cells=
49 Area= 416.3 um <sup>2</sup>	

---



---

- Power of the design:
- 
- 

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
------	----------------	-----------------	-------------	---------------	-----------

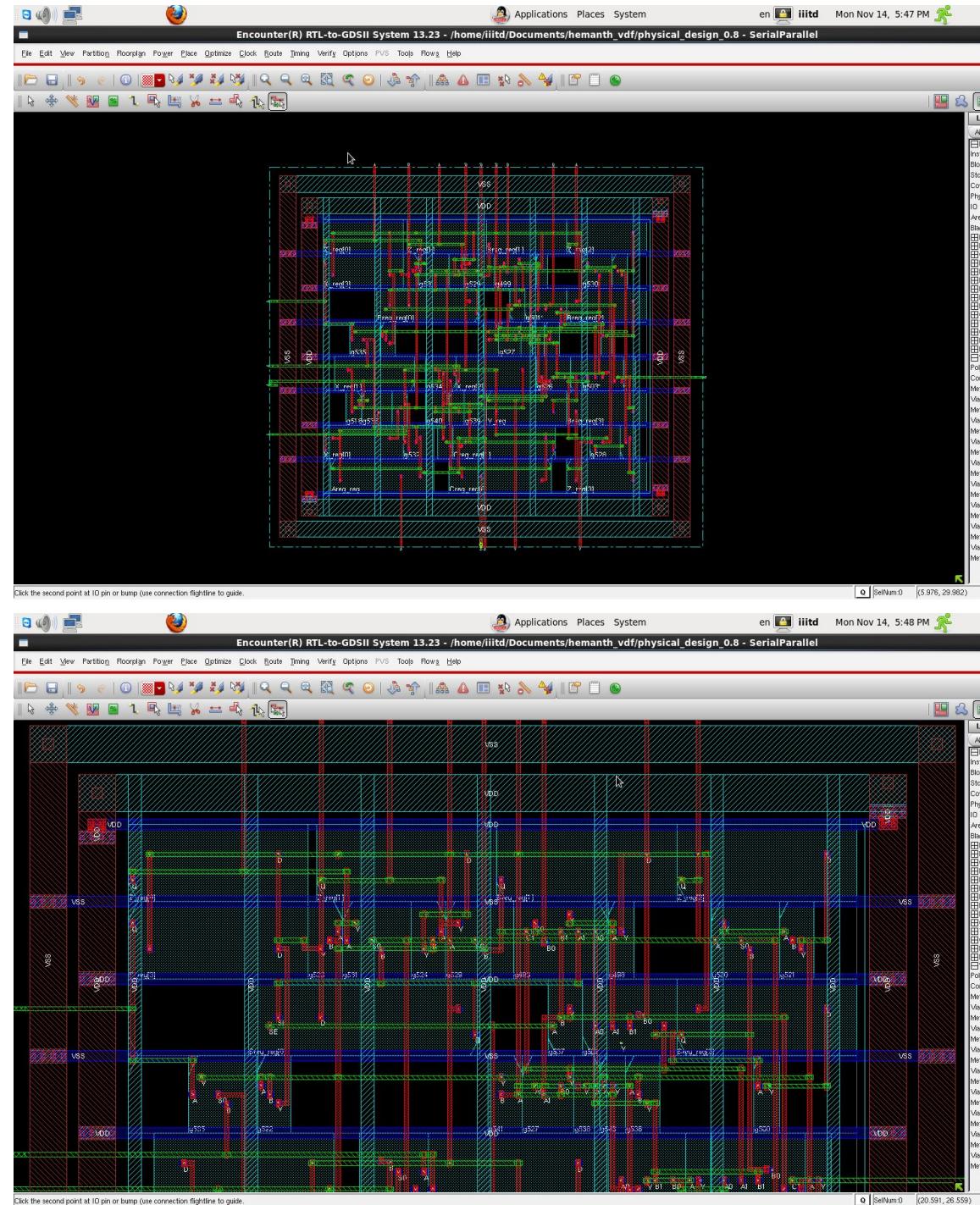
---

Total ( 49 of 49 )	0.0329	0.002201	0.03739	0.002284
--------------------	--------	----------	---------	----------

---

- After placement

- Layout



A zoomed version of the layout before placement is clearly with power grids and strips and cell placement.

- Timing report:
- 
-

### timeDesign Summary

---

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.952	8.773	0.952	4.636	N/A	N/A
TNS (ns):	0.000	0.000	0.000	0.000	N/A	N/A
Violating Paths:	0	0	0	0	N/A	N/A
All Paths:	25	16	20	1	N/A	N/A

	Real	Total	
DRVs			
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 80.882%

Routing Overflow: 0.00% H and 0.00% V

---

---

### timeDesign Summary

---

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.292	0.292	7.953	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	24	16	11	N/A	N/A	N/A

Density: 80.882%

Routing Overflow: 0.00% H and 0.00% V

---

We can see the slack is positive and TNS is zero hence the design is valid.

- Area of the design:

Gate area 2.2707  $\mu\text{m}^2$

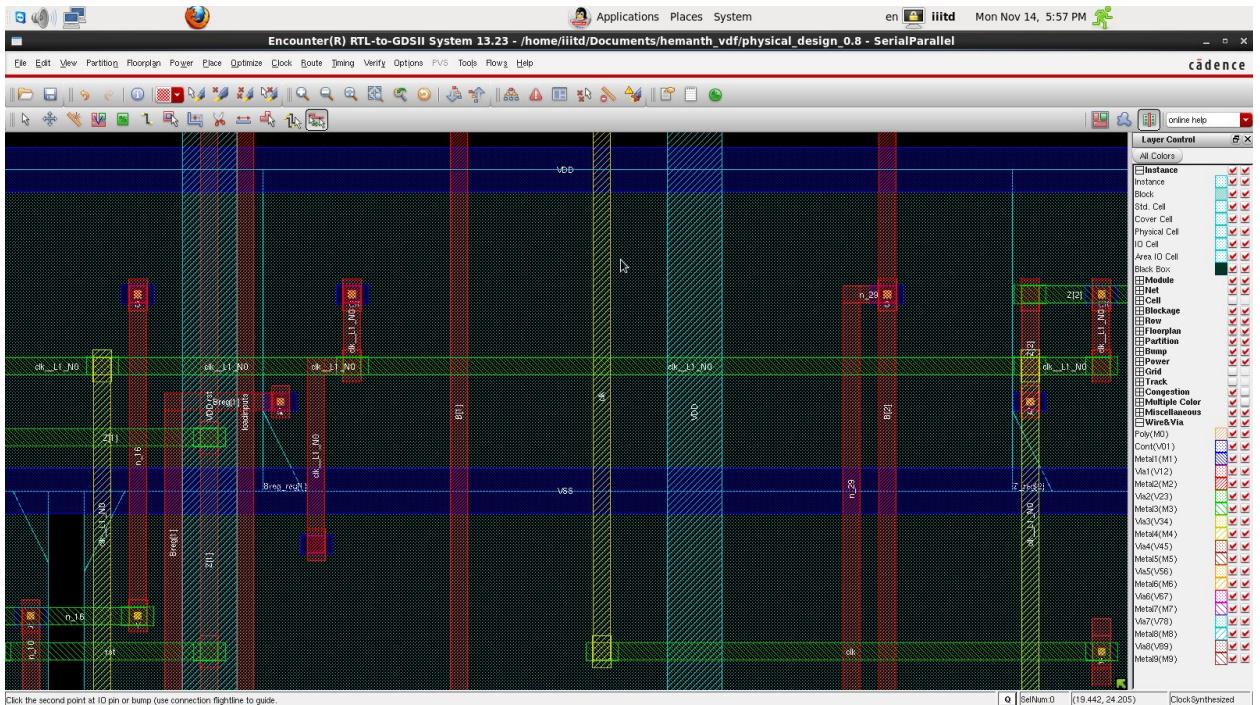
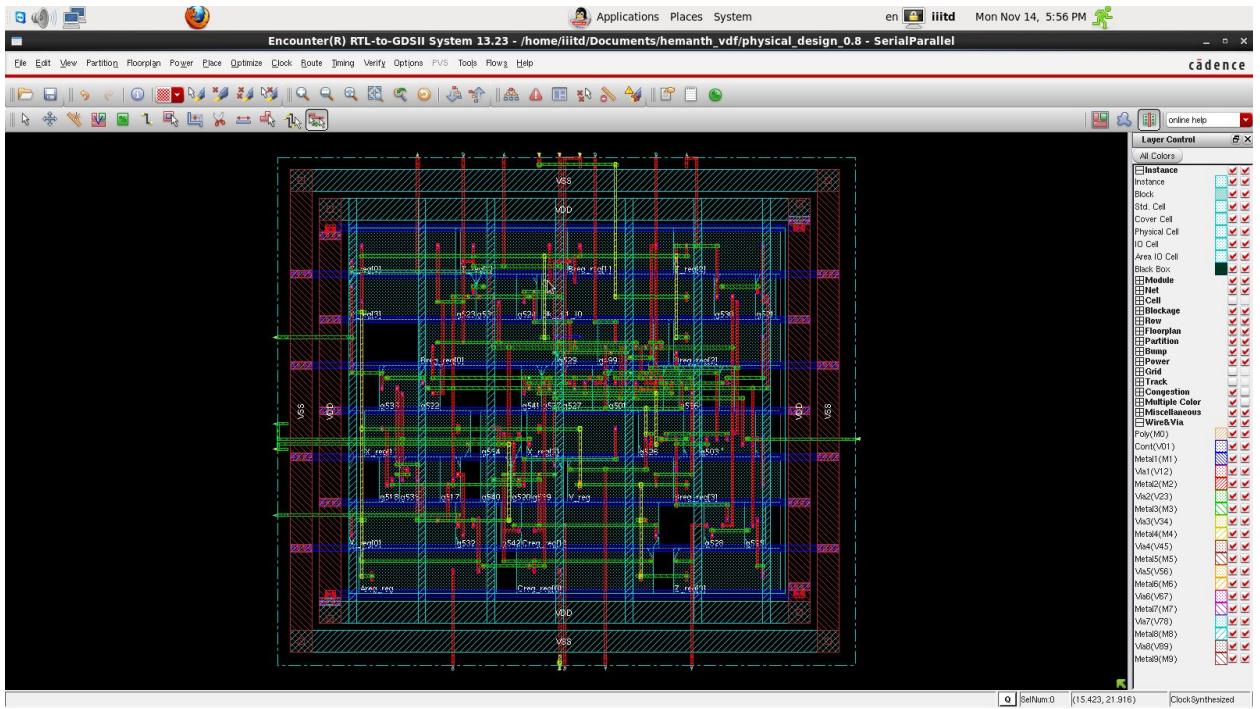
- #### ○ Power of the design:

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
------	----------------	-----------------	-------------	---------------	-----------

Total ( 49 of 49 ) 0.03294 0.002702 0.03792 0.00228

- After CTS:

- Layout:



- Timing report:

---



---

### timeDesign Summary

---

Setup mode	all	reg2reg	in2reg	reg2out	in2out	
clkgate						
WNS (ns):	1.025	8.779	1.025	4.575	N/A	
N/A						
TNS (ns):	0.000	0.000	0.000	0.000	N/A	N/A
Violating Paths:	0	0	0	0	N/A	N/A
All Paths:	25	16	20	1	N/A	N/A

	Real	Total	
DRVs			
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 85.882%

Routing Overflow: 0.00% H and 0.00% V

---

#### timeDesign Summary

---

Hold mode	all	reg2reg	in2reg	reg2out	in2out	
clkgate						
WNS (ns):	0.280	0.280	7.879	N/A	N/A	
N/A						
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	24	16	11	N/A	N/A	N/A

Density: 85.882%  
Routing Overflow: 0.00% H and 0.00% V

- #### ○ Area of the design:

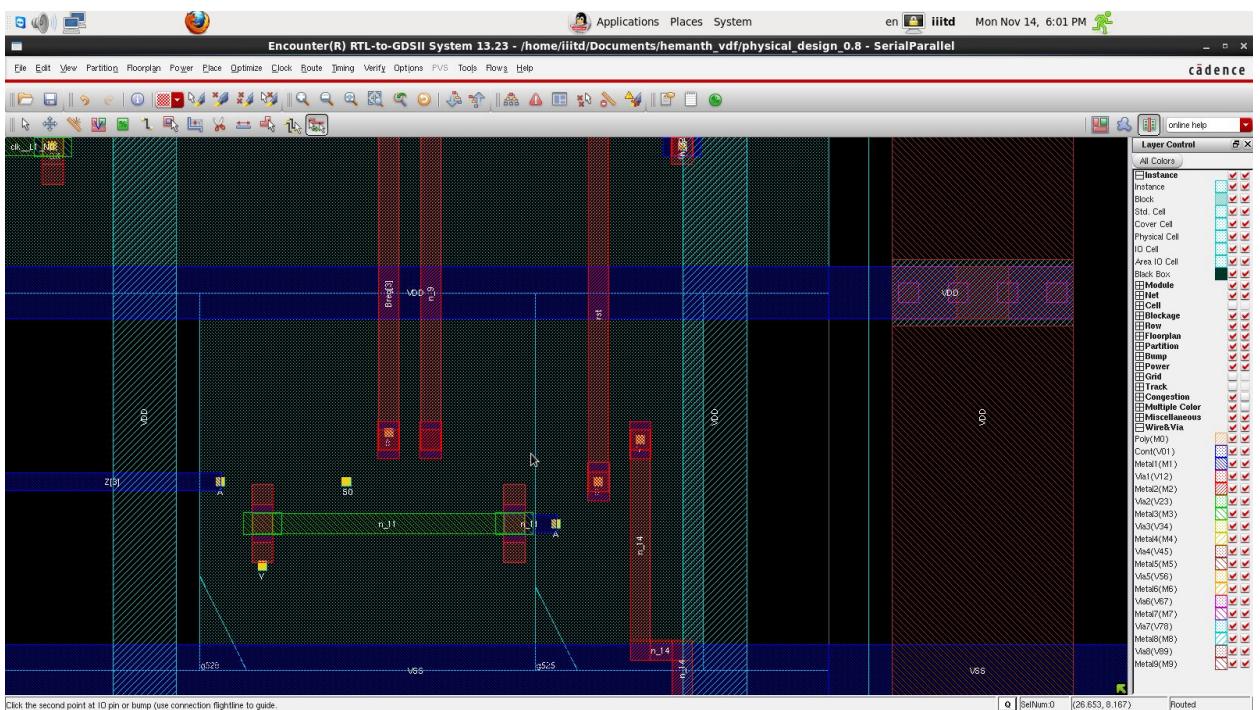
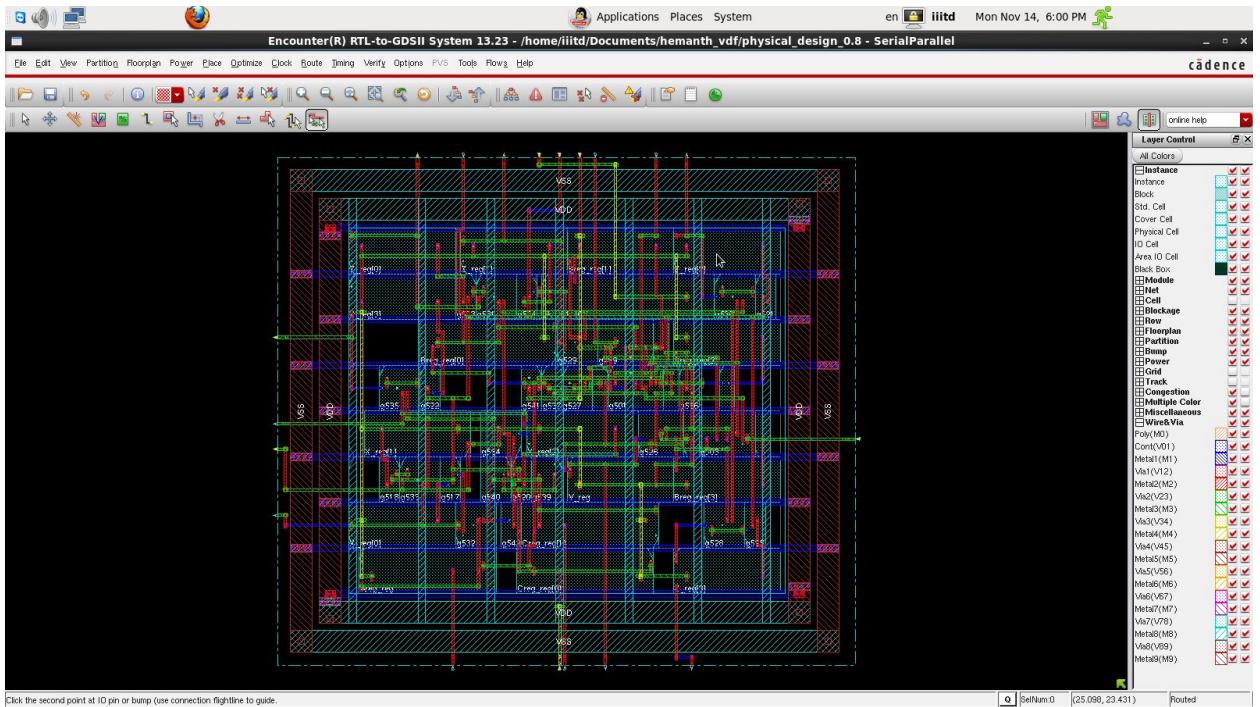
Gate area 2.2707 um<sup>2</sup>

- ### ○ Power of the design:

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
<hr/>					
Total ( 50 of 50 )	0.04533	0.00555	0.05353	0.002651	

- Post route:

- Layout:



- Timing report:

---

timeDesign Summary

---

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.989	8.724	0.989	4.582	N/A	N/A
TNS (ns):	0.000	0.000	0.000	0.000	N/A	N/A
Violating Paths:	0	0	0	0	N/A	N/A
All Paths:	25	16	20	1	N/A	N/A

	Real	Total	
DRVs	+-----+	+-----+	
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 85.882%

---



---

### timeDesign Summary

---

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.277	0.277	7.886	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	24	16	11	N/A	N/A	N/A

Density: 85.882%

---



---

- o Area of the report:
- 
- 

Gate area 2.2707 um<sup>2</sup>

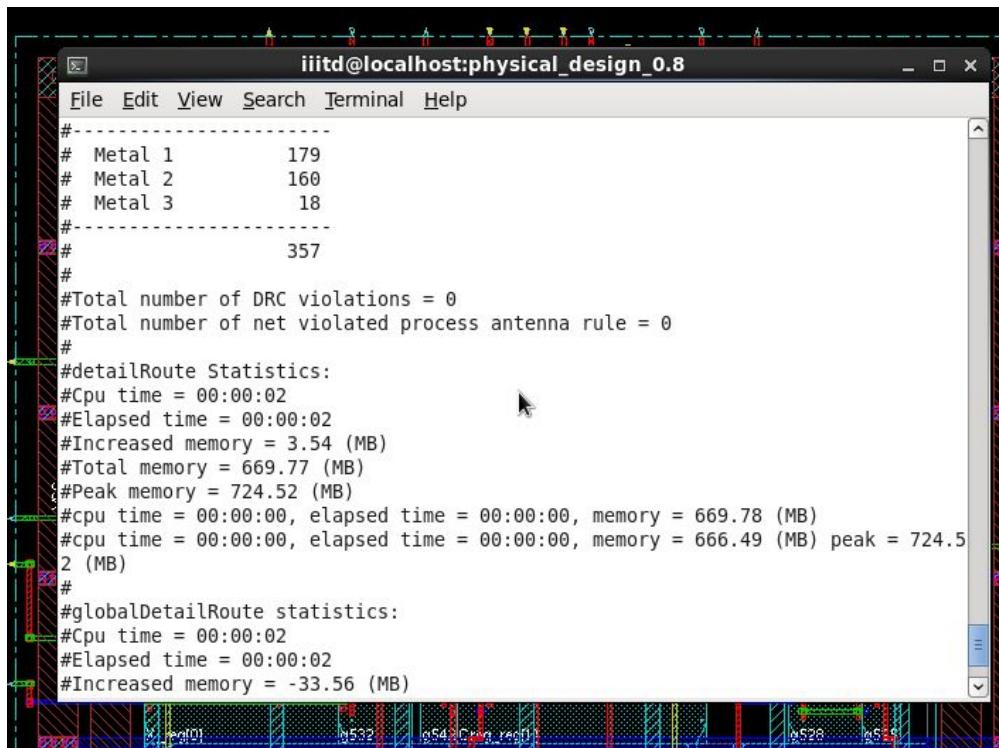
```

Level 0 Module SerialParallel           Gates=      194 Cells=
50 Area=    442.0 um^2
=====
o Power of the report:
=====

-----
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
Total ( 50 of 50 )	0.04533	0.00552	0.0535	0.002651	

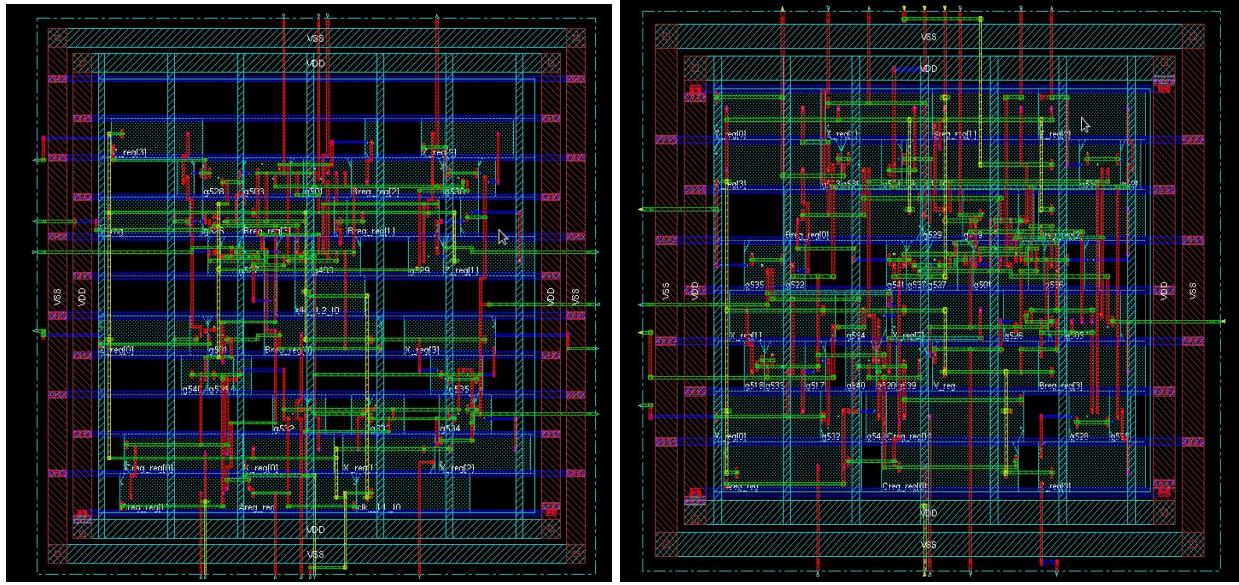
During the routing is done the DRC is automatically checked for the design and from the picture below we can see that there are no DRC and antenna violation error in the design.



```

iiitd@localhost:physical_design_0.8
File Edit View Search Terminal Help
#-----
# Metal 1      179
# Metal 2      160
# Metal 3       18
#
#          357
#
#Total number of DRC violations = 0
#Total number of net violated process antenna rule = 0
#
#detailRoute Statistics:
#Cpu time = 00:00:02
#Elapsed time = 00:00:02
#Increased memory = 3.54 (MB)
#Total memory = 669.77 (MB)
#Peak memory = 724.52 (MB)
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 669.78 (MB)
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 666.49 (MB) peak = 724.5
2 (MB)
#
#globaDetailRoute statistics:
#Cpu time = 00:00:02
#Elapsed time = 00:00:02
#Increased memory = -33.56 (MB)
```

**Change in floor plan:** Cell utilization if basically the area occupied by the standard cells and hard macros(wiring and interconnects data). In the case of 0.5 we have large die area hence the density if the design is lesser and for 0.8 we have small die making the density to 80%. We have Density of the design changed from 50% to 80% since the die size is less in the 0.8 case. And if we compare the the layout after the post routing:



As we can see from the above layout the right layout(0.8) after post routing looks compact/more occupied than the left layout(0.5) since the density of the design is 80 and 50 respectively. The power of the design is almost the same and the number of cell after the post routing is a bit less in the 0.8 case that may be because for the less area available some optimization is done by minimizing the cells. Coming to the routing part it becomes more flexible in the case of 0.8 design since we have more area for the placing and routing the design than the 0.5 since the components are widely placed in the case of 0.8 hence making the routability more easier in this case.