**Seat No:_____** **Enrollment No:_____**

# PARUL UNIVERSITY

## FACULTY OF ENGINEERING & TECHNOLOGY

**B.Tech. Winter 2016 - 17 Examination**

**Semester: 3** **Date: 19-12-2016**
**Subject Code: 03107203** **Time: 10:00AM to 01:00PM**
**Subject Name: Digital Electronics** **Total Marks: 100**

**Instructions:**
1. Attempt all questions from each section.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Write section-A, section-B on separate answer sheets.

**SECTION: A**

**Q:1** ( a) Convert following Numbers as directed **(05)**

(i) $(101001011)_2 = (\ )_{10}$ (ii) $(225.225)_{10} = (\ )_8$

(iii) $(\ 7654\ )_{10} = (\ )_{BCD}$ ( iv) $(\ F28)_{16} = (\ )_{10}$ ( v ) $(\ 414)_8 = (\ )_{16}$

**Q:1** (b) (1) Perform subtractions with the following binary numbers using 2′ s complement **(05)**
(i) 10010 - 10011 (ii) 100 -110000

(2) Find 10's complement of following nos. ( i) 3405.65, (ii) 87.76

**Q:2** (a) Explain De Morgan's theorems in detail. **(07)**

**Q:2** (b) Construct 4*16 Decoder with help of 2*4 Decoder. **(07)**

**OR**

**Q:2** (b) Simplify the function using K-Map and implement with only NOR gates **(07)**

F( w,x,y,z) = Σm( 1 , 3 , 7 , 11 , 15 ) with don't care conditions

d( w,x,y,z ) = Σm( 0, 2 ,5 )

**Q:3** (a) Design Combinational Circuits for Binary to Gray Code Conversion **(07)**

**Q:3** (b) Reduce given expression by using Quine McClusy Method to find Prime Implicants **(06)**
F(a,b,c,d)= ∑m( 0,1,2,5,6,7,8,9,10,14)

**OR**

**Q:3** (b) Design BCD to Excess-3 code converter using minimum number of NAND gates. **(06)**

**Q:4** (a) Explain Half Adder and Full Adder in detail and also Implement a full adder circuit using a decoder and OR gates. **(07)**

**Q:4** (b) What is meant by multiplexer ? Explain with logic diagram and truth table , Operation of 8-to-1 line multiplexer **(06)**

**SECTION: B**

**Q:1** (a) Draw and explain the working of following flip-flops **(05)**
(i) Clocked RS (ii) T-flip-flop

**Q:1** (b) Explain J-K flip-flop with necessary logic diagram, state equation and Truth table. How JK flip-flop is the refinement of RS flip-flop? **(05)**

**Q:2** (a) Design a counter with the following sequence: 0, 4,2,1,6 and repeat. Use JK flip-flop. **(07)**

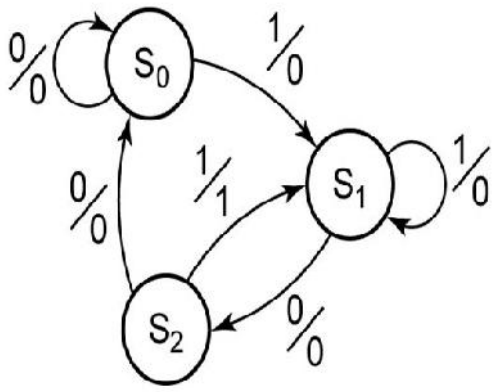
**Q:2** (b) List out 4 different operating modes of Shift Register . And explain in detail SISO & PISO modes. **(06)**

**OR**

**Q:2** (b) Define: State table, State equation, State diagram, input & output equations. **(06)**

**Q:3** (a) Define Odd and Even Parity and Consider 7 digit data as below and convert that data in to Odd Parity Sequence and Even Parity Sequence **(07)**
(i) 0011010 (ii) 0111111 (iii) 0110111 ( iv) 0000100 (v) 1010101

**Q:3** (b) Design Sequence Detector for below State Graph **(06)**




**OR**

(b) Design a 4 bit Binary Counter using D flip flop. **(06)**

**Q:4** (a) Compare RAM , ROM and EPROM and list the different types of PLDs. **(07)**

**Q:4** (b) Reduce the following state table to a minimum number of states and draw reduced state graph. **(07)**

| Input Sequence | Present state | Next state | | Present Output | |
|---|---|---|---|---|---|
| | | X=0 | X=1 | X=0 | X=1 |
| reset | A | B | C | 0 | 0 |
| | | | | | |
| 0 | B | D | E | 0 | 0 |
| 1 | C | F | G | 0 | 0 |
| | | | | | |
| 00 | D | H | I | 0 | 0 |
| 01 | E | J | K | 0 | 0 |
| 10 | F | L | M | 0 | 0 |
| 11 | G | N | P | 0 | 0 |
| | | | | | |
| 000 | H | A | A | 0 | 0 |
| 001 | I | A | A | 0 | 0 |
| 010 | J | A | A | 0 | 1 |
| 011 | K | A | A | 0 | 0 |
| 100 | L | A | A | 0 | 1 |
| 101 | M | A | A | 0 | 0 |
| 110 | N | A | A | 0 | 0 |
| 111 | P | A | A | 0 | 0 |