Seat No:_____ Enrollment No:_____

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech., Summer 2016 - 17 Examination

Semester: 3 **Date: 24/06/2017**
Subject Code: 03107203 **Time: 10 am to 1 pm**
Subject Name: Digital Electronics **Total Marks: 100**

Instructions:
1. Attempt all questions from each section.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Write section-A, section-B on separate answer sheets.

SECTION: A

Q:1 (a) Convert Decimal Number 250.5 to base 3 and base 7. **(05)**

Q:1 (b) Find 1's and 2's complement of following binary nos. $(10001)_2$, $(101011)_2$ **(05)**

Q:2 (a) Implement Boolean function F= x y + x′ y′ + y′ z with OR & NOT gates. **(07)**

Q:2 (b) Define the Integrated Circuit and briefly explain SSI, MSI, LSI and VLSI. **(07)**

OR

Q:2 (b) Give classification of Logic Families and compare CMOS and TTL Families **(07)**

Q:3 (a) Reduce the expression: **(07)**
1. A+B(AC+(B+C')D) 2. (A+(BC)')'(AB'+ABC)

Q:3 (b) Design combinational circuits for a full adder. **(06)**

OR

Q:3 (b) What is meant by multiplexer? Explain with diagram and truth table the Operation of 4-to-1 line multiplexer. **(06)**

Q:4 (a) Simplify Boolean function **(07)**
F =A'B'D'+A'CD+A'BC
d=A'BC'D+ACD+AB'D' Where "d " indicates Don't care conditions.

Q:4 (b) Simplify Boolean function using K-map and draw logic diagram for simplified Boolean function: F(w,x,y,z) = Σ (0,1,2,4,5,6,8,9,12,13,14) **(06)**

SECTION: B

Q:1 (a) Explain operation of Master –Slave J-K Flip-Flop. **(05)**

Q:1 (b) Write excitation table of all types of flip-Flops **(05)**

Q:2 (a) Explain in detail operation of 4 bit Shift Register for all 4 operating modes. **(07)**

Q:2 (b) Compare PLA and PAL. **(06)**

OR

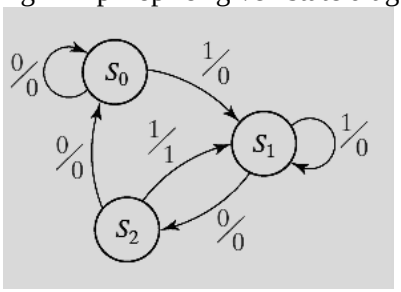
Q:2 (b) Write a short note on FPGA. **(06)**

Q:3 (a) Design a counter with the following binary sequence:0,1,3,7,6,4,and repeat.(Use T flip-flop) **(07)**

Q:3 (b) A sequential circuit has one input (X) and one output (Z). The circuit examines groups of four consecutive inputs and produces an output Z = 1 if the input sequence 0101 or 1001 occurs. The circuit resets after every four inputs. Find the Mealy state graph. **(06)**

OR

Q:3 (b) Design Sequential Circuit using D flip flop for given state diagram. **(06)**



Q:4 (a) Derive the state graph using elimination of redundant state method. (Take appropriate Example.) **(07)**

Q:4 (b) What is the basic difference between synchronous and asynchronous counter? Describe synchronous 3-bit up counter. **(07)**