Seat No: __

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PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B. Tech. Winter 2021 - 22 Examination

Semester: 4th Date: 21/10/2021

Subject Code: 203105253 Time: 10:30am to 1:00pm

Total Marks: 60 Subject Name: Computer Organization & Architecture

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| Inst | ructions: | |
| 1. A | Il questions are compulsory. | |
| | igures to the right indicate full marks. | |
| | Take suitable assumptions wherever necessary. | |
| | tart new question on new page. | |
| | T. C. | |
| 0.1 | Objective Type Questions - (All are compulsory) (Each of one mark) | (15) |
| 1 | The return address of the Sub-routine is pointed to by | (-) |
| _ | | |
| 2 | In interrupts, how does the device identify itself to the processor? | |
| _ | a) By sending its device id b) By sending the machine code for the interrupt service routine | |
| | c) By sending the starting address of the service routine d) None of the mentioned | |
| 3 | The main memory is structured into modules each with its own address register called | |
| | The main memory is structured into installes each with its own address register earlied | |
| 4 | The time lost due to the branch instruction is often referred to as | |
| • | | |
| 5 | LDA Means | |
| | | |
| 6 | The product of 1101 & 1011 is | |
| | The product of 1101 & 1011 is a) 10001111 b) 10101010 c) 11110000 d) 11001100 | |
| 7 | The logic operations are simpler to implement using logic circuits. | |
| | a) True b) False | |
| 8 | In a normal adder circuit, the delay obtained in a generation of the output is | |
| | | |
| 9 | The Master strobes the slave at the end of each clock cycle in Synchronous BUS. | |
| | a) True b) False | |
| 10 | Can a single DMA controller perform operations on two different disks simultaneously? | |
| | a) True b) False | |
| 11 | What functionality of RAM memory prevents it being used for long - term storage? | |
| | A) it is too slow (B) it is unreliable (C) it is volatile (D) it is too bulky | |
| 12 | A symbolic programme is interpreted into binary in | |
| | (a) Directly (b) Three passes. (c) Four passes. (d) Two passes | |
| 13 | If the target operand's value $V(x)$ is contained in the address field, the addressing mode is | |
| | (A) direct (B) indirect (C) implied (D) none of the above | |
| 14 | Ais a binary cell capable of storing information of one bit. | |
| | | |
| 15 | If compared to floating point numbers, arithmetic operations with fixed-point numbers take | |
| | longer to start executing. (a)true (b)false | |
| Q.2 | Answer the following questions. (Attempt any three) | (15) |
| | A) While Execution of program in Basic computer. An Instruction is Stored into IR Register for | |
| | Decoding process. Demonstrate the decoding process with a block diagram | |
| | B) Differentiate between hardwired and micro programmed control unit. | |
| | C) List out different types of addressing modes. | |
| | D) Explain any 2 pipeline hazards in details | |
| Q.3 | A) Design and explain instruction pipeline | (07) |
| - | B) Design flowchart for basic instruction cycle | (08) |
| | OR | . / |
| | B) Design micro programmed control unit. | (08) |
| Q.4 | A) Design Block diagram of hardware for addition and subtraction | (07) |
| - | OR | • |
| | A) Explain any 3-instruction codes. | (07) |
| | B) Explain any 4-arithmetic instruction. | (08) |