Assignment - II

1. Explain about the Design of Micro programme Seaquencer.

The basic components of a micro programmed control unit are the control memeory and the circuit that select the xenext address. The address selection part is called a micro program seaquencer.

There are two multiplexer in the circuit

⇒ The first multiplexer selects an address from one of four sources and routes it into control address register CAR.

⇒ The second multiplexer test the value of a selected status bit and the result of the test is applied to an input logic circuit.

The output from CAR provides the address for the control memory. The content of CAR is incremented and applied to one of the multiplexer inputs and to the subroutine register SBR.

The other three inputs to multiplexer come from

(i) The address field of the present microinstruction

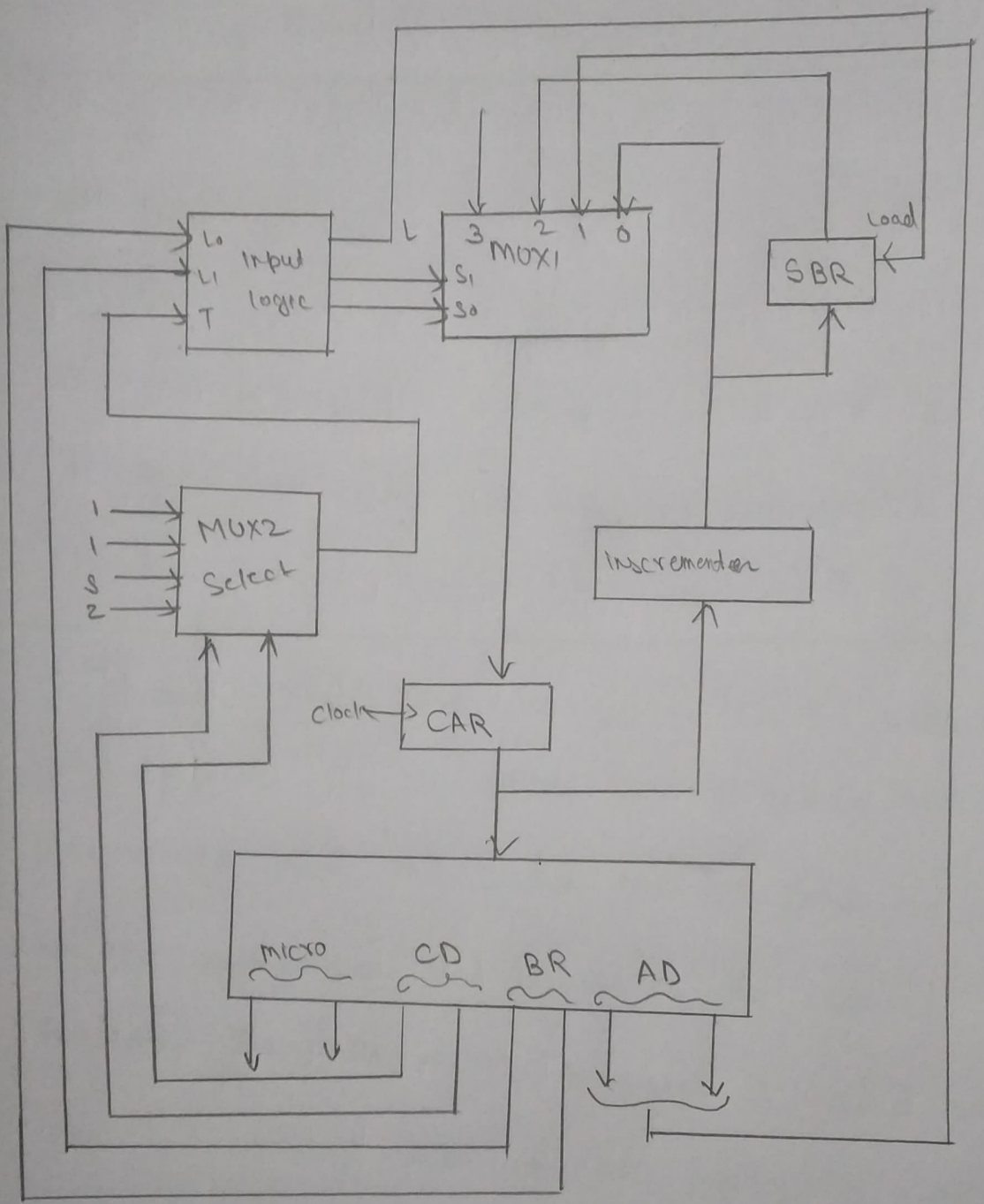
(ii) From the out of SBR

(iii) from an external source that maps the instruction.

The CD (Condition) field of the microinstruction selects one of the status bits in the second multiplexer If the bit selected is equal to 1, the T variable is equal to 1. Otherwise it is equal to 0 The T value together with two bits from the BR (branch) field goes to an input logic circuit. The input logic in a particular sequencer will determine the type of operation that are available in the unit

The input logic circuit in below figure has three input I_0 I_1 and T and three output S_0, S_1 and L. variable S_0 and S_1 select one of the source addresses for CAR. variable L enable the load input in SBR The binary values of selection variables determine the path in the multiplexer ~~for~~ example with $S_1, S_0 = 10$ multiplexer input number 2 is selected and

Establishes transfer path from SBR to CAR



Micro program Sequencer for a control memory

The truth table for the input logic circuit is show in table below

P.T.O

BR Field		Input			MUX 1		Load SBR
		I_1	I_0	T	S_1	S_0	
0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0
0	1	0	1	0	0	0	0
0	1	0	1	1	0	1	1
1	0	1	0	X	1	0	0
1	1	1	1	X	1	1	0

Input I_1 and I_0 are identical to the bit values in the BR field. The bit values for S_1 and S_0 are determined from the stated function and the path in the multiplexer that establishes the required transfer. The subroutine register is loaded with the incremented value of CAR during a call microinstruction (BR = 01) provided that the status bit condition is satisfied (T=1)

2 What are mapping procedures? Explain

Memory mapping

⇒ Direct mapping In cache memory, each block of main memory maps to only cache line.

⇒ Associative mapping Any block of main memory can be loaded into any line of the cache it reduces conflicts but requires more complex hardware to check all cache lines.

⇒ Set-Associative mapping A compromise between direct and associative mapping. the cache is divided into sets, and each block maps to any line within a specific set.

Virtual memory mapping

⇒ paging Divides virtual memory into fixed size pages and physical memory into frames pages are mapped to frames allowing non-contiguous memory allocation and efficient use of physical memory.

⇒ segmentation Divides memory into segments based on logical division like function or data structure each segment has a base address and limit.

Input/output mapping

⇒ Memory mapped I/O. I/O devices are mapped into the address space of the processor allowing the same instruction used for accessing memory ~~for~~ to be used for I/O operations.

File mapping

⇒ Memory mapped files maps the contents of a file into the virtual memory space of a process. This allows a file to be accessed as it it were part of the program's memory enabling efficent file manipulation.

Address mapping

⇒ Logical to physical Address mapping converts logical address generated by the CPO to physical addresses in memory. This mapping is managed by the memory management unit (MMU).

Instruction mapping

⇒ opcode mapping Translate high-level machine instructions into low level operations or micro operation exection executed by the processor's control unit.

3. What about Booth multiplication Algorithm using flowchart and numerical example.

Booth algorithm requires examination of the multiplier bits and shifting of partial product Prior to the shifting the multiplicand may be added to the partial product, substracted from the partial or left unchanged according to the following rules.

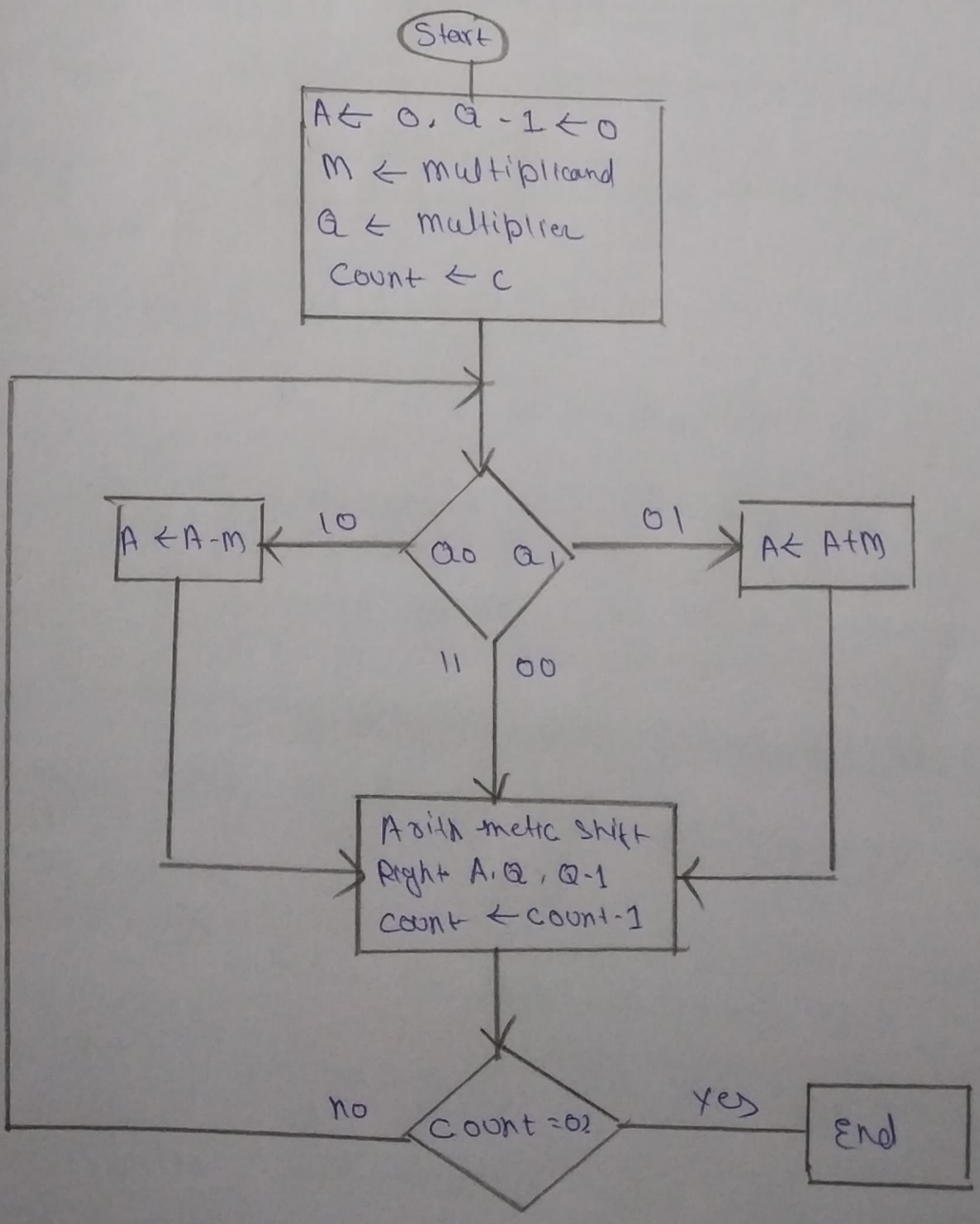
⇒ The multiplicand is subtracted from partial product upon encountering the first least significant 1 in a string of 1's in the multiplier.

⇒ The multiplicand is added to the partial product upon encountering the first 0 in a string of 0's in the multiplier.

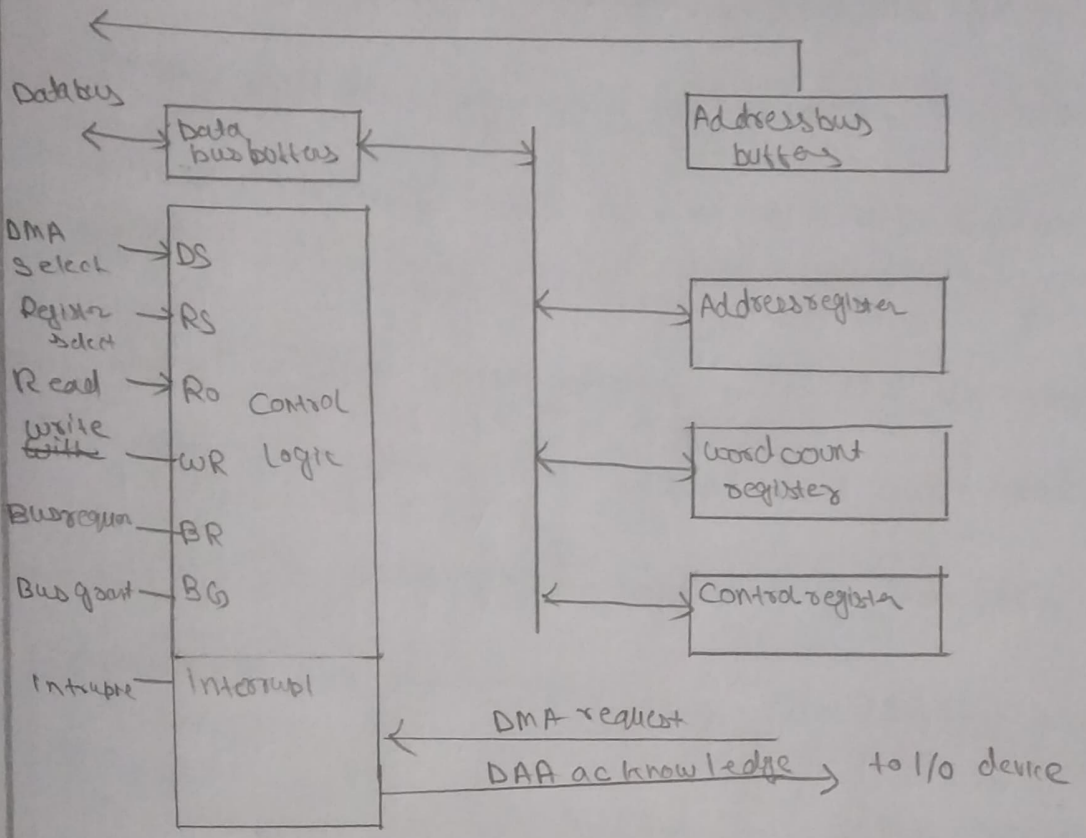
⇒ The partial product does not change when multiplier bit is identical to the previous multiplier bit.

The algorithm works for positive or negative multipliers in 2's complement represention. This is because a negative multiplier ends with a string of 1's and the last operation will be a substraction of the appropriate weight.

The two bits of the multiplier in Qn and Qn+1 are inspected. If the two bits are equal to 10, it means that the first 1 in a string of 1's has been encountered. This requires a subtraction of the multiplicand from the partial product in Ac. If the two bits are equal to 01, it means that the first 0 in a string of 0's has been encountered.



4 Explain the working of DMA Controller



Direct memory ACCESS (DMA)

The unit communicates with the CPU via the data bus and control lines. The registers in the DMA are selected by the CPU through the address bus by enabling the DS (DMA Select) and RS (register select) input the RD (read) and WR (write) input are bidirectional.

When the BG (bus grant) input is 0, the CPU can communicate with the DMA registers throughthe data bus to read from or write to

the DMA registers. When BG = 1, the CPU has relinquished (ceased) the buses and the DMA can communicate directly with the memory by specifying the address bus and activating the RD or WR control.

The DMA communicates with the external peripheral through the request and acknowledge lines by using a prescribed handshaking procedure. The DMA controller has three registers. an address register a word count register. and a control register. The address register contains an address to specify the desired location memory. All registers in the DMA appear to the CPU as I/O interface registers. Thus the CPU can read from or write into the DMA registers under program control via the data bus.

5. What is pipelining ? Explain about Arithmetic pipelining.

Pipelining is the process of accumulating instruction from the processor through a pipeline. It allow storing and executing instruction in an orderly process it is also know as pipeline

Arithmetic pipelining.

Arithmetic pipelines are usually found in most of the computers. They are used for floating point operations, multiplication of fixed point numbers etc for example the input to the floating point Adder pipelines is

$X = A * 2^a$

$Y = B * 2^b$

Here A and B are mantissas (significant digit of floating point number) while, a and b are exponents

The floating point addition and subtraction

Compare the exponents

Align the mantissas

Add or substract mantissas

produce the result.