**CS2100 Assignment #2**

AY2024/25 Semester 1

**Deadline: Monday, 14 October 2024, 1:00pm**

TEMPLATE FOR SUBMISSION

36

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Full name: Tutorial grp: **T**

**Q1.** (Total: 15 marks)

18

Cycle time: ps [4 marks]

55.6

Clock frequency: GHz [3 marks]

11

Time taken for beq instruction: ps [3 marks]

ALU

Optimization: new [5 marks]

Explain your answers below.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Instruction Mem (ps) | Register Read (ps) | ALU  (ps) | Mem Read (ps) | Mem Write (ps) | Register Write (ps) | Total (ps) |
| addi | 5 | 2 | 4 | - | - | 2 | 13 |
| lw | 5 | 2 | 4 | 5 | - | 2 | 18 |
| sw | 5 | 2 | 4 | - | 7 | - | 18 |
| beq | 5 | 2 | 4 | - | - | - | 11 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Instruction | New Register Read (ps) | New  Register Write (ps) | Total with New Reg File (ps) | New ALU  (ps) | Total with New ALU (ps) |
| addi | 1 | 1 | 11 | 2 | 11 |
| lw | 1 | 1 | 16 | 2 | 16 |
| sw | 1 | - | 17 | 2 | 16 |
| beq | 1 | - | 10 | 2 | 9 |

Slowest instructions with longest total execution time are lw and sw, and datapath is single-cycle so they form the critical path and hence Cycle Time = 18 ps.

Clock Frequency (1 / Period)

= 1 / (18 \* 10-12 \* 109)

= 55.6 GHz (3 s.f.)  
Note:

* 10-12 to convert ps to s
* 109 to convert Hz to GHz

New ALU will decrease total execution time of sw and beq instruction more and makes new cycle time 16 ps instead of 17 ps. Hence, I will go for the new ALU.

Note:

* Data Mem (Mem Read and Mem Write, cannot have both concurrently)
* Instruction Mem assumed to take 5 ps like Data Mem (also a mem and performs same operation).

**Q2.** (Total: 5 marks)

Note: Green highlights are Δs

Value of controls signals (X stands for “don’t care”)

RegDst: 0

ALUSrc: X

MemToReg: X

RegWrite: 1

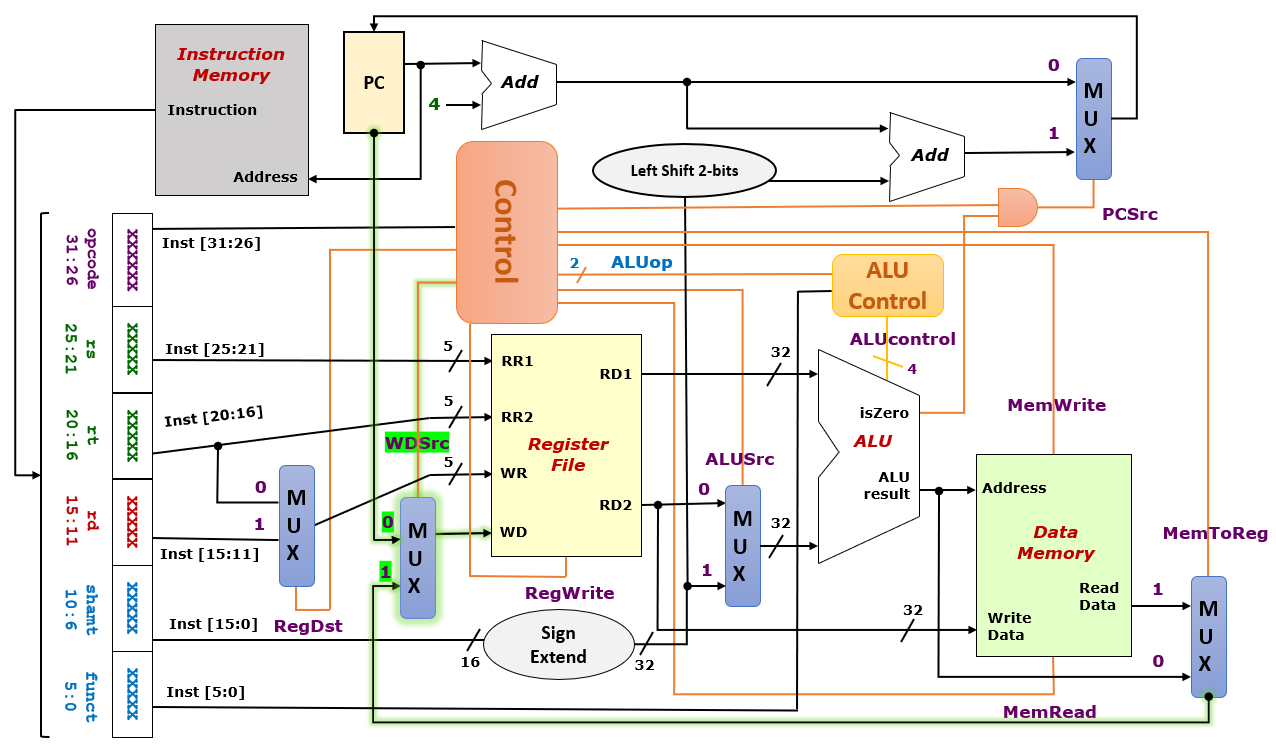
MemRead: 0

MemWrite: 0

PCSrc: 0

WDSrc: 0

ALUop: 00  
ALUcontrol: 0010



The new instruction is given as whatiispc $R where $R is rt in the instruction register since the instruction is of I-format. When the opcode of whatiispc is detected by the Control Unit of the MIPS Processor, the new control signal called WDSrc (stands for “Write Data Source”) will have the value 0 (instead of the value 1 for other instructions that use WD). The new multiplexer will use WDSrc to select the current PC value to store as Write Data (WD), which will then be written into Write Register (WR), which is $R, by the Register File eventually.

**Q3.** (Total: 3 marks)

A + B’ + C’ + D’ + E’ + F’

(a) [1 mark]

A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F

(b) [2 marks]

**Q4.** (Total: 4 marks)

(a) [2 marks]

(b) (1, 5, 8, 12) [2 marks]

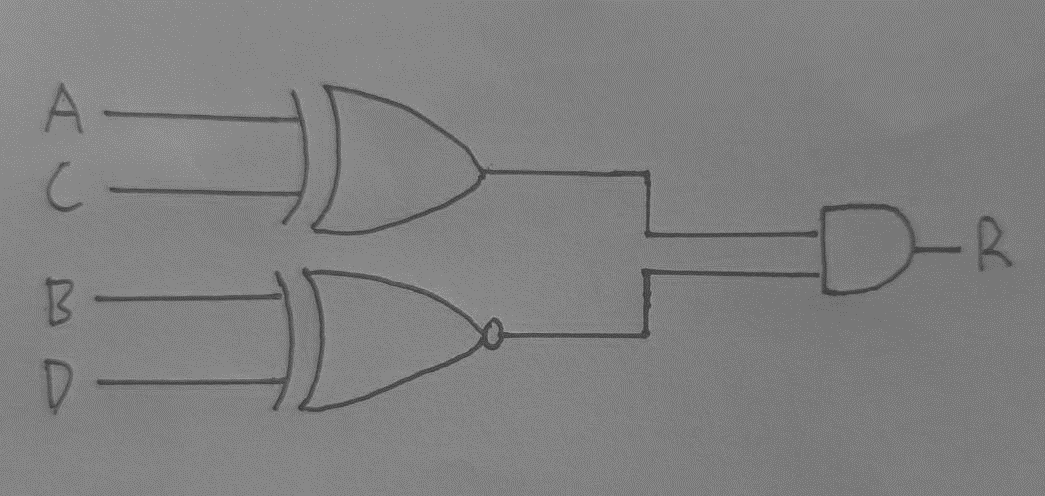
**Q5.** (Total: 3 marks)

Draw your circuit below.

**(A ⊕ C) · (B ⊙ D)**

**B ⊙ D**

**A ⊕ C**



**Q6.** (Total: 7 marks)

6

(a) Number of PIs in the K-map of : [1 mark]

1

(b) Number of EPIs in the K-map of : [1 mark]

3

(c) Number of distinct simplified SOP expressions for : [1 mark]

(d) One simplified SOP expression for : [2 marks]

A’ ⋅ B’ + B ⋅ C + B’ ⋅ D

(e) One simplified POS expression for : [2 marks]

(B’ + C) ⋅ (A’ + B + D)

**Q7.** (Total:3 marks)

(a) [1 mark]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | X |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | X |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | X |
| 1 | 0 | 0 | 1 | X |
| 1 | 0 | 1 | 0 | X |
| 1 | 0 | 1 | 1 | X |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | X |
| 1 | 1 | 1 | 1 | 1 |

(b) Simplified SOP expression [2 marks]

A ⋅ C + B’ ⋅ D’ + A’ ⋅ B ⋅ C’ ⋅ D

**Workings**

Write your workings here. They will not be graded, but the grader might look at it to figure out where you went wrong.

**Workings for Q3**

3110 = 0111112

Therefore, M31 = A + B’ + C’ + D’ + E’ + F’

2910 = 0111012

Therefore, m29 = A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F

m29 ⋅ M31

= A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ (A + B’ + C’ + D’ + E’ + F’)

= A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ A

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ B’

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ C’

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ D’

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ E’

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ F’

= A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ E’ (Inverse/Complement Law + 0 Element Theorem)

= A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F (Idempotency Theorem)

**K-map for Q6**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | X | 1 | 1 | 1 |
| 01 | 0 | 0 | 1 | X |
| 11 | 0 | 0 | X | 1 |
| 10 | X | X | 1 | 0 |