**CS2100 Assignment #2**

AY2024/25 Semester 1

**Deadline: Monday, 14 October 2024, 1:00pm**

TEMPLATE FOR SUBMISSION

36

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Full name: Tutorial grp: **T**

**Q1.** (Total: 15 marks)

17

Cycle time: ps [4 marks]

58.8

Clock frequency: GHz [3 marks]

10

Time taken for beq instruction: ps [3 marks]

ALU

Optimization: new [5 marks]

Explain your answers below.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Instruction Mem (ps) | Register Read (ps) | ALU  (ps) | Mem Read (ps) | Mem Write (ps) | Register Write (ps) | Total (ps) |
| addi | 5 | 1 | 4 | - | - | 1 | 11 |
| lw | 5 | 1 | 4 | 5 | - | 1 | 16 |
| sw | 5 | 1 | 4 | - | 7 | - | 17 |
| beq | 5 | 1 | 4 | - | - | - | 10 |

Note:

* Register File (includes Reg Read and Reg Write, 2 ps assumed to be split evenly among them)
* Data Mem (includes Mem Read and Mem Write, cannot have both concurrently)
* Instruction Mem assumed to take 5 ps as Data Mem takes 5 ps for Mem Read, Data Mem is also a mem and we are reading a mem from Instruction Mem too (same operation).

Since sw is the slowest instruction with the longest total execution time of 17 ps, and the datapath is single-cycle, it forms the critical path and hence Cycle Time = 17 ps.

Freq = 1 / Period. Therefore,

Clock Frequency

= 1 / (17 \* 10-12 \* 109)

= 58.8 GHz (3 s.f.)  
Note:

* 10-12 to convert ps to s
* 109 to convert Hz to GHz

<continued below…>

After optimization with new Register File that takes 1 ps (assumed to be split evenly among Reg Read and Reg Write):

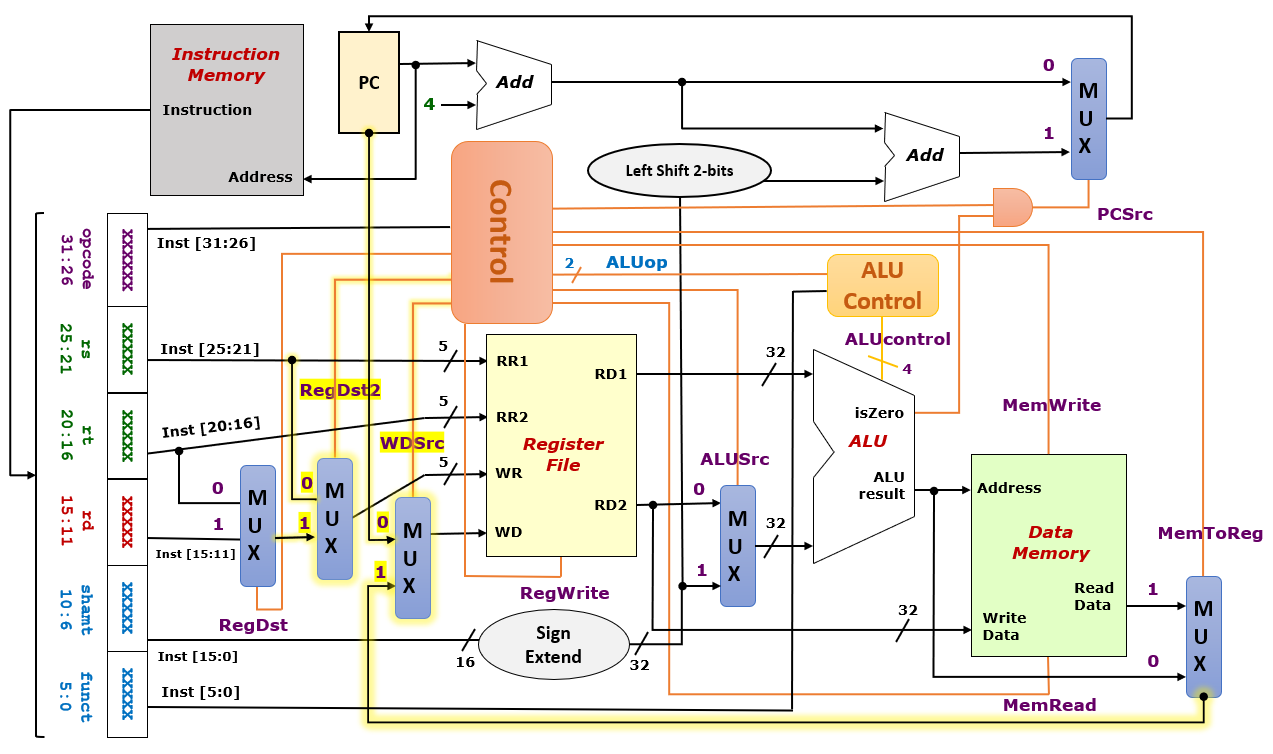
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Instruction Mem (ps) | Register Read (ps) | ALU  (ps) | Mem Read (ps) | Mem Write (ps) | Register Write (ps) | Total (ps) |
| addi | 5 | 0.5 | 4 | - | - | 0.5 | 10 |
| lw | 5 | 0.5 | 4 | 5 | - | 0.5 | 15 |
| sw | 5 | 0.5 | 4 | - | 7 | - | 16.5 |
| beq | 5 | 0.5 | 4 | - | - | - | 9.5 |

After optimization with new ALU that takes 2 ps:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Instruction Mem (ps) | Register Read (ps) | ALU  (ps) | Mem Read (ps) | Mem Write (ps) | Register Write (ps) | Total (ps) |
| addi | 5 | 1 | 2 | - | - | 1 | 9 |
| lw | 5 | 1 | 2 | 5 | - | 1 | 14 |
| sw | 5 | 1 | 2 | - | 7 | - | 15 |
| beq | 5 | 1 | 2 | - | - | - | 8 |

After applying both optimizations separately, it is clear that having the new ALU will decrease the total execution time of each instruction more than the new Register File. Hence, I will go for the new ALU.

**Q2.** (Total: 5 marks)



Note: The yellow highlighted parts are the changes

<continued below…>

When the opcode of whatiispc is detected by the Control Unit of the MIPS Processor, a control signal is sent to the new created multiplexer to ensure that the 1st operand input to the ALU is the current PC value instead of RD1.

**Q3.** (Total: 3 marks)

(a) [1 mark]

(b) [2 marks]

**Q4.** (Total: 4 marks)

(a) [2 marks]

(b) ( ) [2 marks]

**Q5.** (Total: 3 marks)

Draw your circuit below.

**Q6.** (Total: 7 marks)

(a) Number of PIs in the K-map of : [1 mark]

(b) Number of EPIs in the K-map of : [1 mark]

(c) Number of distinct simplified SOP expressions for : [1 mark]

(d) One simplified SOP expression for : [2 marks]

(e) One simplified POS expression for : [2 marks]

**Q7.** (Total:3 marks)

(a) [1 mark]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 0 |  |
| 0 | 1 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 |  |

(b) Simplified SOP expression [2 marks]

**Workings**

Write your workings here. They will not be graded, but the grader might look at it to figure out where you went wrong.

**Workings for Q3**

**K-map for Q6**