**CS2100 Assignment #2**

AY2024/25 Semester 1

**Deadline: Monday, 14 October 2024, 1:00pm**

TEMPLATE FOR SUBMISSION

36

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Full name: Tutorial grp: **T**

**Q1.** (Total: 15 marks)

17

Cycle time: ps [4 marks]

58.8

Clock frequency: GHz [3 marks]

10

Time taken for beq instruction: ps [3 marks]

ALU

Optimization: new [5 marks]

Explain your answers below.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Instruction Mem (ps) | Register Read (ps) | ALU  (ps) | Mem Read (ps) | Mem Write (ps) | Register Write (ps) | Total (ps) |
| addi | 5 | 1 | 4 | - | - | 1 | 11 |
| lw | 5 | 1 | 4 | 5 | - | 1 | 16 |
| sw | 5 | 1 | 4 | - | 7 | - | 17 |
| beq | 5 | 1 | 4 | - | - | - | 10 |

Note:

* Register File (includes Reg Read and Reg Write, 2 ps assumed to be split evenly among them)
* Data Mem (includes Mem Read and Mem Write, cannot have both concurrently)
* Instruction Mem assumed to take 5 ps as Data Mem takes 5 ps for Mem Read, Data Mem is also a mem and we are reading a mem from Instruction Mem too (same operation).

Since sw is the slowest instruction with the longest total execution time of 17 ps, and the datapath is single-cycle, it forms the critical path and hence Cycle Time = 17 ps.

Freq = 1 / Period. Therefore,

Clock Frequency

= 1 / (17 \* 10-12 \* 109)

= 58.8 GHz (3 s.f.)  
Note:

* 10-12 to convert ps to s
* 109 to convert Hz to GHz

<continued below…>

After optimization with new Register File that takes 1 ps (assumed to be split evenly among Reg Read and Reg Write):

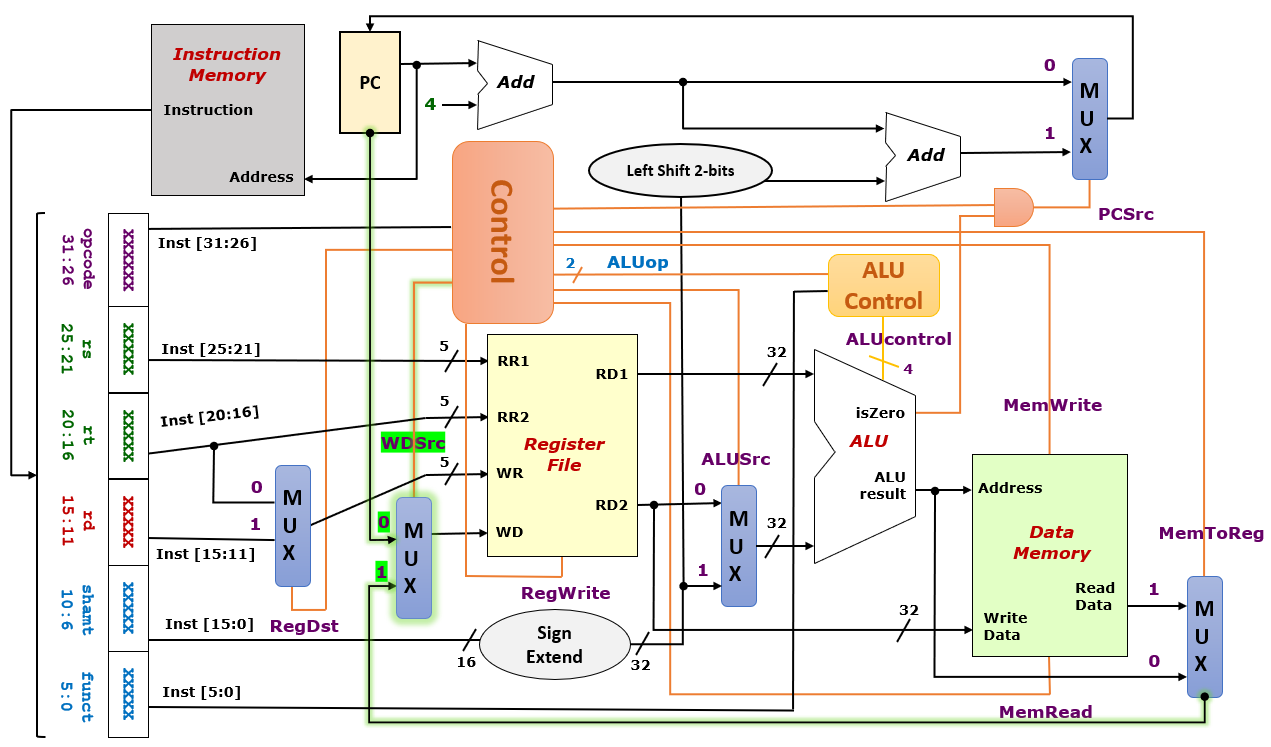
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Instruction Mem (ps) | Register Read (ps) | ALU  (ps) | Mem Read (ps) | Mem Write (ps) | Register Write (ps) | Total (ps) |
| addi | 5 | 0.5 | 4 | - | - | 0.5 | 10 |
| lw | 5 | 0.5 | 4 | 5 | - | 0.5 | 15 |
| sw | 5 | 0.5 | 4 | - | 7 | - | 16.5 |
| beq | 5 | 0.5 | 4 | - | - | - | 9.5 |

After optimization with new ALU that takes 2 ps:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Instruction Mem (ps) | Register Read (ps) | ALU  (ps) | Mem Read (ps) | Mem Write (ps) | Register Write (ps) | Total (ps) |
| addi | 5 | 1 | 2 | - | - | 1 | 9 |
| lw | 5 | 1 | 2 | 5 | - | 1 | 14 |
| sw | 5 | 1 | 2 | - | 7 | - | 15 |
| beq | 5 | 1 | 2 | - | - | - | 8 |

After applying both optimizations separately, it is clear that having the new ALU will decrease the total execution time of each instruction more than the new Register File. Hence, I will go for the new ALU.

**Q2.** (Total: 5 marks)



Note: The green highlighted parts are the changes

<continued below…>

The new instruction is given as whatiispc $R where $R is rt in the instruction register since the instruction is of I-format.

When the opcode of whatiispc is detected by the Control Unit of the MIPS Processor, the new control signal called WDSrc (stands for “Write Data Source”) will have the value 0 (instead of the value 1 for other instructions that use WD).

The new multiplexer will use WDSrc to select the current PC value to store as Write Data (WD), which will then be written into Write Register (WR), which is $R, by the Register File eventually.

Value of controls signals (X stands for “don’t care” [can be 0 or 1])

RegDst: 0

ALUSrc: X

MemToReg: X

RegWrite: 1

MemRead: 0 (I put 0 over X as MemRead and MemWrite cannot be 1 simultaneously)

MemWrite: 0 (I put 0 over X as MemRead and MemWrite cannot be 1 simultaneously)

PCSrc: 0

WDSrc: 0

**Q3.** (Total: 3 marks)

A + B’ + C’ + D’ + E’ + F’

(a) [1 mark]

A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F

(b) [2 marks]

**Q4.** (Total: 4 marks)

(a) [2 marks]

(b) (1, 5, 8, 12) [2 marks]

**Q5.** (Total: 3 marks)

Draw your circuit below.

**Q6.** (Total: 7 marks)

(a) Number of PIs in the K-map of : [1 mark]

(b) Number of EPIs in the K-map of : [1 mark]

(c) Number of distinct simplified SOP expressions for : [1 mark]

(d) One simplified SOP expression for : [2 marks]

(e) One simplified POS expression for : [2 marks]

**Q7.** (Total:3 marks)

(a) [1 mark]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 0 |  |
| 0 | 1 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 |  |

(b) Simplified SOP expression [2 marks]

**Workings**

Write your workings here. They will not be graded, but the grader might look at it to figure out where you went wrong.

**Workings for Q3**

3110 = 0111112

Therefore, M31 = A + B’ + C’ + D’ + E’ + F’

2910 = 0111012

Therefore, m29 = A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F

m29 ⋅ M31

= A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ (A + B’ + C’ + D’ + E’ + F’)

= A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ A

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ B’

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ C’

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ D’

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ E’

+ A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ F’

= A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F ⋅ E’ (Inverse/Complement Law + 0 Element Theorem)

= A’ ⋅ B ⋅ C ⋅ D ⋅ E’ ⋅ F (Idempotency Theorem)

**K-map for Q6**